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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	8MHz
Connectivity	I²C, SPI
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	12
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.72V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	24-VFQFN Exposed Pad
Supplier Device Package	24-HVQFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc8n04fhi24z

- Unique device serial number for identification

3. Applications

- Configurable LED strip/christmas tree LEDs via NFC
- Smart toy/interactive robot data logger
- Buttonless/contactless control panel
- Contactless diagnostic
- NFC e-locker
- Smart manufacturing
- NFC OTA

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
LPC8N04FHI24	HVQFN24	plastic thermal enhanced very thin quad flat package; no leads; 24 terminals; body 4 × 4 × 0.85 mm	SOT616-3

5. Marking

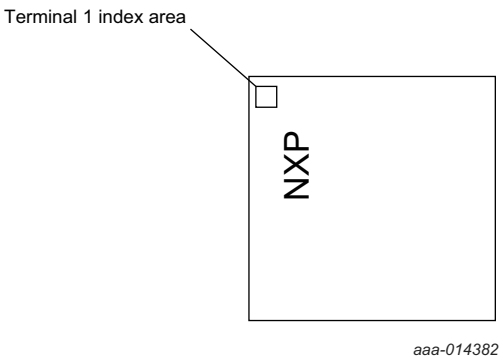


Fig 1. HVQFN24 package marking

The LPC8N04 HVQFN24 package has the following top-side marking:

- First line: Syww
  - yww: Date code with y = year and ww = week.
- Second line: xxxx
- Third line: LPC8N04

6. Block diagram

The internal block diagram of the LPC8N04 is shown in Figure 2. It consists of a Power Management Unit (PMU), clocks, timers, a digital computation and control cluster (ARM Cortex-M0+ and memories) and AHB-APB slave modules.

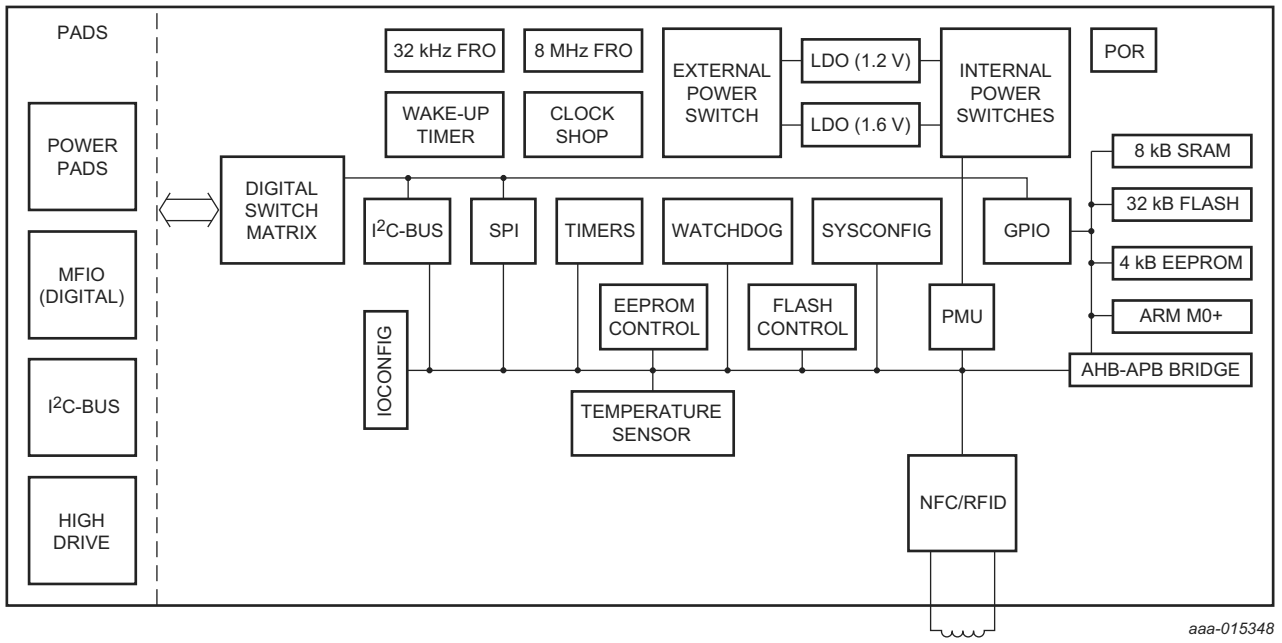


Fig 2. LPC8N04 block diagram

7. Pinning information

7.1 Pinning

7.1.1 HVQFN24 package

Figure 3 shows the pad layout of the LPC8N04 in the HVQFN24 package.

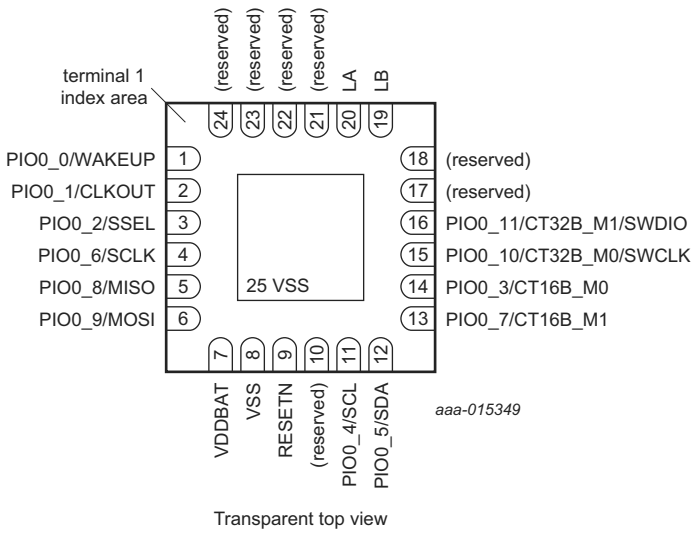


Fig 3. Pad configuration HVQFN24

Table 2. Pad allocation table of the HVQFN24 package

Pad	Symbol	Pad	Symbol
1	PIO0_0/WAKEUP	13[1]	PIO0_7/CT16B_M1
2	PIO0_1/CLKOUT	14[1]	PIO0_3/CT16B_M0
3	PIO0_2/SSEL	15[1]	PIO0_10/CT32B_M0/SWCLK
4	PIO0_6/SCLK	16[1]	PIO0_11/CT32B_M1/SWDIO
5	PIO0_8/MISO	17[2]	RESERVED
6	PIO0_9/MOSI	18[2]	RESERVED
7	VDDBAT	19	LB
8	VSS	20	LA
9	RESETN	21[2]	RESERVED
10	RESERVED	22[2]	RESERVED
11	PIO0_4/SCL	23[2]	RESERVED
12	PIO0_5/SDA	24[2]	RESERVED

[1] High source current pads; see Section 8.6.3.

[2] These pads must be tied to ground.

The SFRO runs at 8 MHz. The system clock is derived from it and can be set to 8 MHz, 4 MHz, 2 MHz, 1 MHz, 500 kHz, 250 kHz, 125 kHz or 62.5 kHz (Note: some features are not available when using the lower clock speeds). The TFRO runs at 32.768 kHz and is the clock source for the timer unit. The TFRO cannot be disabled.

Following reset, the LPC8N04 starts operating at the default 500 kHz system clock frequency to minimize dynamic current consumption during the boot cycle.

The SYSAHBCLKCTRL register gates the system clock to the various peripherals and memories. The temperature sensor receives a fixed clock frequency, irrespective of the system clock divider settings, while the digital part uses the system clock (AHB clock 0).

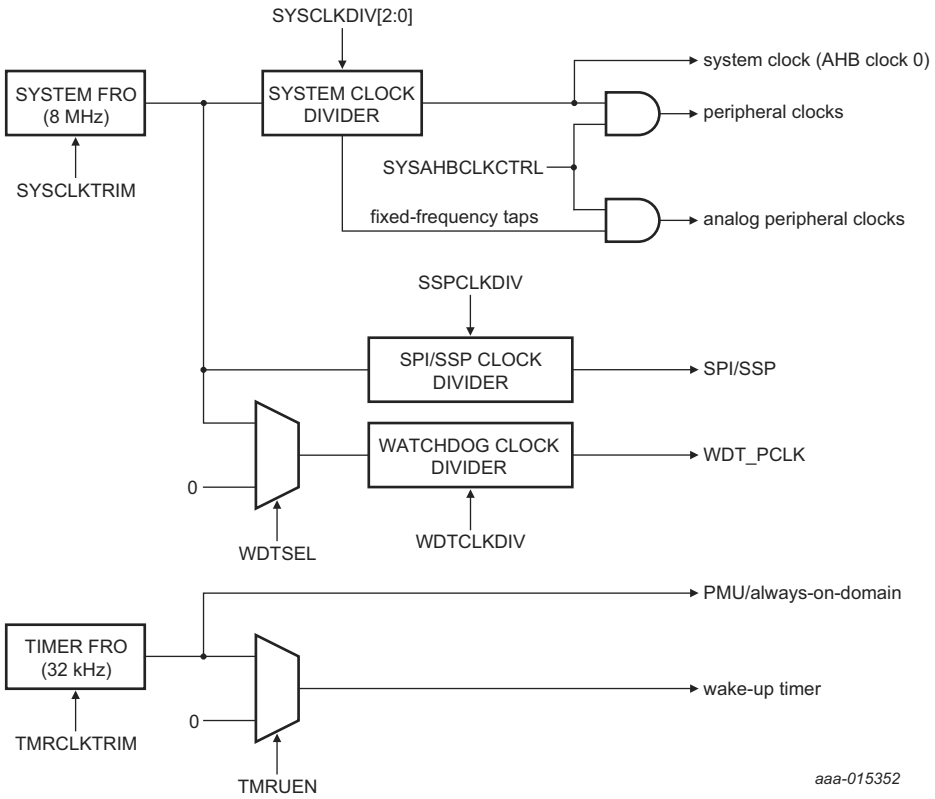


Fig 5. LPC8N04 clock generator block diagram

8.3.2 Reset

Reset has three sources on the LPC8N04: the RESETN pin, watchdog reset and a software reset.

Table 4. IC power states

State	VDD_ALON	DPDN[1]	Sleep or Deep-sleep	LDO1 1.2 V	LDO2 1.6 V
NOPOWER	no	X[2]	X[2]	off	off
ACTIVE	yes	0	0	on	on
DEEPPDN	yes	1	0	off	off
SLEEP/DEEPSLEEP	yes	0	1	on	on

[1] DPDN indicates whether the system is in deep power-down mode.

[2] X = don't care.

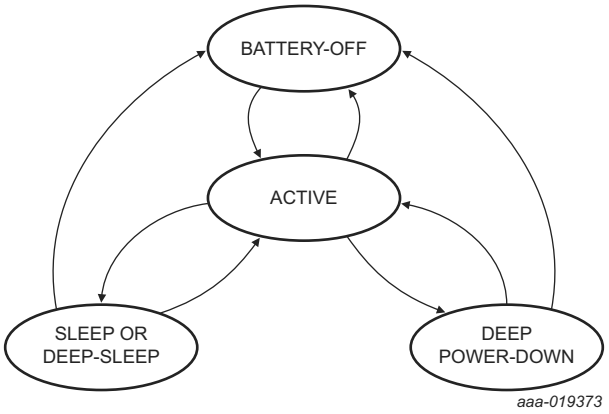


Fig 7. PMU state transition diagram

The power-up sequence is shown in Figure 8. Applying battery power when the PSWBAT switch is closed, or NFC power becomes available, provides the always-on part with a Power-On Reset (POR) signal. The TFRO is initiated which starts a state machine in the PMU. In the first state, the LDO1V2 powering the digital domain is started. In the second state, the LDO1V6 powering the analog domain is started which starts the flash memory. Enabling the LDO1V2, and the SFRO stabilizing, triggers the system_por. The system is now considered to be 'on'. The system can boot when the flash memory is fully operational.

The total start-up time from trigger to active mode/boot is about 2.5 ms.

If there is no battery power, but there is RF power, the same procedure is followed except that PSWNFC connects power to the LDOs.

The user cannot disable the TFRO as it is used by the PMU.

Remark: When running without a battery, energy harvesting is limited to 2 MHz system clock.

Table 5. State transition events for DEEPSLEEP to ACTIVE

Event	Description
RESETN	reset asserted
RTC event	if the timer reaches preset value
Watchdog	watchdog issues interrupt or reset
WAKEUP	signal on WAKEUP pin
RF field	RF field is detected, potential NFC command input (if set in PMU)
Start logic interrupt	one of the enabled start logic interrupts is asserted

Table 6. State transition events for DEEPPDN to ACTIVE

Event	Description
RESETN	reset asserted
RTC event	if the timer reaches preset value
WAKEUP	signal on WAKEUP pin (when enabled)
RF field	RF field is detected, potential NFC command input (if set in PMU)

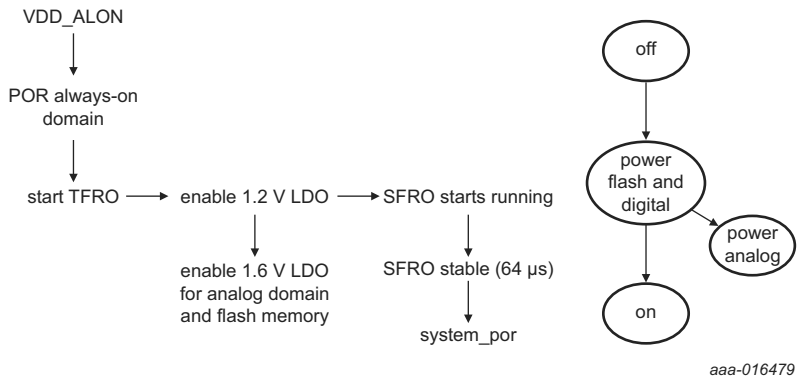


Fig 8. LPC8N04 power-up sequence

8.4.1.1 Applying power to the PCB/system with battery for the first time

To support long shelf life without draining the battery, the LPC8N04 is not connected to an external supply pin until RESET pin is asserted and de-asserted or the NFC field is present. Once the RESET or the NFC field is applied, the LPC8N04 is powered.

8.4.2 Power Management Unit (PMU)

The Power Management Unit (PMU) partly resides in the digital power domain and partly in the always-on domain. The PMU controls the sleep, deep sleep and deep power-down modes and the power flow to the different internal circuit blocks. Five general-purpose registers in the PMU can be used to retain data during deep power-down mode. These registers are located in the always-on domain. The PMU also raises a BOD interrupt, if necessary, if VDD_ALON drops below 1.8 V.

The power to the different APB analog slaves is controlled through a power-down configuration register.

[1] Interrupt 0 to 10 correspond to PIO0_0 to PIO0_10; interrupt 11 corresponds to RFID/NFC external access; interrupt 12 corresponds to the RTC on/off timer.

8.6 I/O configuration

The I/O configuration registers control the electrical characteristics of the pads. The following features are programmable:

- Pin function
- Internal pull-up/pull-down resistor or bus keeper function
- Low-pass filter
- I^2C-bus mode for pads hosting the I^2C-bus function

The IOCON registers control the function (GPIO or peripheral function), the input mode, and the hysteresis of all PIO0_m pins. In addition, the I^2C-bus pins can be configured for different I^2C-bus modes.

The FUNC bits in the IOCON registers can be set to GPIO (FUNC = 000) or to a peripheral function. If the pins are GPIO pins, the GPIO0DIR registers determine whether the pin is configured as an input or output. For any peripheral function, the pin direction is controlled automatically depending on the functionality of the pin. The GPIO0DIR registers have no effect on peripheral functions.

8.6.1 PIO0 pin mode

The MODE bits in the IOCON register allow the selection of on-chip pull-up or pull-down resistors for each pin, or to select the repeater mode. The possible on-chip resistor configurations are pull-up enabled, pull-down enabled, or no pull-up/pull-down. The default value is no pull-up or pull-down enabled. The repeater mode enables the pull-up resistor when the pin is at logic 1, and enables the pull-down resistor when the pin is at logic 0. This mode causes the pin to retain its last known state if it is configured as an input and is not driven externally. The state retention is not applicable to the deep power-down mode. Repeater mode is typically used to prevent a pin from floating when it is temporarily not driven. Allowing it to float could potentially use significant power.

8.6.2 PIO0 I^2C-bus mode

If the FUNC bits of registers PIO0_4 and PIO0_5 select the I^2C-bus function, the I^2C-bus pins can be configured for different I^2C-bus modes:

- Standard mode/fast mode I^2C-bus with input glitch filter (including an open-drain output according to the I^2C-bus specification)
- Standard open-drain I/O functionality without input filter

8.6.3 PIO0 current source mode

PIO0_3, PIO0_7, PIO0_10 and PIO0_11 are high-source pads that can deliver up to 20 mA to the load. These PIO pins can be set to either digital mode or analog current sink mode. In digital mode, the output voltage of the pad switches between VSS and VDD. In analog current drive mode, the output current sink switches between the values set by the ILO and IHI bits. The maximum pad voltage is limited to 5 V.

8.8 I²C-bus controller

8.8.1 Features

Standard I²C-bus compliant interfaces may be configured as master, slave, or master/slave.

- Arbitration is handled between simultaneously transmitting masters without corruption of serial data on the bus
- Programmable clock allows adjustment of I²C-bus transfer rates
- Data transfer is bidirectional between masters and slaves
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus
- Serial clock synchronization is used as a handshake mechanism to suspend and resume serial transfer
- Supports standard mode (100 kbit/s) and fast mode (400 kbit/s)
- Optional recognition of up to four slave addresses
- Monitor mode allows observing all I²C-bus traffic, regardless of slave address
- The I²C-bus can be used for test and diagnostic purposes
- The I²C-bus contains a standard I²C-bus compliant interface with two pins
- Possibility to wake up LPC8N04 on matching I²C-bus slave address

8.8.2 General description

Two types of data transfers are possible on the I²C-bus, depending on the state of the direction bit (R/W):

1. Data transfer from a master transmitter to a slave receiver. The first byte transmitted by the master is the slave address. Next follows a number of data bytes. The slave returns an acknowledge bit after each received byte.
2. Data transfer from a slave transmitter to a master receiver. The master transmits the first byte (the slave address). The slave then returns an acknowledge bit. The slave then transmits the data bytes to the master. The master returns an acknowledge bit after all received bytes other than the last byte. At the end of the last received byte, a not-acknowledge is returned. The master device generates all of the serial clock pulses and the START and STOP conditions. A transfer is ended with a STOP condition or with a repeated START condition. As a repeated START condition is also the beginning of the next serial transfer, the I²C-bus is not released.

The I²C-bus interface is byte oriented and has four operating modes: master transmitter mode, master receiver mode, slave transmitter mode and slave receiver mode.

The I²C-bus interface is completely I²C-bus compliant, supporting the ability to power off the LPC8N04 independent of other devices on the same I²C-bus.

The I²C-bus interface requires a minimum 2 MHz system clock to operate in normal mode, and 8 MHz for fast mode.

8.8.3 I²C-bus pin description

Table 8. I²C-bus pin description

Pin	Type	Description
SDA	I/O	I²C-bus serial data
SCL	I/O	I²C-bus serial clock

The I²C-bus pins must be configured through the PIO0_4 and PIO0_5 registers for standard mode or fast mode. The I²C-bus pins are open-drain outputs and fully compatible with the I²C-bus specification.

8.9 SPI controller

8.9.1 Features

- Compatible with Motorola SPI, 4-wire Texas Instruments Synchronous Serial Interface (SSI), and National Semiconductor Microwire buses
- Synchronous serial communication
- Supports master or slave operation
- Eight-frame FIFOs for both transmit and receive
- 4-bit to 16-bit frame

8.9.2 General description

The SPI/SSP is a Synchronous Serial Port (SSP) controller capable of operation on an SPI, 4-wire SSI, or Microwire bus. It can interact with multiple masters and slaves on the bus. Only a single master and a single slave can communicate on the bus during a given data transfer. Data transfers are in principle full duplex, with frames of 4 bits to 16 bits of bidirectional data flowing between master and slave. In practice, often only one of these two data flows carries meaningful data.

8.9.3 Pin description

Table 9. SPI pin description

Pin name	Type	Interface pin SPI	SSI	Microwire	Description
SCLK	I/O	SCLK	CLK	SK	serial clock
SSEL	I/O	SSEL	FS	CS	frame sync/slave select
MISO	I/O	MISO	DR (M) DX (S)	SI (M) SO (S)	master input slave output
MOSI	I/O	MOSI	DX (M) DR (S)	SO (M) SI (S)	master output slave input

Pin detailed descriptions

Serial clock — SCK/CLK/SK is a clock signal used to synchronize the transfer of data. The master drives the clock signal and the slave receives it. When SPI/SSP interface is used, the clock is programmable to be active HIGH or active LOW, otherwise it is always active HIGH. SCK only switches during a data transfer. At any other time, the SPI/SSP interface either stays in its inactive state or is not driven (remains in high-impedance state).

Frame sync/slave select — When the SPI/SSP interface is a bus master, it drives this signal to an active state before the start of serial data. It then releases it to an inactive state after the data has been sent. The active state can be HIGH or LOW depending upon the selected bus and mode. When the SPI/SSP interface is a bus slave, this signal qualifies the presence of data from the master according to the protocol in use.

When there is only one master and slave, the master signals, frame sync or slave select, can be connected directly to the corresponding slave input. When there are multiple slaves, further qualification of frame sync/slave select inputs is normally necessary to prevent more than one slave from responding to a transfer.

Master Input Slave Output (MISO) — The MISO signal transfers serial data from the slave to the master. When the SPI/SSP is a slave, it outputs serial data on this signal. When the SPI/SSP is a master, it clocks in serial data from this signal. It does not drive this signal and leaves it in a high-impedance state when the SPI/SSP is a slave and not selected by FS/SSEL.

Master Output Slave Input (MOSI) — The MOSI signal transfers serial data from the master to the slave. When the SPI/SSP is a master, it outputs serial data on this signal. When the SPI/SSP is a slave, it clocks in serial data from this signal.

8.10 RFID/NFC communication unit

8.10.1 Features

- ISO/IEC14443A part 1 to part 3 compatible
- MIFARE (Ultralight) EV1 compatible
- NFC Forum Type 2 compatible
- Easy interfacing with standard user memory space READ/WRITE commands
- Passive operation possible

8.10.2 General description

The RFID/NFC interface allows communication using 13.56 MHz proximity signaling.

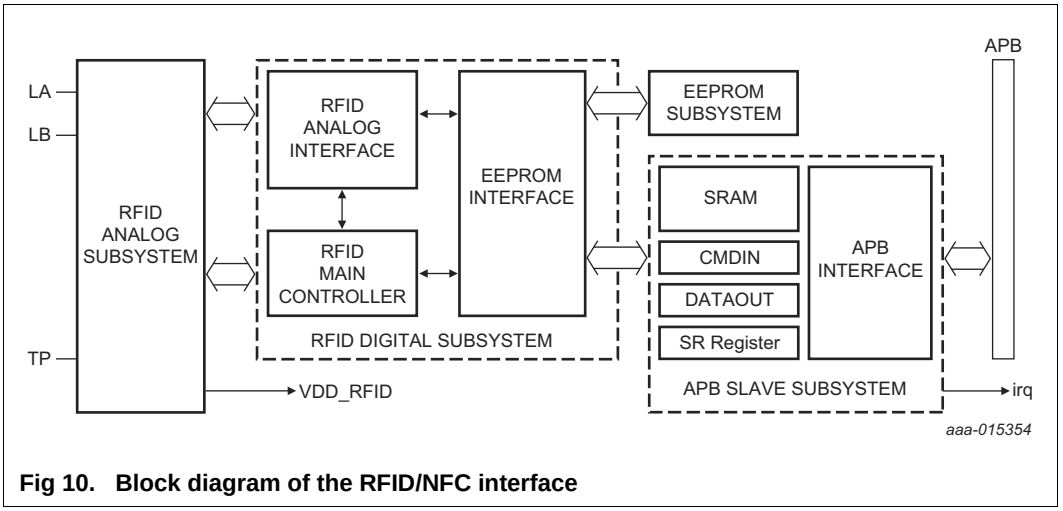


Fig 10. Block diagram of the RFID/NFC interface

8.18.3 Erasing/programming flash

Erasing and programming are separate operations. Both are possible only on memory sectors that are unprotected and unlocked. Protect/lock information is stored inside the memory itself, so the controller is not aware of protection status. Therefore, if a program/erase operation is performed on a protected or locked sector, it does not flag an error.

Protection — At exit from reset, all sectors are protected against accidental modification. To allow modification, a sector must be unprotected. It can then be protected again after that the modification is performed.

Locking — Each flash sector has a lock bit. Lock bits can be set but cannot be cleared. Locked sectors cannot be erased and reprogrammed.

8.19 On-chip SRAM

The LPC8N04 contains a total of 8 kB on-chip SRAM memory configured as $256 \times 2 \times 4 \times 32$ bit.

8.20 On-chip EEPROM

The LPC8N04 contains a 4 kB EEPROM. This EEPROM is organized in 64 rows of 32×16-bit words. Of these rows, the last four contain calibration and test data and are locked. This data is either used by the bootloader after reset, or made accessible to the application via firmware Application Programming Interface (API).

8.20.1 Reading from EEPROM

Reading is done via the AHB interface. The memory is mapped on the bus address space, as a contiguous address space. Memory data words are seen on the bus using a little endian arrangement.

8.20.2 Writing to EEPROM

Erasing and programming is performed, as a single operation, on one or more words inside a single page.

Previous write operations have transferred the data to be programmed into the memory page buffer. The page buffer tracks which words were written to (offset within the page only). Words not written to, retain their previous content.

9. Limiting values

Table 10. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		–0.5	+3.6	V
V_I	input voltage	normal PIO pads (V_{DD} = 0.6 V)	–0.5	+3.6	V
		high-source PIO pads	–0.5	+5.5	V
		LA/LB pads	–0.5	+5.5	V
I_{DD}	supply current	per supply pin	-	100	mA
I_{SS}	ground supply current	per supply pin	-	100	mA
I_{lu}	latch-up current	I/O; $-0.5V_{DD} < V_I < +1.5V_{DD}$; $T_j < 125$ °C	-	100	mA
T_{stg}	storage temperature		–40	+125	°C
T_j	junction temperature		-	125	°C
P_{tot}	total power dissipation		-	1	W
V_{ESD}	electrostatic discharge voltage	human body model; all pins	–2000	+2000	V
		charged device model; all pins	–500	+500	V

10. Static characteristics

Table 11. Static characteristics

T_{amb} = −40 °C to +85 °C, unless otherwise stated.

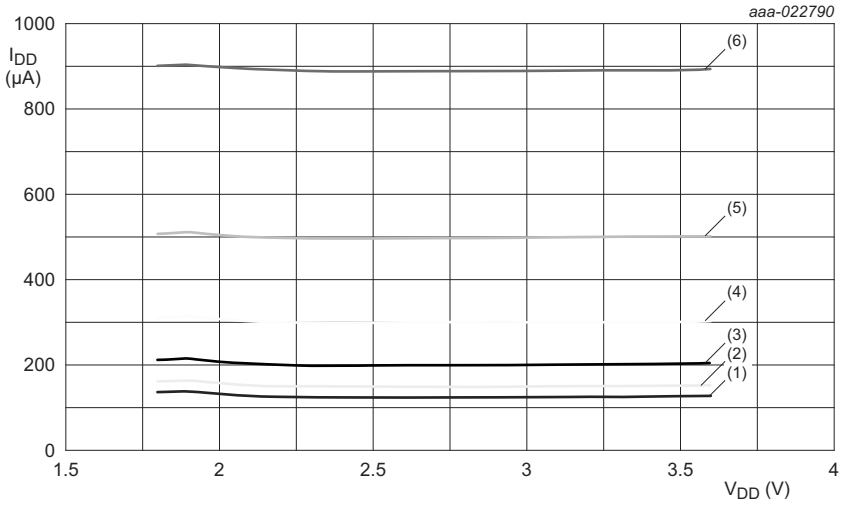
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply pins						
V_{DD}	supply voltage		1.72	3.0	3.60	V
I_{DD}	supply current	voltage and clock frequency dependent [1]	-	-	-	μA
$I_{L(off)}$	off-state leakage current		-	-	50	nA
$I_{DD(pd)}$	power-down mode supply current	deep power-down mode	-	3	-	μA
Standard GPIO pins						
V_{IH}	HIGH-level input voltage		0.7 × V_{DD}	-	-	V
V_{IL}	LOW-level input voltage		-	-	0.3 × V_{DD}	V
V_{hys}	hysteresis voltage		0.4	-	-	V
R_{pd}	pull-down resistance		-	72	-	kΩ
R_{pu}	pull-up resistance		-	73	-	kΩ
I_S	source current	HIGH-level V_{DD} = 1.8 V [2]	-	2	-	mA
		HIGH-level V_{DD} = 3.6 V [2]	-	8	-	mA
		LOW-level V_{DD} = 1.8 V [2]	-	4	-	mA
		LOW-level V_{DD} = 3.6 V [2]	-	16	-	mA
High-drive GPIO pins						
I_S	source current	HIGH-level V_{DD} = 1.8 V [3]	4	-	6	mA
		HIGH-level V_{DD} = 3.6 V [3]	13	-	18	mA
		LOW-level V_{DD} = 1.8 V [3]	5.5	-	8	mA
		LOW-level V_{DD} = 3.6 V [3]	22	-	32	mA
I^2C-bus pins						
I_S	source current	LOW-level V_{DD} = 1.8 V [4]	2	-	8.5	mA
		LOW-level V_{DD} = 3.6 V [4]	9.5	-	38	mA
Brownout detect						
$V_{trip(bo)}$	brownout trip voltage	falling V_{DD}	-	1.8	-	V
		rising V_{DD}	-	1.875	-	V
V_{hys}	hysteresis voltage		-	75	-	mV
General						
$R_{pu(int)}$	internal pull-up resistance	on pin RESETN	-	100	-	kΩ
C_{ext}	external capacitance	on pin RESETN	-	-	1	nF

[1] See Figure 11.

[2] PIO0_0, PIO0_1, PIO0_2, PIO0_6, PIO0_8, PIO0_9.

[3] PIO0_3, PIO0_7, PIO0_10, PIO0_11.

[4] PIO0_4, PIO0_5.



Plot of I_{DD} / V_{DD} when ARM running a while-1 loop in normal mode, no NFC field present.

(1) System clock = 250 kHz
(2) System clock = 500 kHz
(3) System clock = 1 MHz
(4) System clock = 2 MHz
(5) System clock = 4 MHz
(6) System clock = 8 MHz

Fig 11. Active current consumption

Table 12. Temperature sensor characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{CC(pd)}$	power-down mode supply current	TSENS disabled	-	-	1	nA
I_{stb}	standby current	TSENS enabled	-	6	7	μA
$I_{CC(oper)}$	operating supply current	TSENS converting	-	10	12	μA
T_{acc}	temperature accuracy		−1.5	-	+1.5	°C

Note: The absolute accuracy is valid for the factory calibration of the temperature sensor. The sensor can be user-calibrated to reach higher accuracy.

Table 13. Antenna input characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_i	input capacitance	[1]	-	50	-	pF
f_i	input frequency		-	13.56	-	MHz

[1] T_{amb} = 22 °C, f = 13.56 MHz, RMS voltage between LA and LB = 1.5 V.

Table 14. EEPROM characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{ret(data)}$	data retention time	T_{amb} = 22 °C	10	-	-	year

11. Dynamic characteristics

11.1 I/O pins

Table 15. I/O dynamic characteristics

These characteristics apply to standard port pins and RESETN pin.
T_{amb} = −40 °C to +85 °C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_r	rise time	pin configured as output	3.0	-	5.0	ns
t_f	fall time	pin configured as output	2.5	-	5.0	ns

11.2 I²C-bus

Table 16. I²C-bus dynamic characteristics

See UM10204 - I²C-bus specification and user manual (Ref. 3) for details.
T_{amb} = −40 °C to +85 °C[1]; see the timing diagram in Figure 12.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCL}	SCL clock frequency	standard mode	0	-	100	kHz
		fast mode	0	-	400	kHz
t_f	fall time of both SDA and SCL signals	standard mode [2][3][4]	-	-	300	ns
		fast mode [2][3][4]	$20 + 0.1 \times C_b$	-	300	ns
t_{LOW}	LOW period of the SCL clock	standard mode	4.7	-	-	µs
		fast mode	1.3	-	-	µs
t_{HIGH}	HIGH period of the SCL clock	standard mode	4.0	-	-	µs
		fast mode	0.6	-	-	µs
$t_{HD;DAT}$	data hold time	standard mode [2][5][6]	0	-	-	µs
		fast mode [2][5][6]	0	-	-	µs
$t_{SU;DAT}$	data set-up time	standard mode [7][8]	250	-	-	ns
		fast mode [7][8]	100	-	-	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] A device must internally provide a hold time of at least 300 ns for the SDA signal (regarding the $V_{IH(min)}$ of the SCL signal). The hold time is to bridge the undefined region of the falling edge of SCL.

[3] C_b = total capacitance of one bus line in pF.

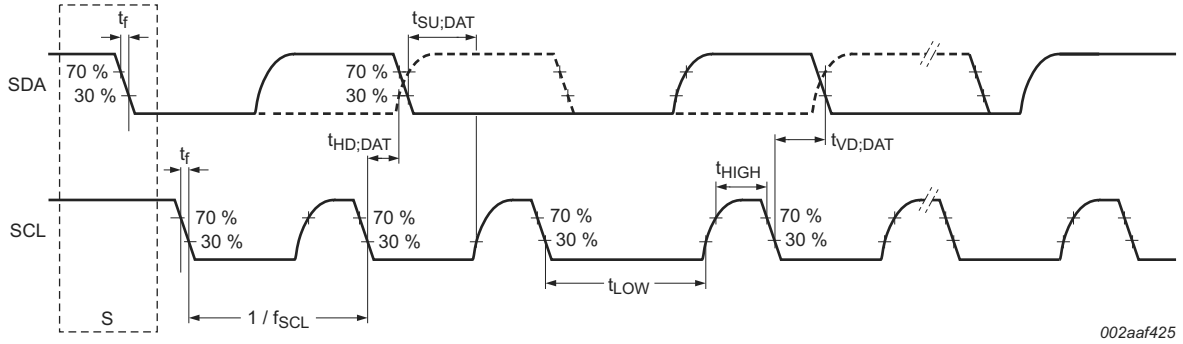
[4] The maximum t_f for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time for the SDA output stage t_f is specified at 250 ns. It allows series protection resistors to be connected between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_f.

[5] $t_{HD;DAT}$ is the data hold time that is measured from the falling edge of SCL; applies to data in transmission and the acknowledge.

[6] The maximum $t_{HD;DAT}$ could be 3.45 µs and 0.9 µs for standard mode and fast mode. However, it must be less than the maximum of $t_{VD;DAT}$ or $t_{VD;ACK}$ by a transition time (see Ref. 3). Only meet this maximum if the device does not stretch the LOW period (t_{LOW}) of the SCL signal. If the clock stretches the SCL, the data must be valid by the set-up time before it releases the clock.

[7] $t_{SU;DAT}$ is the data set-up time that is measured against the rising edge of SCL; applies to data in transmission and the acknowledge.

[8] A fast mode I²C-bus device can be used in a standard-mode I²C-bus system but it must meet the requirement $t_{SU;DAT}$ = 250 ns. This requirement is automatically the case if the device does not stretch the LOW period of the SCL signal. If it does, it must output the next data bit to the SDA line $t_{r(max)} + t_{SU;DAT} = 1000 + 250 = 1250$ ns before the SCL line is released. This procedure is in accordance with the standard-mode I²C-bus specification. Also, the acknowledge timing must meet this set-up time.



S = START condition

Fig 12. I²C-bus pins clock timing

11.3 SPI interfaces

Table 17. Dynamic characteristics of SPI pins in SPI mode

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SPI master						
$t_{cy(clk)}$	clock cycle time	full-duplex mode [1]	50	-	-	ns
		when only transmitting [1]	40	-	-	ns
$t_{SU;DAT}$	data set-up time	2.4 V ≤ V_{DD} < 3.6 V [2]	15	-	-	ns
		2.0 V ≤ V_{DD} < 2.4 V [2]	20	-	-	ns
		1.8 V ≤ V_{DD} < 2.0 V [2]	24	-	-	ns
$t_{HD;DAT}$	data hold time	[2]	0	-	-	ns
$t_{v(Q)}$	data output valid time	[2]	-	-	10	ns
$t_{h(Q)}$	data output hold time	[2]	0	-	-	ns
SPI slave						
$T_{cy(PCLK)}$	PCLK cycle time	[3][4]	0	-	-	ns
$t_{HD;DAT}$	data hold time	[3][4]	3 × $T_{cy(PCLK)}$ + 4	-	-	ns
$t_{v(Q)}$	data output valid time	[3][4]	-	-	3 × $T_{cy(PCLK)}$ + 11	ns
$t_{h(Q)}$	data output hold time	[3][4]	-	-	2 × $T_{cy(PCLK)}$ + 5	ns

[1] $t_{cy(clk)}$ = (SSPCLKDIV × (1 + SCR) × CPSDVSR) / f_{main}. The clock cycle time derived from the SPI bit rate $t_{cy(clk)}$ is a function of:
a) the main clock frequency f_{main}
b) the SPI peripheral clock divider (SSPCLKDIV)
c) the SPI SCR parameter (specified in the SSP0CR0 register)
d) the SPI CPSDVSR parameter (specified in the SPI clock prescale register)

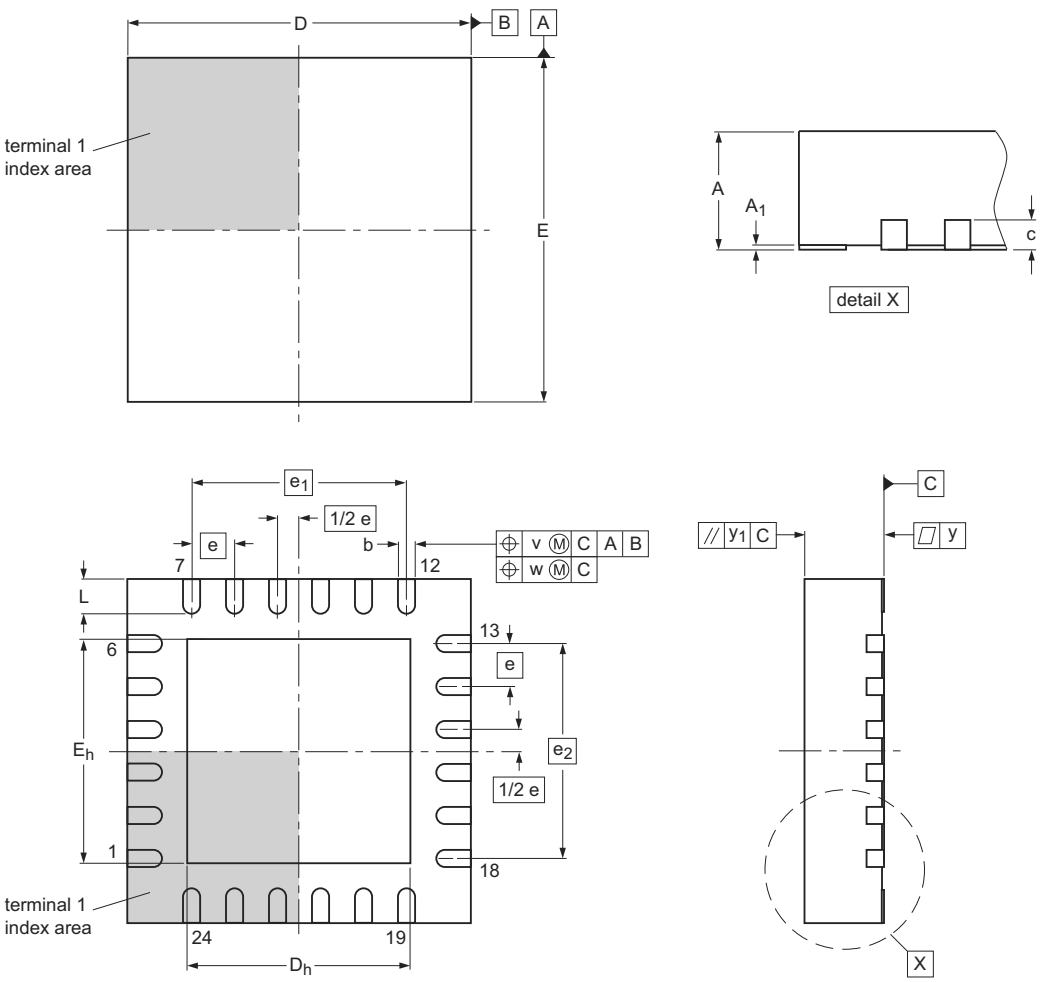
[2] T_{amb} = −40 °C to +105 °C.

[3] $t_{cy(clk)}$ = 12 × $T_{cy(PCLK)}$.

[4] T_{amb} = 25 °C for normal voltage supply: V_{DD} = 3.3 V.

12. Package outline

HVQFN24: plastic thermal enhanced very thin quad flat package; no leads; 24 terminals; body 4 x 4 x 0.85 mm **SOT616-3**



Dimensions (mm are the original dimensions)

Unit(1)		A(1)	A_1	b	c	D(1)	D_h	E(1)	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	max	1	0.05	0.30		4.1	2.75	4.1	2.75				0.5				
	nom				0.2					0.5	2.5	2.5		0.1	0.05	0.05	0.1
	min		0.00	0.18		3.9	2.45	3.9	2.45				0.3				

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot616-3_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT616-3		MO-220				~~16-02-17~~ 16-07-14

Fig 15. HVQFN24 package outline

13. Abbreviations

Table 18. Abbreviations

Acronym	Description
ADC	Analog-to-Digital Converter
AHB	Advanced High-performance Bus
AMBA	Advanced Microcontroller Bus Architecture
APB	Advanced Peripheral Bus
API	Application Programming Interface
ARM	Advanced RISC Machine
BOD	BrownOut Detection
CGU	Clock Generator Unit
EEPROM	Electrically Erasable Programmable Read-Only Memory
GPIO	General Purpose Input Output
I^2C	Inter-Integrated Circuit
LDO	Low DropOut
MISO	Master Input Slave Output
MOSI	Master Output Slave Input
NDEF	NFC Data Exchange Format
NFC	Near Field Communication
NVIC	Nested Vectored Interrupt Controller
PMU	Power Management Unit
POR	Power-On Reset
PWM	Pulse Width Modulation
RFID	Radio Frequency Identification
RISC	Reduced Instruction Set Computer
RTC	Real-Time Clock
SFRO	System Free-Running Oscillator
SI	Slave Input
SO	Slave Output
SPI	Serial Peripheral Interface
SR	Status Register
SSI	Synchronous Serial Interface
SSP	Synchronous Serial Port
SWD	Serial Wire Debug
TFRO	Timer Free-Running Oscillator
WDT	WatchDog Timer

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20. Contents

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