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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

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Details

Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I ² C, SCI, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	26
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.63V
Data Converters	A/D 10x12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount, Wettable Flank
Package / Case	32-VFQFN Exposed Pad
Supplier Device Package	32-VQFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsamda1e16b-mbt

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
Access								
Reset								
Bit	15	14	13	12	11	10	9	8
Access								
Reset								
Bit	7	6	5	4	3	2	1	0
								SMEMP
Access								R
Reset								x

Bit 0 – SMEMP: System Memory Present

This bit indicates whether system memory is present on the bus that connects to the ROM table.

This bit is set at power-up if the device is not protected, indicating that the system memory is accessible from a debug adapter.

This bit is cleared at power-up if the device is protected, indicating that the system memory is not accessible from a debug adapter.

15.13.14 Peripheral Identification 4

Name: PID4
Offset: 0x1FD0 [ID-00001c14]
Reset: 0x00000000
Property: -

Value	Description
0	The APBA clock for the PM is stopped.
1	The APBA clock for the PM is enabled.

Bit 0 – PAC0: PAC0 APB Clock Enable

Value	Description
0	The APBA clock for the PAC0 is stopped.
1	The APBA clock for the PAC0 is enabled.

18.8.9 APBB Mask

Name: APBBMASK
Offset: 0x1C [ID-00001b7b]
Reset: 0x0000007F
Property: Write-Protected

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
Access								
Reset								
Bit	15	14	13	12	11	10	9	8
Access								
Reset								
Bit	7	6	5	4	3	2	1	0
			USB	DMAC	PORT	NVMCTRL	DSU	PAC1
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			1	1	1	1	1	1

Bit 5 – USB: USB APB Clock Enable

Value	Description
0	The APBB clock for the USB is stopped.
1	The APBB clock for the USB is enabled.

Bit 4 – DMAC: DMAC APB Clock Enable

Value	Description
0	The APBB clock for the DMAC is stopped.
1	The APBB clock for the DMAC is enabled.

Bit 3 – PORT: PORT APB Clock Enable

- 32KHz to 2MHz input reference clock frequency range
 - Three possible sources for the reference clock
 - Adjustable proportional integral controller
 - Fractional part used to achieve 1/16th of reference clock step
- 3.3V Brown-Out Detector (BOD33)
 - Programmable threshold
 - Threshold value loaded from Flash User Calibration at startup
 - Triggers resets or interrupts
 - Operating modes:
 - Continuous mode
 - Sampled mode for low power applications (programmable refresh frequency)
 - Hysteresis
- Internal Voltage Regulator system (VREG)
 - Operating modes:
 - Normal mode
 - Low-power mode
 - With an internal non-configurable Brown-out detector (BOD12)
- 1.2V Brown-Out Detector (BOD12)
 - Programmable threshold
 - Threshold value loaded from Flash User Calibration at start-up
 - Triggers resets or interrupts
 - Operating modes:
 - Continuous mode
 - Sampled mode for low power applications (programmable refresh frequency)
 - Hysteresis
- Voltage Reference System (VREF)
 - Bandgap voltage generator with programmable calibration value
 - Temperature sensor
 - Bandgap calibration value loaded from Flash Factory Calibration at start-up

21.5.2 Power Management

The RTC will continue to operate in any sleep mode where the selected source clock is running. The RTC interrupts can be used to wake up the device from sleep modes. Events connected to the event system can trigger other operations in the system without exiting sleep modes. Refer to the *Power Manager* for details on the different sleep modes.

The RTC will be reset only at power-on (POR) or by setting the Software Reset bit in the Control register (CTRL.SWRST=1).

Related Links

[PM – Power Manager](#)

21.5.3 Clocks

The RTC bus clock (CLK_RTC_APB) can be enabled and disabled in the Power Manager, and the default state of CLK_RTC_APB can be found in the Peripheral Clock Masking section.

A generic clock (GCLK_RTC) is required to clock the RTC. This clock must be configured and enabled in the Generic Clock Controller before using the RTC. Refer to *GCLK – Generic Clock Controller* for details.

This generic clock is asynchronous to the user interface clock (CLK_RTC_APB). Due to this asynchronicity, accessing certain registers will require synchronization between the clock domains. Refer to [Synchronization](#) for further details.

The RTC should not work with the Generic Clock Generator 0.

Related Links

[Peripheral Clock Masking](#)

[GCLK - Generic Clock Controller](#)

21.5.4 DMA

Not applicable.

21.5.5 Interrupts

The interrupt request line is connected to the Interrupt Controller. Using the RTC interrupts requires the Interrupt Controller to be configured first. Refer to *Nested Vector Interrupt Controller* for details.

Related Links

[Nested Vector Interrupt Controller](#)

21.5.6 Events

The events are connected to the *Event System*.

Related Links

[EVSYS – Event System](#)

21.5.7 Debug Operation

When the CPU is halted in debug mode the RTC will halt normal operation. The RTC can be forced to continue operation during debugging. Refer to the Debug Control (DBGCTRL) register for details.

21.5.8 Register Access Protection

Registers with write-access can be optionally write-protected by the Peripheral Access Controller (PAC), except for the following:

- Interrupt Flag Status and Clear register (INTFLAG)

Offset	Name	Bit Pos.								
0x0D ... 0x0F	Reserved									
0x10	COUNT	7:0	COUNT[7:0]							
0x11		15:8	COUNT[15:8]							
0x12	Reserved									
0x13	Reserved									
0x14	PER	7:0	PER[7:0]							
0x15		15:8	PER[15:8]							
0x16	Reserved									
0x17	Reserved									
0x18	COMP0	7:0	COMP[7:0]							
0x19		15:8	COMP[15:8]							
0x1A	COMP1	7:0	COMP[7:0]							
0x1B		15:8	COMP[15:8]							

Table 21-3. MODE2 - Mode Register Summary

Offset	Name	Bit Pos.									
0x00	CTRL	7:0	MATCHCLR	CLKREP			MODE[1:0]		ENABLE	SWRST	
0x01		15:8					PRESCALER[3:0]				
0x02	READREQ	7:0			ADDR[5:0]						
0x03		15:8	RREQ	RCONT							
0x04	EVCTRL	7:0	PEREO7	PEREO6	PEREO5	PEREO4	PEREO3	PEREO2	PEREO1	PEREO0	
0x05		15:8	OVFEO							ALARMEO0	
0x06	INTENCLR	7:0	OVF	SYNCRDY						ALARM0	
0x07	INTENSET	7:0	OVF	SYNCRDY						ALARM0	
0x08	INTFLAG	7:0	OVF	SYNCRDY						ALARM0	
0x09	Reserved										
0x0A	STATUS	7:0	SYNCBUSY								
0x0B	DBGCTRL	7:0								DBGRUN	
0x0C	FREQCORR	7:0	SIGN	VALUE[6:0]							
0x0D ... 0x0F	Reserved										
0x10	CLOCK	7:0	MINUTE[1:0]		SECOND[5:0]						
0x11		15:8	HOUR[3:0]				MINUTE[5:2]				
0x12		23:16	MONTH[1:0]		DAY[4:0]						HOUR[4]
0x13		31:24	YEAR[5:0]						MONTH[3:2]		
0x14 ... 0x17	Reserved										
0x18	ALARM0	7:0	MINUTE[1:0]		SECOND[5:0]						
0x19		15:8	HOUR[3:0]				MINUTE[5:2]				
0x1A		23:16	MONTH[1:0]		DAY[4:0]						HOUR[4]

Writing a one to CTRL.SWRST will always take precedence, meaning that all other writes in the same write-operation will be discarded.

Due to synchronization, there is a delay from writing CTRL.SWRST until the reset is complete. CTRL.SWRST and STATUS.SYNCBUSY will both be cleared when the reset is complete.

This bit is not enable-protected.

Value	Description
0	There is no reset operation ongoing.
1	The reset operation is ongoing.

21.8.2 Control - MODE1

Name: CTRL

Offset: 0x00 [ID-00003035]

Reset: 0x0000

Property: Enable-Protected, Write-Protected, Write-Synchronized

Bit	15	14	13	12	11	10	9	8
					PRESCALER[3:0]			
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0
Bit	7	6	5	4	3	2	1	0
					MODE[1:0]		ENABLE	SWRST
Access					R/W	R/W	R/W	W
Reset					0	0	0	0

Bits 11:8 – PRESCALER[3:0]: Prescaler

These bits define the prescaling factor for the RTC clock source (GCLK_RTC) to generate the counter clock (CLK_RTC_CNT).

These bits are not synchronized.

PRESCALER[3:0]	Name	Description
0x0	DIV1	CLK_RTC_CNT = GCLK_RTC/1
0x1	DIV2	CLK_RTC_CNT = GCLK_RTC/2
0x2	DIV4	CLK_RTC_CNT = GCLK_RTC/4
0x3	DIV8	CLK_RTC_CNT = GCLK_RTC/8
0x4	DIV16	CLK_RTC_CNT = GCLK_RTC/16
0x5	DIV32	CLK_RTC_CNT = GCLK_RTC/32
0x6	DIV64	CLK_RTC_CNT = GCLK_RTC/64
0x7	DIV128	CLK_RTC_CNT = GCLK_RTC/128
0x8	DIV256	CLK_RTC_CNT = GCLK_RTC/256
0x9	DIV512	CLK_RTC_CNT = GCLK_RTC/512

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
							WAKEUPENx	WAKEUPENx
Access							R/W	R/W
Reset							0	0
Bit	15	14	13	12	11	10	9	8
	WAKEUPENx	WAKEUPENx	WAKEUPENx	WAKEUPENx	WAKEUPENx	WAKEUPENx	WAKEUPENx	WAKEUPENx
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	WAKEUPENx	WAKEUPENx	WAKEUPENx	WAKEUPENx	WAKEUPENx	WAKEUPENx	WAKEUPENx	WAKEUPENx
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 17,16,15,14,13,12,11,10,9,8,7,6,5,4,3,2,1,0 – WAKEUPENx : External Interrupt x Wake-up Enable [x=17..0]

This bit enables or disables wake-up from sleep modes when the EXTINTx pin matches the external interrupt sense configuration.

Value	Description
0	Wake-up from the EXTINTx pin is disabled.
1	Wake-up from the EXTINTx pin is enabled.

23.8.10 Configuration n

Name: CONFIG
Offset: 0x18 + n*0x04 [n=0..2]
Reset: 0x00000000
Property: Write-Protected

Some registers are enable-protected, meaning they can only be written when the module is disabled. Enable-protection is denoted by the "Enable-Protected" property in each individual register description.

24.8.1 Control A

Name: CTRLA
Offset: 0x00 [ID-00000b2c]
Reset: 0x0000
Property: PAC Write-Protection

Bit	15	14	13	12	11	10	9	8
	CMDEX[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	CMD[6:0]							
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bits 15:8 – CMDEX[7:0]: Command Execution

When this bit group is written to the key value 0xA5, the command written to CMD will be executed. If a value different from the key value is tried, the write will not be performed and the Programming Error bit in the Status register (STATUS.PROGE) will be set. PROGE is also set if a previously written command is not completed yet.

The key value must be written at the same time as CMD. If a command is issued through the APB bus on the same cycle as an AHB bus access, the AHB bus access will be given priority. The command will then be executed when the NVM block and the AHB bus are idle.

INTFLAG.READY must be '1' when the command is issued.

Bit 0 of the CMDEX bit group will read back as '1' until the command is issued.

Note: The NVM Address bit field in the Address register (ADDR.ADDR) uses 16-bit addressing.

Bits 6:0 – CMD[6:0]: Command

These bits define the command to be executed when the CMDEX key is written.

CMD[6:0]	Group Configuration	Description
0x00-0x01	-	Reserved
0x02	ER	Erase Row - Erases the row addressed by the ADDR register in the NVM main array.
0x03	-	Reserved
0x04	WP	Write Page - Writes the contents of the page buffer to the page addressed by the ADDR register.

PMUXE[3:0]	Name	Description
0x6	G	Peripheral function G selected
0x7	H	Peripheral function H selected
0x8	I	Peripheral function I selected
0x9-0xF	-	Reserved

25.8.13 Pin Configuration



Tip: The I/O pins are assembled in pin groups ("PORT groups") with up to 32 pins. Group 0 consists of the PA pins, group 1 is for the PB pins, etc. Each pin group has its own PORT registers. For example, the register address offset for the Data Direction (DIR) register for group 0 (PA00 to PA31) is 0x00, and the register address offset for the DIR register for group 1 (PB00 to PB31) is 0x80.

There are up to 32 Pin Configuration registers in each PORT group, one for each I/O line.

Name: PINCFG

Offset: 0x40 + n*0x01 [n=0..31]

Reset: 0x00

Property: PAC Write-Protection

Bit	7	6	5	4	3	2	1	0
		DRVSTR				PULLEN	INEN	PMUXEN
Access		R/W				R/W	R/W	R/W
Reset		0				0	0	0

Bit 6 – DRVSTR: Output Driver Strength Selection

This bit controls the output driver strength of an I/O pin configured as an output.

Value	Description
0	Pin drive strength is set to normal drive strength.
1	Pin drive strength is set to stronger drive strength.

Bit 2 – PULLEN: Pull Enable

This bit enables the internal pull-up or pull-down resistor of an I/O pin configured as an input.

Value	Description
0	Internal pull resistor is disabled, and the input is in a high-impedance configuration.
1	Internal pull resistor is enabled, and the input is driven to a defined logic level in the absence of external input.

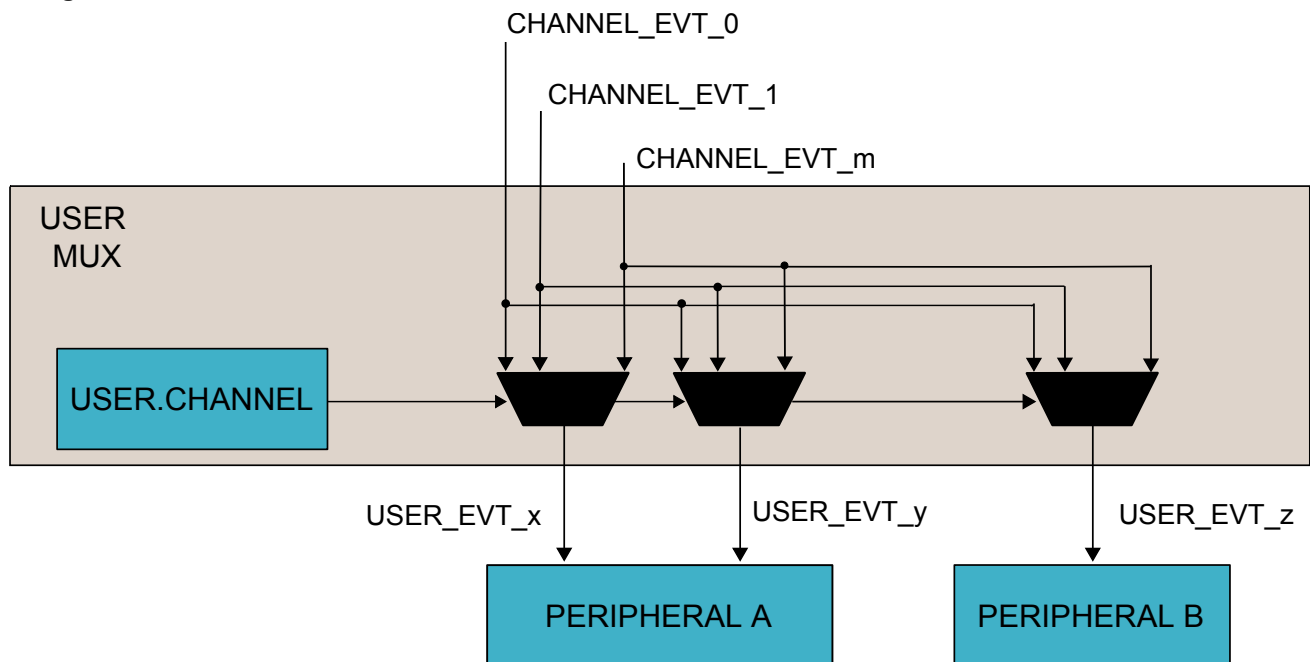
Bit 1 – INEN: Input Enable

This bit controls the input buffer of an I/O pin configured as either an input or output.

Writing a zero to this bit disables the input buffer completely, preventing read-back of the physical pin state when the pin is configured as either an input or output.

To configure a user multiplexer, the USER register must be written in a single 16-bit write. It is possible to read out the configuration of a user by first selecting the user by writing to USER.USER using an 8-bit write and then performing a read of the 16-bit USER register.

Figure 26-2. User MUX



26.6.2.4 Channel Setup

An event channel can select one event from a list of event generators. Depending on configuration, the selected event could be synchronized, resynchronized or asynchronously sent to the users. When synchronization or resynchronization is required, the channel includes an internal edge detector, allowing the Event System to generate internal events when rising, falling or both edges are detected on the selected event generator. An event channel is able to generate internal events for the specific software commands. All these configurations are available in the Channel register (CHANNEL).

To configure a channel, the Channel register must be written in a single 32-bit write. It is possible to read out the configuration of a channel by first selecting the channel by writing to CHANNEL.CHANNEL using a, 8-bit write, and then performing a read of the CHANNEL register.

26.6.2.5 Channel Path

There are three different ways to propagate the event provided by an event generator:

- Asynchronous path
- Synchronous path
- Resynchronized path

data bit is shifted in. And the Receive Complete Interrupt flag in the Interrupt Flag Status and Clear register (INTFLAG.RXC) will be set. The received data can be retrieved by reading DATA.

When the last character has been transmitted and there is no valid data in DATA, the Transmit Complete Interrupt flag in the Interrupt Flag Status and Clear register (INTFLAG.TXC) will be set. When the transaction is finished, the master must pull the \overline{SS} line high to notify the slave. If Master Slave Select Enable (CTRLB.MSSEN) is set to '0', the software must pull the \overline{SS} line high.

Slave

In slave mode (CTRLA.MODE=0x2), the SPI interface will remain inactive with the MISO line tri-stated as long as the \overline{SS} pin is pulled high. Software may update the contents of DATA at any time as long as the Data Register Empty flag in the Interrupt Status and Clear register (INTFLAG.DRE) is set.

When \overline{SS} is pulled low and SCK is running, the slave will sample and shift out data according to the transaction mode set. When the content of TxDATA has been loaded into the shift register, INTFLAG.DRE will be set, and new data can be written to DATA.

Similar to the master, the slave will receive one character for each character transmitted. A character will be transferred into the two-level receive buffer within the same clock cycle its last data bit is received. The received character can be retrieved from DATA when the Receive Complete interrupt flag (INTFLAG.RXC) is set.

When the master pulls the \overline{SS} line high, the transaction is done and the Transmit Complete Interrupt flag in the Interrupt Flag Status and Clear register (INTFLAG.TXC) will be set.

After DATA is written it takes up to three SCK clock cycles until the content of DATA is ready to be loaded into the shift register on the next character boundary. As a consequence, the first character transferred in a SPI transaction will not be the content of DATA. This can be avoided by using the preloading feature. Refer to [Preloading of the Slave Shift Register](#).

When transmitting several characters in one SPI transaction, the data has to be written into DATA register with at least three SCK clock cycles left in the current character transmission. If this criteria is not met, the previously received character will be transmitted.

Once the DATA register is empty, it takes three CLK_SERCOM_APB cycles for INTFLAG.DRE to be set.

29.6.2.7 Receiver Error Bit

The SPI receiver has one error bit: the Buffer Overflow bit (BUFOVF), which can be read from the Status register (STATUS). Once an error happens, the bit will stay set until it is cleared by writing '1' to it. The bit is also automatically cleared when the receiver is disabled.

There are two methods for buffer overflow notification, selected by the immediate buffer overflow notification bit in the Control A register (CTRLA.IBON):

If CTRLA.IBON=1, STATUS.BUFOVF is raised immediately upon buffer overflow. Software can then empty the receive FIFO by reading RxDATA until the receiver complete interrupt flag in the Interrupt Flag Status and Clear register (INTFLAG.RXC) goes low.

If CTRLA.IBON=0, the buffer overflow condition travels with data through the receive FIFO. After the received data is read, STATUS.BUFOVF and INTFLAG.ERROR will be set along with INTFLAG.RXC, and RxDATA will be zero.

29.6.3 Additional Features

29.6.3.1 Address Recognition

When the SPI is configured for slave operation (CTRLA.MODE=0x2) with address recognition (CTRLA.FORM is 0x2), the SERCOM address recognition logic is enabled: the first character in a transaction is checked for an address match.

Bit 1 – ENABLE: Enable

Due to synchronization, there is delay from writing CTRLA.ENABLE until the peripheral is enabled/disabled. The value written to CTRLA.ENABLE will read back immediately, and the ENABLE Synchronization Busy bit in the SYNCBUSY register (SYNCBUSY.ENABLE) will be set. SYNCBUSY.ENABLE will be cleared when the operation is complete.

This bit is not enable protected.

Value	Description
0	The peripheral is disabled.
1	The peripheral is enabled.

Bit 0 – SWRST: Software Reset

Writing a '0' to this bit has no effect.

Writing a '1' to this bit resets all registers in the TC, except DBGCTRL, to their initial state, and the TC will be disabled.

Writing a '1' to CTRLA.SWRST will always take precedence; all other writes in the same write-operation will be discarded.

Due to synchronization there is a delay from writing CTRLA.SWRST until the reset is complete. CTRLA.SWRST and SYNCBUSY.SWRST will both be cleared when the reset is complete.

This bit is not enable protected.

Value	Description
0	There is no reset operation ongoing.
1	The reset operation is ongoing.

32.8.2 Read Request

Name: READREQ

Offset: 0x02 [ID-00001cd8]

Reset: 0x0000

Bit	15	14	13	12	11	10	9	8
	RREQ	RCONT						
Access	W	R/W						
Reset	0	0						

Bit	7	6	5	4	3	2	1	0
				ADDR[4:0]				
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bit 15 – RREQ: Read Request

Writing a zero to this bit has no effect.

This bit will always read as zero.

Writing a one to this bit requests synchronization of the register pointed to by the Address bit group (READREQ.ADDR) and sets the Synchronization Busy bit in the Status register (STATUS.SYNCBUSY).

```

value = cycle * dithercy;
if ((MASK & value) + dithercy) > MASK)
    return 1;
return 0;
}

```

Dithering on Period

Writing DITHERCY in PER will lead to an average PWM period configured by the following formulas.

DITH4 mode:

$$PwmPeriod = \left(\frac{DITHERCY}{16} + PER \right) \left(\frac{1}{f_{GCLK_TCC}} \right)$$

Note: If DITH4 mode is enabled, the last 4 significant bits from PER/CCx or COUNT register correspond to the DITHERCY value, rest of the bits corresponds to PER/CCx or COUNT value.

DITH5 mode:

$$PwmPeriod = \left(\frac{DITHERCY}{32} + PER \right) \left(\frac{1}{f_{GCLK_TCC}} \right)$$

DITH6 mode:

$$PwmPeriod = \left(\frac{DITHERCY}{64} + PER \right) \left(\frac{1}{f_{GCLK_TCC}} \right)$$

Dithering on Pulse Width

Writing DITHERCY in CCx will lead to an average PWM pulse width configured by the following formula.

DITH4 mode:

$$PwmPulseWidth = \left(\frac{DITHERCY}{16} + CCx \right) \left(\frac{1}{f_{GCLK_TCC}} \right)$$

DITH5 mode:

$$PwmPulseWidth = \left(\frac{DITHERCY}{32} + CCx \right) \left(\frac{1}{f_{GCLK_TCC}} \right)$$

DITH6 mode:

$$PwmPulseWidth = \left(\frac{DITHERCY}{64} + CCx \right) \left(\frac{1}{f_{GCLK_TCC}} \right)$$

Note: The PWM period will remain static in this case.

33.6.3.4 Ramp Operations

Three ramp operation modes are supported. All of them require the timer/counter running in single-slope PWM generation. The ramp mode is selected by writing to the Ramp Mode bits in the Waveform Control register (WAVE.RAMP).

RAMP1 Operation

This is the default PWM operation, described in [Single-Slope PWM Generation](#).

RAMP2 Operation

These operation modes are dedicated for power factor correction (PFC), Half-Bridge and Push-Pull SMPS topologies, where two consecutive timer/counter cycles are interleaved, see [Figure 33-18](#). In cycle

Name: DBGCTRL
Offset: 0x1E [ID-00002e48]
Reset: 0x00
Property: PAC Write-Protection

Bit	7	6	5	4	3	2	1	0
						FDDBD		DBGRUN
Access						R/W		R/W
Reset						0		0

Bit 2 – FDDBD: Fault Detection on Debug Break Detection

This bit is not affected by software reset and should not be changed by software while the TCC is enabled.

By default this bit is zero, and the on-chip debug (OCD) fault protection is disabled. When this bit is written to '1', OCD break request from the OCD system will trigger non-recoverable fault. When this bit is set, OCD fault protection is enabled and OCD break request from the OCD system will trigger a non-recoverable fault.

Value	Description
0	No faults are generated when TCC is halted in debug mode.
1	A non recoverable fault is generated and FAULTD flag is set when TCC is halted in debug mode.

Bit 0 – DBGRUN: Debug Running State

This bit is not affected by software reset and should not be changed by software while the TCC is enabled.

Value	Description
0	The TCC is halted when the device is halted in debug mode.
1	The TCC continues normal operation when the device is halted in debug mode.

33.8.9 Event Control

Name: EVCTRL
Offset: 0x20 [ID-00002e48]
Reset: 0x00000000
Property: PAC Write-Protection, Enable-Protected

33.8.14 Counter Value

Note: Prior to any read access, this register must be synchronized by user by writing the according TCC Command value to the Control B Set register (CTRLBSET.CMD=READSYNC).

Name: COUNT

Offset: 0x34 [ID-00002e48]

Reset: 0x00000000

Property: PAC Write-Protection, Write-Synchronized, Read-Synchronized

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
	COUNT[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	COUNT[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	COUNT[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 23:0 – COUNT[23:0]: Counter Value

These bits hold the value of the counter register.

Note: When the TCC is configured as 16-bit timer/counter, the excess bits are read zero.

Note: This bit field occupies the MSB of the register, [23:m]. m is dependent on the Resolution bit in the Control A register (CTRLA.RESOLUTION):

CTRLA.RESOLUTION	Bits [23:m]
0x0 - NONE	23:0 (depicted)
0x1 - DITH4	23:4
0x2 - DITH5	23:5
0x3 - DITH6	23:6

33.8.15 Pattern

SPEED[1:0]	SPEED STATUS
0x0	Low-speed mode
0x1	Full-speed mode
0x2	Reserved
0x3	Reserved

34.8.2.4 Device Frame Number

Name: FNUM
Offset: 0x10 [ID-0000306e]
Reset: 0x0000
Property: Read only

Bit	15	14	13	12	11	10	9	8
	FNCERR		FNUM[10:5]					
Access	R/W		R/W	R/W	R/W	R/W	R/W	R/W
Reset	0		0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	FNUM[4:0]					MFNUM[2:0]		
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 15 – FNCERR: Frame Number CRC Error

This bit is cleared upon receiving a USB reset.

This bit is set when a corrupted frame number (or micro-frame number) is received.

This bit and the SOF (or MSOF) interrupt bit are updated at the same time.

Bits 13:3 – FNUM[10:0]: Frame Number

These bits are cleared upon receiving a USB reset.

These bits are updated with the frame number information as provided from the last SOF packet even if a corrupted SOF is received.

Bits 2:0 – MFNUM[2:0]: Micro Frame Number

These bits are cleared upon receiving a USB reset or at the beginning of each Start-of-Frame (SOF interrupt).

These bits are updated with the micro-frame number information as provided from the last MSOF packet even if a corrupted MSOF is received.

34.8.2.5 Device Interrupt Enable Clear

This register allows the user to disable an interrupt without doing a read-modify-write operation. Changes in this register will also be reflected in the Interrupt Enable Set (INTENSET) register.

MUXPOS[4:0]	Group configuration	Description
0x03	PIN3	ADC AIN3 pin
0x04	PIN4	ADC AIN4 pin
0x05	PIN5	ADC AIN5 pin
0x06	PIN6	ADC AIN6 pin
0x07	PIN7	ADC AIN7 pin
0x08	PIN8	ADC AIN8 pin
0x09	PIN9	ADC AIN9 pin
0x0A	PIN10	ADC AIN10 pin
0x0B	PIN11	ADC AIN11 pin
0x0C	PIN12	ADC AIN12 pin
0x0D	PIN13	ADC AIN13 pin
0x0E	PIN14	ADC AIN14 pin
0x0F	PIN15	ADC AIN15 pin
0x10	PIN16	ADC AIN16 pin
0x11	PIN17	ADC AIN17 pin
0x12	PIN18	ADC AIN18 pin
0x13	PIN19	ADC AIN19 pin
0x14-0x17		Reserved
0x18	TEMP	Temperature reference
0x19	BANDGAP	Bandgap voltage
0x1A	SCALED COREVCC	1/4 scaled core supply
0x1B	SCALED IOVCC	1/4 scaled I/O supply
0x1C	DAC	DAC output
0x1D-0x1F		Reserved

35.8.9 Event Control

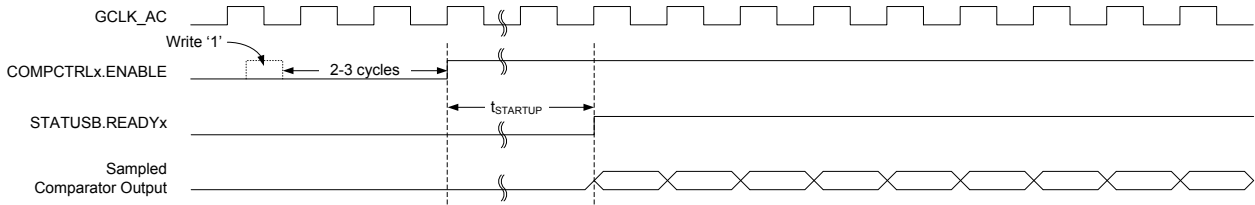
Name: EVCTRL

Offset: 0x14 [ID-00002049]

Reset: 0x00

Property: Write-Protected

Figure 36-2. Continuous Measurement Example



For low-power operation, comparisons can be performed during sleep modes without a clock. The comparator is enabled continuously, and changes of the comparator state are detected asynchronously. When a toggle occurs, the Power Manager will start CLK_AC_DIG to register the appropriate peripheral events and interrupts. The CLK_AC_DIG clock is then disabled again automatically, unless configured to wake up the system from sleep.

Related Links

[Electrical Characteristics](#)

Single-Shot

Single-shot operation is selected by writing COMPCTRLx.SINGLE to '1'. During single-shot operation, the comparator is normally idle. The user starts a single comparison by writing '1' to the respective Start Comparison bit in the write-only Control B register (CTRLB.STARTx). The comparator is enabled, and after the start-up time has passed, a single comparison is done and STATUSA is updated. Appropriate peripheral events and interrupts are also generated. No new comparisons will be performed.

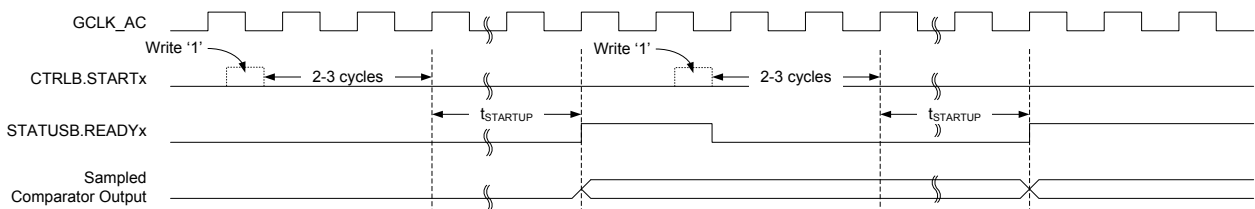
Writing '1' to CTRLB.STARTx also clears the Comparator x Ready bit in the Status B register (STATUSB.READYx). STATUSB.READYx is set automatically by hardware when the single comparison has completed.

To remove the need for polling, an additional means of starting the comparison is also available. A read of the Status C register (STATUSC) will start a comparison on all comparators currently configured for single-shot operation. The read will stall the bus until all enabled comparators are ready. If a comparator is already busy with a comparison, the read will stall until the current comparison is complete, and a new comparison will not be started.

A single-shot measurement can also be triggered by the Event System. Setting the Comparator x Event Input bit in the Event Control Register (EVCTRL.COMPEIx) enables triggering on incoming peripheral events. Each comparator can be triggered independently by separate events. Event-triggered operation is similar to user-triggered operation; the difference is that a peripheral event from another hardware module causes the hardware to automatically start the comparison and clear STATUSB.READYx.

To detect an edge of the comparator output in single-shot operation for the purpose of interrupts, the result of the current measurement is compared with the result of the previous measurement (one sampling period earlier). An example of single-shot operation is shown in the figure below.

Figure 36-3. Single-Shot Example



For low-power operation, event-triggered measurements can be performed during sleep modes. When the event occurs, the Power Manager will start CLK_AC_DIG. The comparator is enabled, and after the startup time has passed, a comparison is done and appropriate peripheral events and interrupts are also

Figure 36-6. Continuous Mode Filtering

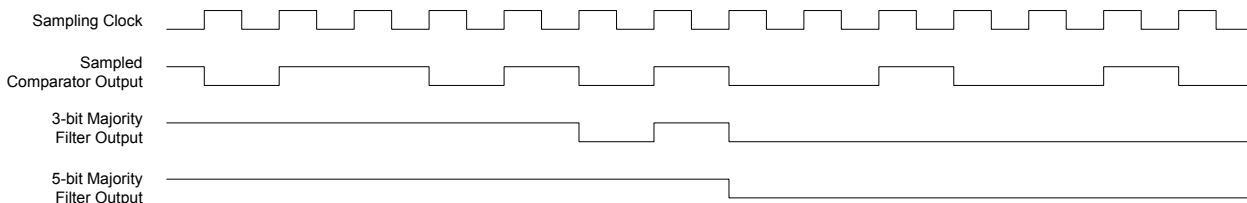
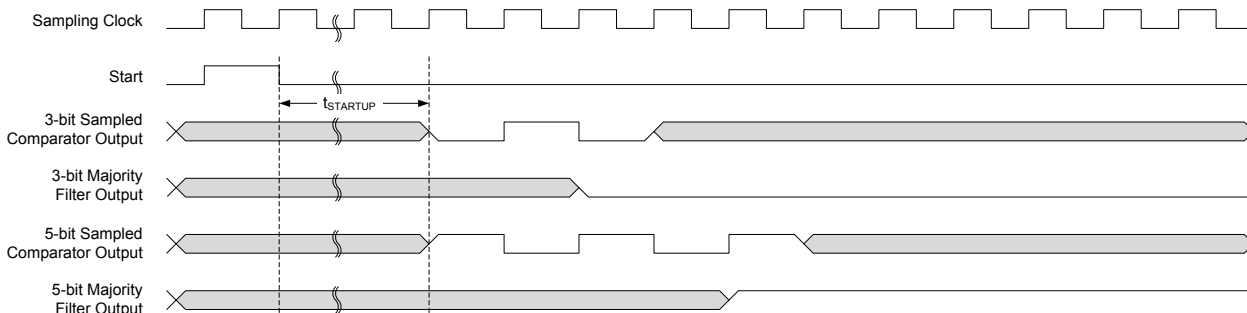


Figure 36-7. Single-Shot Filtering



During sleep modes, filtering is supported only for single-shot measurements. Filtering must be disabled if continuous measurements will be done during sleep modes, or the resulting interrupt/event may be generated incorrectly.

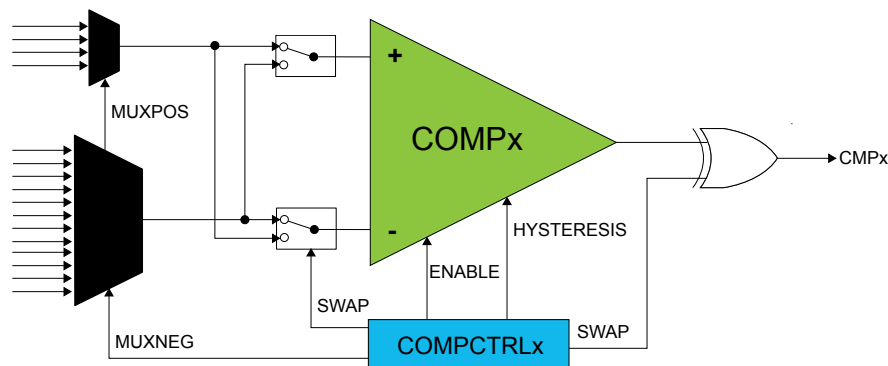
36.6.10 Comparator Output

The output of each comparator can be routed to an I/O pin by setting the Output bit group in the Comparator Control x register (COMPCTRLx.OUT). This allows the comparator to be used by external circuitry. Either the raw, non-synchronized output of the comparator or the CLK_AC-synchronized version, including filtering, can be used as the I/O signal source. The output appears on the corresponding CMP[x] pin.

36.6.11 Offset Compensation

The Swap bit in the Comparator Control registers (COMPCTRLx.SWAP) controls switching of the input signals to a comparator's positive and negative terminals. When the comparator terminals are swapped, the output signal from the comparator is also inverted, as shown in [Figure 36-8](#). This allows the user to measure or compensate for the comparator input offset voltage. As part of the input selection, COMPCTRLx.SWAP can be changed only while the comparator is disabled.

Figure 36-8. Input Swapping for Offset Compensation



36.6.12 Interrupts

The AC has the following interrupt sources:

Parameter	Conditions	Symbol	Min.	Typ.	Max.	Unit
	$C_L = 20\text{pF}$, XOSC.GAIN = 1, AGC off					
	$f = 4\text{MHz}$, $C_L = 20\text{pF}$, XOSC.GAIN = 1, AGC on		-	102	219	
	$f = 8\text{MHz}$, $C_L = 20\text{pF}$, XOSC.GAIN = 2, AGC off		-	243	380	
Current Consumption	$f = 8\text{MHz}$, $C_L = 20\text{pF}$, XOSC.GAIN = 2, AGC on		-	166	299	μA
	$f = 16\text{MHz}$, $C_L = 20\text{pF}$, XOSC.GAIN = 3, AGC off		-	493	685	
	$f = 16\text{MHz}$, $C_L = 20\text{pF}$, XOSC.GAIN = 3, AGC on		-	293	480	
	$f = 32\text{MHz}$, $C_L = 18\text{pF}$, XOSC.GAIN = 4, AGC off		-	1343	1975	
	$f = 32\text{MHz}$, $C_L = 18\text{pF}$, XOSC.GAIN = 4, AGC on		-	555	776	