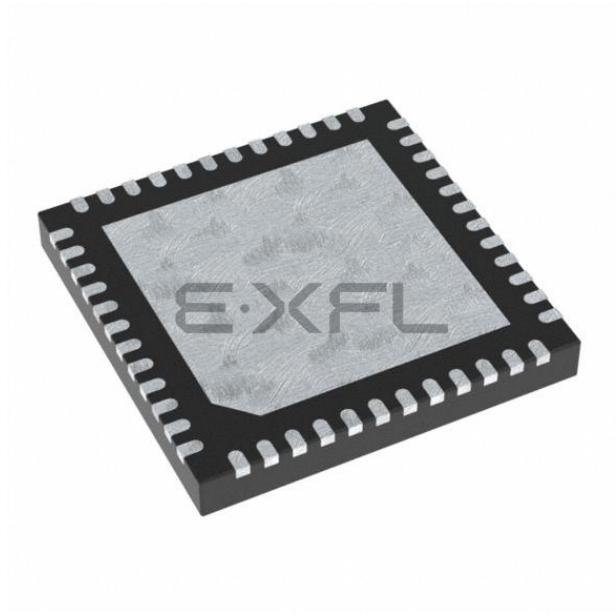

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I²C, SCI, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	38
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.63V
Data Converters	A/D 14x12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	48-QFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsamda1g15b-mbt

3.1.2 SAM DA1G

Ordering Code	Flash (Bytes)	SRAM (Bytes)	Package	Carrier Type	Temp.Grade	PTC, USB, I^2S
ATSAMDA1 G14A-ABT(1)	16K	4K	TQFP48	Tape and Reel	-40°C to +105°C	Yes
ATSAMDA1 G14A-MBT(1)	16K	4K	QFN48	Tape and Reel	-40°C to +105°C	Yes
ATSAMDA1 G15A-ABT(1)	32K	4K	TQFP48	Tape and Reel	-40°C to +105°C	Yes
ATSAMDA1 G15A-MBT(1)	32K	4K	QFN48	Tape and Reel	-40°C to +105°C	Yes
ATSAMDA1 G16A-ABT(1)	64K	8K	TQFP48	Tape and Reel	-40°C to +105°C	Yes
ATSAMDA1 G16A-MBT(1)	64K	8K	QFN48	Tape and Reel	-40°C to +105°C	Yes

1. Contact your local sales representative for availability.

3.1.3 SAM DA1J

Ordering Code	Flash (Bytes)	SRAM (Bytes)	Package	Carrier Type	Temp.Grade	PTC, USB, I^2S
ATSAMDA1J 14A-ABT(1)	16K	4K	TQFP64	Tape and Reel	-40°C to +105°C	Yes
ATSAMDA1J 15A-ABT(1)	32K	4K	TQFP64	Tape and Reel	-40°C to +105°C	Yes
ATSAMDA1J 16A-ABT(1)	64K	8K	TQFP64	Tape and Reel	-40°C to +105°C	Yes

1. Contact your local sales representative for availability.

3.2 Device Variant B

3.2.1 SAM DA1E

Ordering Code	Flash (Bytes)	SRAM (Bytes)	Package	Carrier Type	Temp.Grade	PTC, USB, I^2S
ATSAMDA1E 14B-ABT(1)	16K	4K	TQFP32	Tape and Reel	-40°C to +105°C	Yes
ATSAMDA1E 14B-MBT(1)	16K	4K	QFN32	Tape and Reel	-40°C to +105°C	Yes
ATSAMDA1E 15B-ABT(1)	32K	4K	TQFP32	Tape and Reel	-40°C to +105°C	Yes

Ordering Code	Flash (Bytes)	SRAM (Bytes)	Package	Carrier Type	Temp.Grade	PTC, USB, I²S
ATSAMDA1E 15B-MBT(1)	32K	4K	QFN32	Tape and Reel	-40°C to +105°C	Yes
ATSAMDA1E 16B-ABT(1)	64K	8K	TQFP32	Tape and Reel	-40°C to +105°C	Yes
ATSAMDA1E 16B-MBT(1)	64K	8K	QFN32	Tape and Reel	-40°C to +105°C	Yes

1. Contact your local sales representative for availability.

3.2.2 SAM DA1G

Ordering Code	Flash (Bytes)	SRAM (Bytes)	Package	Carrier Type	Temp.Grade	PTC, USB, I²S
ATSAMDA1 G14B-ABT(1)	16K	4K	TQFP48	Tape and Reel	-40°C to +105°C	Yes
ATSAMDA1 G14B-MBT(1)	16K	4K	QFN48	Tape and Reel	-40°C to +105°C	Yes
ATSAMDA1 G15B-ABT(1)	32K	4K	TQFP48	Tape and Reel	-40°C to +105°C	Yes
ATSAMDA1 G15B-MBT(1)	32K	4K	QFN48	Tape and Reel	-40°C to +105°C	Yes
ATSAMDA1 G16B-ABT(1)	64K	8K	TQFP48	Tape and Reel	-40°C to +105°C	Yes
ATSAMDA1 G16B-MBT(1)	64K	8K	QFN48	Tape and Reel	-40°C to +105°C	Yes

1. Contact your local sales representative for availability.

3.2.3 SAM DA1J

Ordering Code	Flash (Bytes)	SRAM (Bytes)	Package	Carrier Type	Temp.Grade	PTC, USB, I²S
ATSAMDA1J 14B-ABT(1)	16K	4K	TQFP64	Tape and Reel	-40°C to +105°C	Yes
ATSAMDA1J 15B-ABT(1)	32K	4K	TQFP64	Tape and Reel	-40°C to +105°C	Yes
ATSAMDA1J 16B-ABT(1)	64K	8K	TQFP64	Tape and Reel	-40°C to +105°C	Yes

1. Contact your local sales representative for availability.

Related Links

PM – Power Manager

13.6.2 Register Description

Atomic 8-, 16- and 32-bit accesses are supported. In addition, the 8-bit quarters and 16-bit halves of a 32-bit register, and the 8-bit halves of a 16-bit register can be accessed directly. Refer to the Product Mapping for PAC locations.

13.6.2.1 PAC0 Register Description

Write Protect Clear

Name: WPCLR
Offset: 0x00 [ID-00000a18]
Reset: 0x000000
Property: –

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
		EIC	RTC	WDT	GCLK	SYSCTRL	PM	
Access		R/W	R/W	R/W	R/W	R/W	R/W	
Reset		0	0	0	0	0	0	

Bit 6 – EIC
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 5 – RTC
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 5 – USB
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 4 – DMAC:
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 3 – PORT
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 2 – NVMCTRL
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 1 – DSU
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

13.6.2.3 PAC2 Register Description

Write Protect Clear

Bit	31	30	29	28	27	26	25	24
	ADDR[29:22]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	ADDR[21:14]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	ADDR[13:6]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	ADDR[5:0]						AMOD[1:0]	
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:2 – ADDR[29:0]: Address
Initial word start address needed for memory operations.

Bits 1:0 – AMOD[1:0]: Access Mode
The functionality of these bits is dependent on the operation mode.

Bit description when operating CRC32: refer to 32-bit Cyclic Redundancy Check CRC32

Bit description when testing onboard memories (MBIST): refer to Testing of On-Board Memories MBIST

15.13.5 Length

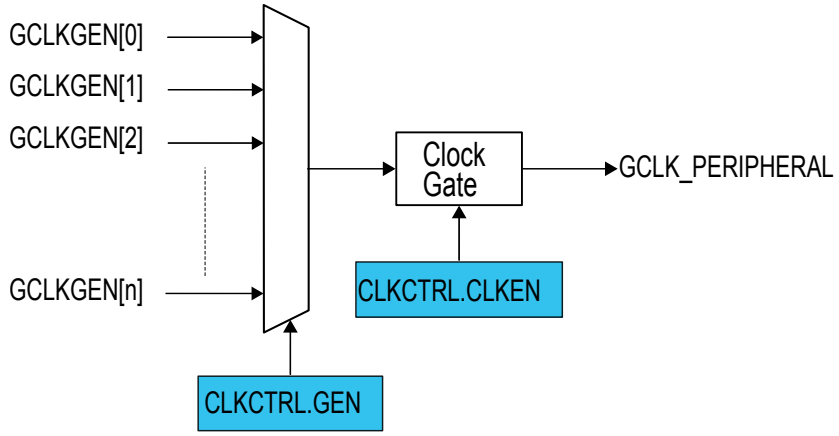
Name: LENGTH
Offset: 0x0008 [ID-00001c14]
Reset: 0x00000000
Property: PAC Write-Protection

according to the Output Off Value bit. If the Output Off Value bit in GENCTRL (GENCTRL.OOV) is zero, the output clock will be low when generic clock generator is turned off. If GENCTRL.OOV=1, the output clock will be high when Generator is turned off.

In standby mode, if the clock is output (GENCTRL.OE=1), the clock on the GCLK_IO pin is frozen to the OOV value if the Run In Standby bit in GENCTRL (GENCTRL.RUNSTDBY) is zero. If GENCTRL.RUNSTDBY=1, the GCLKGEN clock is kept running and output to GCLK_IO.

17.6.3 Generic Clock

Figure 17-4. Generic Clock Multiplexer



17.6.3.1 Enabling a Generic Clock

Before a generic clock is enabled, one of the Generators must be selected as the source for the generic clock by writing to CLKCTRL.GEN. The clock source selection is individually set for each generic clock.

When a Generator has been selected, the generic clock is enabled by setting the Clock Enable bit in CLKCTRL (CLKCTRL.CLKEN=1). The CLKCTRL.CLKEN bit must be synchronized to the generic clock domain. CLKCTRL.CLKEN will continue to read as its previous state until the synchronization is complete.

17.6.3.2 Disabling a Generic Clock

A generic clock is disabled by writing CLKCTRL.CLKEN=0. The SYNCBUSY bit will be cleared when this write-synchronization is complete. CLKCTRL.CLKEN will stay in its previous state until the synchronization is complete. The generic clock is gated when disabled.

17.6.3.3 Selecting a Clock Source for the Generic Clock

When changing a generic clock source by writing to CLKCTRL.GEN, the generic clock must be disabled before being re-enabled it with the new clock source setting. This prevents glitches during the transition:

1. Write CLKCTRL.CLKEN=0
2. Assert that CLKCTRL.CLKEN reads '0'
3. Change the source of the generic clock by writing CLKCTRL.GEN
4. Re-enable the generic clock by writing CLKCTRL.CLKEN=1

17.6.3.4 Configuration Lock

The generic clock configuration can be locked for further write accesses by setting the Write Lock bit in the CLKCTRL register (CLKCTRL.WRTLOCK). All writes to the CLKCTRL register will be ignored. It can only be unlocked by a Power Reset.

The Generator source of a locked generic clock are also locked, too: The corresponding GENCTRL and GENDIV are locked, and can be unlocked only by a Power Reset.

19.7 Register Summary

Offset	Name	Bit Pos.								
0x00	INTENCLR	7:0	DFLLLCKC	DFLLLCKF	DFLLOOB	DFLLRDY	OSC8MRDY	OSC32KRDY	XOSC32KRDY	XOSCRDY
0x01		15:8	DPLLLCKR				B33SRDY	BOD33DET	BOD33RDY	DFLLRCS
0x02		23:16							DPLLLTO	DPLLLCKF
0x03		31:24								
0x04	INTENSET	7:0	DFLLLCKC	DFLLLCKF	DFLLOOB	DFLLRDY	OSC8MRDY	OSC32KRDY	XOSC32KRDY	XOSCRDY
0x05		15:8	DPLLLCKR				B33SRDY	BOD33DET	BOD33RDY	DFLLRCS
0x06		23:16							DPLLLTO	DPLLLCKF
0x07		31:24								
0x08	INTFLAG	7:0	DFLLLCKC	DFLLLCKF	DFLLOOB	DFLLRDY	OSC8MRDY	OSC32KRDY	XOSC32KRDY	XOSCRDY
0x09		15:8	DPLLLCKR				B33SRDY	BOD33DET	BOD33RDY	DFLLRCS
0x0A		23:16							DPLLLTO	DPLLLCKF
0x0B		31:24								
0x0C	PCLKSR	7:0	DFLLLCKC	DFLLLCKF	DFLLOOB	DFLLRDY	OSC8MRDY	OSC32KRDY	XOSC32KRDY	XOSCRDY
0x0D		15:8	DPLLLCKR				B33SRDY	BOD33DET	BOD33RDY	DFLLRCS
0x0E		23:16							DPLLLTO	DPLLLCKF
0x0F		31:24								
0x10	XOSC	7:0	ONDEMAND	RUNSTDBY				XTALEN	ENABLE	
0x11		15:8	STARTUP[3:0]				AMPGC	GAIN[2:0]		
0x12 ... 0x13	Reserved									
0x14	XOSC32K	7:0	ONDEMAND	RUNSTDBY	AAMPEN		EN32K	XTALEN	ENABLE	
0x15		15:8				WRTLOCK		STARTUP[2:0]		
0x16 ... 0x17	Reserved									
0x18	OSC32K	7:0	ONDEMAND	RUNSTDBY				EN32K	ENABLE	
0x19		15:8				WRTLOCK		STARTUP[2:0]		
0x1A		23:16		CALIB[6:0]						
0x1B		31:24								
0x1C	OSCULP32K	7:0	WRTLOCK			CALIB[4:0]				
0x1D ... 0x1F	Reserved									
0x20	OSC8M	7:0	ONDEMAND	RUNSTDBY					ENABLE	
0x21		15:8							PRESC[1:0]	
0x22		23:16	CALIB[7:0]							
0x23		31:24	FRANGE[1:0]				CALIB[11:8]			
0x24	DFLLCTRL	7:0	ONDEMAND	RUNSTDBY	USBCRM	LLAW	STABLE	MODE	ENABLE	
0x25		15:8					WAITLOCK	BPLCKC	QLDIS	CCDIS
0x26	Reserved									

Bit	31	30	29	28	27	26	25	24
	FRANGE[1:0]				CALIB[11:8]			
Access	R/W	R/W			R/W	R/W	R/W	R/W
Reset	x	x			0	0	0	0

Bit	23	22	21	20	19	18	17	16
	CALIB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	x

Bit	15	14	13	12	11	10	9	8
							PRESC[1:0]	
Access							R/W	R/W
Reset							1	1

Bit	7	6	5	4	3	2	1	0
	ONDEMAND	RUNSTDBY					ENABLE	
Access	R/W	R/W					R/W	
Reset	1	0					1	

Bits 31:30 – FRANGE[1:0]: Oscillator Frequency Range
These bits control the oscillator frequency range according to the table below. These bits are loaded from Flash Calibration at startup.

FRANGE[1:0]	Description
0x0	4 to 6MHz
0x1	6 to 8MHz
0x2	8 to 11MHz
0x3	11 to 15MHz

Bits 27:16 – CALIB[11:0]: Oscillator Calibration
These bits control the oscillator calibration. The calibration field is split in two:

CALIB[11:6] is for temperature calibration

CALIB[5:0] is for overall process calibration

These bits are loaded from Flash Calibration at startup.

Bits 9:8 – PRESC[1:0]: Oscillator Prescaler
These bits select the oscillator prescaler factor setting according to the table below.

PRESC[1:0]	Description
0x0	1
0x1	2
0x2	4
0x3	8

Value	Description
0	The DPLL is always on when enabled.
1	The DPLL is activated only when a peripheral request the DPLL as a source clock. The DPLLCTRLA.ENABLE bit must be one to validate that operation, otherwise the peripheral request has no effect.

Bit 6 – RUNSTDBY: Run in Standby

Value	Description
0	The DPLL is disabled in standby sleep mode.
1	The DPLL is not stopped in standby sleep mode.

Bit 1 – ENABLE: DPLL Enable
The software operation of enabling or disabling the DPLL takes a few clock cycles, so check the DPLLSTATUS.ENABLE status bit to identify when the DPLL is successfully activated or disabled.

Value	Description
0	The DPLL is disabled.
1	The DPLL is enabled.

19.8.18 DPLL Ratio Control

Name: DPLLRATIO
Offset: 0x48 [ID-00003d5d]
Reset: 0x00000000
Property: Write-Protected

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
					LDRFRAC[3:0]			
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit	15	14	13	12	11	10	9	8
					LDR[11:8]			
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit	7	6	5	4	3	2	1	0
	LDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 19:16 – LDRFRAC[3:0]: Loop Divider Ratio Fractional Part
Write this field with the fractional part of the frequency multiplier.

20.6.5 Synchronization

Due to asynchronicity between the main clock domain and the peripheral clock domains, some registers need to be synchronized when written or read.

When executing an operation that requires synchronization, the Synchronization Busy bit in the Status register (STATUS.SYNCBUSY) will be set immediately, and cleared when synchronization is complete. The Synchronization Ready interrupt can be used to signal when synchronization is complete. This can be accessed via the Synchronization Ready Interrupt Flag in the Interrupt Flag Status and Clear register (INTFLAG.SYNCRDY).

If an operation that requires synchronization is executed while STATUS.SYNCBUSY='1', the bus will be stalled. All operations will complete successfully, but the CPU will be stalled and interrupts will be pending as long as the bus is stalled.

The following registers are synchronized when written:

- Control register (CTRL)
- Clear register (CLEAR)

Required write-synchronization is denoted by the "Write-Synchronized" property in the register description.

Related Links

Register Synchronization

20.7 Register Summary

Register summary

Offset	Name	Bit Pos.								
0x0	CTRL	7:0	ALWAYSON					WEN	ENABLE	
0x1	CONFIG	7:0	WINDOW[3:0]				PER[3:0]			
0x2	EWCTRL	7:0					EWOFFSET[3:0]			
0x3	Reserved									
0x4	INTENCLR	7:0								EW
0x5	INTENSET	7:0								EW
0x6	INTFLAG	7:0								EW
0x7	STATUS	7:0	SYNCBUSY							
0x8	CLEAR	7:0	CLEAR[7:0]							

20.8 Register Description

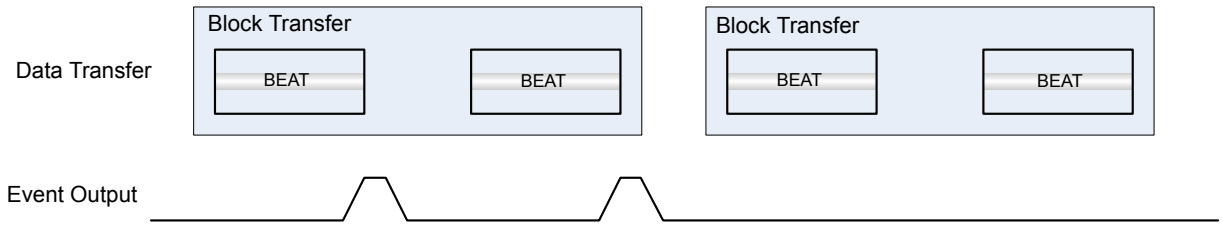
Registers can be 8, 16, or 32 bits wide. Atomic 8-, 16-, and 32-bit accesses are supported. In addition, the 8-bit quarters and 16-bit halves of a 32-bit register, and the 8-bit halves of a 16-bit register can be accessed directly.

Some registers require synchronization when read and/or written. Synchronization is denoted by the "Read-Synchronized" and/or "Write-Synchronized" property in each individual register description.

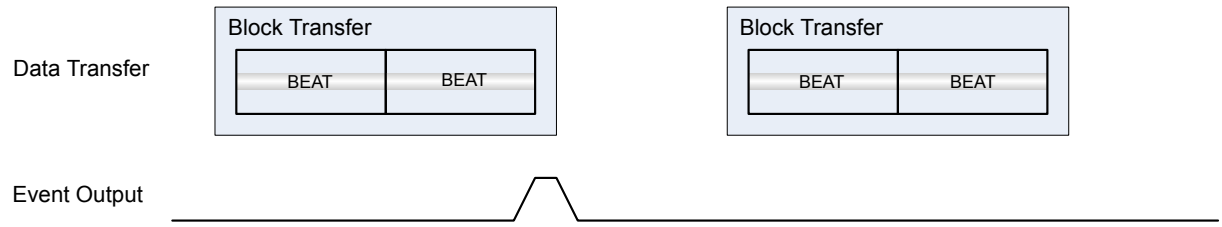
Some registers are enable-protected, meaning they can only be written when the module is disabled. Enable-protection is denoted by the "Enable-Protected" property in each individual register description.

Figure 22-15. Event Output Generation

Beat Event Output



Block Event Output



22.6.3.6 Aborting Transfers

Transfers on any channel can be aborted gracefully by software by disabling the corresponding DMA channel. It is also possible to abort all ongoing or pending transfers by disabling the DMAC.

When a DMA channel disable request or DMAC disable request is detected:

- Ongoing transfers of the active channel will be disabled when the ongoing beat transfer is completed and the write-back memory section is updated. This prevents transfer corruption before the channel is disabled.
- All other enabled channels will be disabled in the next clock cycle.

The corresponding Channel Enable bit in the Channel Control A register is cleared (CHCTRLA.ENABLE=0) when the channel is disabled.

The corresponding DMAC Enable bit in the Control register is cleared (CTRL.DMAENABLE=0) when the entire DMAC module is disabled.

22.6.3.7 CRC Operation

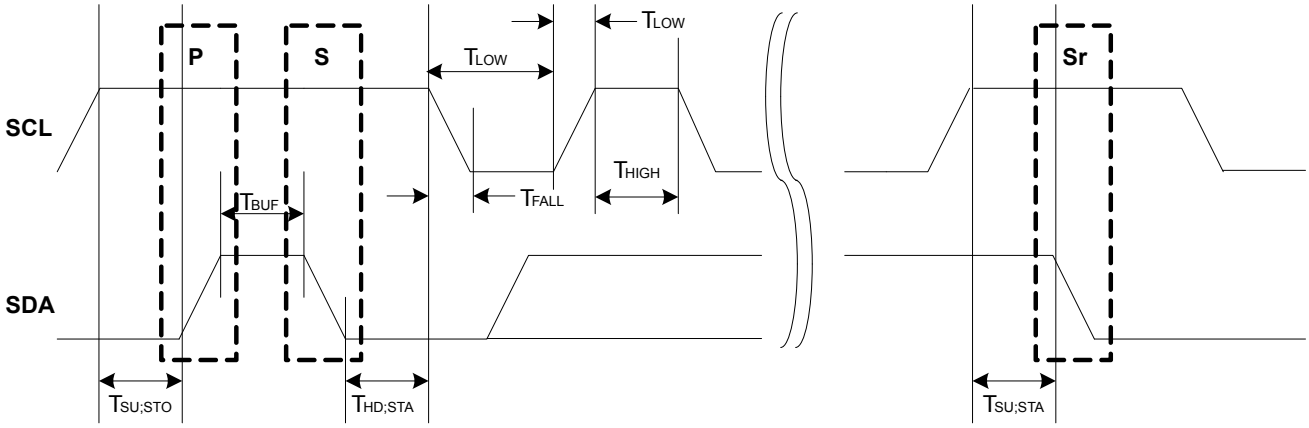
A cyclic redundancy check (CRC) is an error detection technique used to find errors in data. It is commonly used to determine whether the data during a transmission, or data present in data and program memories has been corrupted or not. A CRC takes a data stream or a block of data as input and generates a 16- or 32-bit output that can be appended to the data and used as a checksum.

When the data is received, the device or application repeats the calculation: If the new CRC result does not match the one calculated earlier, the block contains a data error. The application will then detect this and may take a corrective action, such as requesting the data to be sent again or simply not using the incorrect data.

The CRC engine in DMAC supports two commonly used CRC polynomials: CRC-16 (CRC-CCITT) and CRC-32 (IEEE 802.3). Typically, applying CRC-n (CRC-16 or CRC-32) to a data block of arbitrary length will detect any single alteration that is ≤n bits in length, and will detect the fraction 1-2-n of all longer error bursts.

Value	Name	Description
0x00	DISABLE	Only software/event triggers
0x01	SERCOM0 RX	SERCOM0 RX Trigger
0x02	SERCOM0 TX	SERCOM0 TX Trigger
0x03	SERCOM1 RX	SERCOM1 RX Trigger
0x04	SERCOM1 TX	SERCOM1 TX Trigger
0x05	SERCOM2 RX	SERCOM2 RX Trigger
0x06	SERCOM2 TX	SERCOM2 TX Trigger
0x07	SERCOM3 RX	SERCOM3 RX Trigger
0x08	SERCOM3 TX	SERCOM3 TX Trigger
0x09	SERCOM4 RX	SERCOM4 RX Trigger
0x0A	SERCOM4 TX	SERCOM4 TX Trigger
0x0B	SERCOM5 RX	SERCOM5 RX Trigger
0x0C	SERCOM5 TX	SERCOM5 TX Trigger
0x0D	TCC0 OVF	TCC0 Overflow Trigger
0x0E	TCC0 MC0	TCC0 Match/Compare 0 Trigger
0x0F	TCC0 MC1	TCC0 Match/Compare 1 Trigger
0x10	TCC0 MC2	TCC0 Match/Compare 2 Trigger
0x11	TCC0 MC3	TCC0 Match/Compare 3 Trigger
0x12	TCC1 OVF	TCC1 Overflow Trigger
0x13	TCC1 MC0	TCC1 Match/Compare 0 Trigger
0x14	TCC1 MC1	TCC1 Match/Compare 1 Trigger
0x15	TCC2 OVF	TCC2 Overflow Trigger
0x16	TCC2 MC0	TCC2 Match/Compare 0 Trigger
0x17	TCC2 MC1	TCC2 Match/Compare 1 Trigger
0x18	TC0 OVF	TC0 Overflow Trigger
0x19	TC0 MC0	TC0 Match/Compare 0 Trigger
0x1A	TC0 MC1	TC0 Match/Compare 1 Trigger
0x1B	TC1 OVF	TC1 Overflow Trigger
0x1C	TC1 MC0	TC1 Match/Compare 0 Trigger
0x1D	TC1 MC1	TC1 Match/Compare 1 Trigger
0x1E	TC2 OVF	TC2 Overflow Trigger
0x1F	TC2 MC0	TC2 Match/Compare 0 Trigger
0x20	TC2 MC1	TC2 Match/Compare 1 Trigger
0x21	TC3 OVF	TC3 Overflow Trigger
0x22	TC3 MC0	TC3 Match/Compare 0 Trigger
0x23	TC3 MC1	TC3 Match/Compare 1 Trigger
0x24	TC4 OVF	TC4 Overflow Trigger
0x25	TC4 MC0	TC4 Match/Compare 0 Trigger
0x26	TC4 MC1	TC4 Match/Compare 1 Trigger
0x27	ADC RESRDY	ADC Result Ready Trigger
0x28	DAC EMPTY	DAC Empty Trigger
0x29	I2S RX 0	I2S RX 0 Trigger
0x2A	I2S RX 1	I2S RX 1 Trigger
0x2B	I2S TX 0	I2S TX 0 Trigger
0x2C	I2S TX 0	I2S TX 1 Trigger

Figure 30-6. SCL Timing



The following parameters are timed using the SCL low time period T_{LOW}. This comes from the Master Baud Rate Low bit group in the Baud Rate register (BAUD.BAUDLOW). When BAUD.BAUDLOW=0, or the Master Baud Rate bit group in the Baud Rate register (BAUD.BAUD) determines it.

- T_{LOW} – Low period of SCL clock
- $T_{SU;STO}$ – Set-up time for stop condition
- T_{BUF} – Bus free time between stop and start conditions
- $T_{HD;STA}$ – Hold time (repeated) start condition
- $T_{SU;STA}$ – Set-up time for repeated start condition
- T_{HIGH} is timed using the SCL high time count from BAUD.BAUD
- T_{RISE} is determined by the bus impedance; for internal pull-ups. Refer to *Electrical Characteristics*.
- T_{FALL} is determined by the open-drain current limit and bus impedance; can typically be regarded as zero. Refer to *Electrical Characteristics* for details.

The SCL frequency is given by:

$$f_{\mathrm{SCL}} = \frac{1}{T_{\mathrm{LOW}} + T_{\mathrm{HIGH}} + T_{\mathrm{RISE}}}$$

When BAUD.BAUDLOW is zero, the BAUD.BAUD value is used to time both SCL high and SCL low. In this case the following formula will give the SCL frequency:

$$f_{\mathrm{SCL}} = \frac{f_{\mathrm{GCLK}}}{10 + 2BAUD + f_{\mathrm{GCLK}} \cdot T_{\mathrm{RISE}}}$$

When BAUD.BAUDLOW is non-zero, the following formula determines the SCL frequency:

$$f_{\mathrm{SCL}} = \frac{f_{\mathrm{GCLK}}}{10 + BAUD + BAUDLOW + f_{\mathrm{GCLK}} \cdot T_{\mathrm{RISE}}}$$

The following formulas can determine the SCL T_{LOW} and T_{HIGH} times:

$$T_{\mathrm{LOW}} = \frac{BAUDLOW + 5}{f_{\mathrm{GCLK}}}$$

$$T_{\mathrm{HIGH}} = \frac{BAUD + 5}{f_{\mathrm{GCLK}}}$$

Note: The I²C standard *Fm+* (Fast-mode plus) requires a nominal high to low SCL ratio of 1:2, and BAUD should be set accordingly. At a minimum, BAUD.BAUD and/or BAUD.BAUDLOW must be non-zero.

Condition	Request		
	DMA	Interrupt	Event
Stop received (SB)		Yes	
Error (ERROR)		Yes	

30.6.4.1 DMA Operation

Smart mode must be enabled for DMA operation in the Control B register by writing CTRLB.SMEN=1.

Slave DMA

When using the I²C slave with DMA, an address match will cause the address interrupt flag (INTFLAG.ADDRMATCH) to be raised. After the interrupt has been serviced, data transfer will be performed through DMA.

The I²C slave generates the following requests:

- Write data received (RX): The request is set when master write data is received. The request is cleared when DATA is read.
- Read data needed for transmit (TX): The request is set when data is needed for a master read operation. The request is cleared when DATA is written.

Master DMA

When using the I²C master with DMA, the ADDR register must be written with the desired address (ADDR.ADDR), transaction length (ADDR.LEN), and transaction length enable (ADDR.LENEN). When ADDR.LENEN is written to 1 along with ADDR.ADDR, ADDR.LEN determines the number of data bytes in the transaction from 0 to 255. DMA is then used to transfer ADDR.LEN bytes followed by an automatically generated NACK (for master reads) and a STOP.

If a NACK is received by the slave for a master write transaction before ADDR.LEN bytes, a STOP will be automatically generated and the length error (STATUS.LENERR) will be raised along with the INTFLAG.ERROR interrupt.

The I²C master generates the following requests:

- Read data received (RX): The request is set when master read data is received. The request is cleared when DATA is read.
- Write data needed for transmit (TX): The request is set when data is needed for a master write operation. The request is cleared when DATA is written.

30.6.4.2 Interrupts

The I²C slave has the following interrupt sources. These are asynchronous interrupts. They can wake-up the device from any sleep mode:

- Error (ERROR)
- Data Ready (DRDY)
- Address Match (AMATCH)
- Stop Received (PREC)

The I²C master has the following interrupt sources. These are asynchronous interrupts. They can wake-up the device from any sleep mode:

- Error (ERROR)
- Slave on Bus (SB)
- Master on Bus (MB)

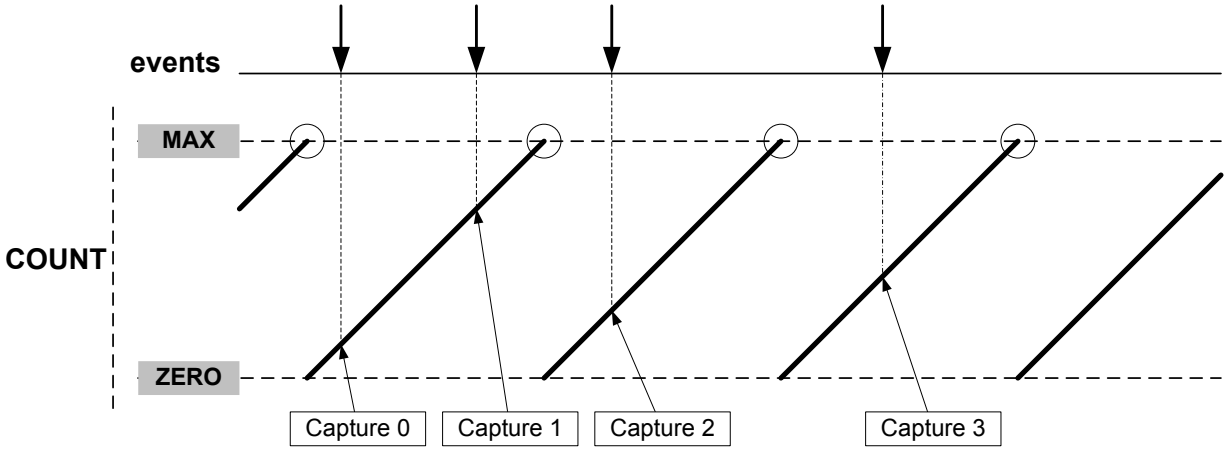
33.6.2.7 Capture Operations

To enable and use capture operations, the Match or Capture Channel x Event Input Enable bit in the Event Control register (EVCTRL.MCEIx) must be written to '1'. The capture channels to be used must also be enabled in the Capture Channel x Enable bit in the Control A register (CTRLA.CPTENx) before capturing can be performed.

Event Capture Action

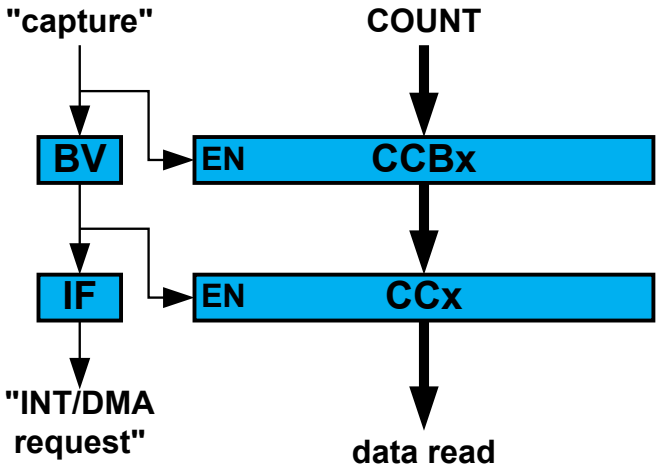
The compare/capture channels can be used as input capture channels to capture events from the Event System, and give them a timestamp. The following figure shows four capture events for one capture channel.

Figure 33-14. Input Capture Timing



For input capture, the buffer register and the corresponding CCx act like a FIFO. When CCx is empty or read, any content in CCBx is transferred to CCx. The buffer valid flag is passed to set the CCx interrupt flag (IF) and generate the optional interrupt, event or DMA request. CCBx register value can't be read, all captured data must be read from CCx register.

Figure 33-15. Capture Double Buffering



The TCC can detect capture overflow of the input capture channels: When a new capture event is detected while the Capture Buffer Valid flag (STATUS.CCBV) is still set, the new timestamp will not be stored and INTFLAG.ERR will be set.

Period and Pulse-Width (PPW) Capture Action

Writing a one to this bit will set the Synchronization Ready Interrupt Enable bit, which enables the Synchronization Ready interrupt.

Value	Description
0	The Synchronization Ready interrupt is disabled.
1	The Synchronization Ready interrupt is enabled.

Bit 2 – WINMON: Window Monitor Interrupt Enable
Writing a zero to this bit has no effect.

Writing a one to this bit will set the Window Monitor Interrupt bit and enable the Window Monitor interrupt.

Value	Description
0	The Window Monitor interrupt is disabled.
1	The Window Monitor interrupt is enabled.

Bit 1 – OVERRUN: Overrun Interrupt Enable
Writing a zero to this bit has no effect.

Writing a one to this bit will set the Overrun Interrupt bit and enable the Overrun interrupt.

Value	Description
0	The Overrun interrupt is disabled.
1	The Overrun interrupt is enabled.

Bit 0 – RESRDY: Result Ready Interrupt Enable
Writing a zero to this bit has no effect.

Writing a one to this bit will set the Result Ready Interrupt bit and enable the Result Ready interrupt.

Value	Description
0	The Result Ready interrupt is disabled.
1	The Result Ready interrupt is enabled.

35.8.12 Interrupt Flag Status and Clear

Name: INTFLAG
Offset: 0x18 [ID-00002049]
Reset: 0x00
Property: -

Bit	7	6	5	4	3	2	1	0
					SYNCRDY	WINMON	OVERRUN	RESRDY
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit 3 – SYNCRDY: Synchronization Ready
This flag is cleared by writing a one to the flag.

This flag is set on a one-to-zero transition of the Synchronization Busy bit in the Status register (STATUS.SYNCBUSY), except when caused by an enable or software reset, and will generate an interrupt request if INTENCLR/SET.SYNCRDY is one.

Writing a zero to this bit has no effect.

Table 39-12. I²C Pins Characteristics in I²C Configuration

Parameter	Condition	Symbol	Min.	Typ.	Max.	Unit
Pull-up - Pull-down resistance		R_{PULL}	20	40	60	kΩ
Input low-level voltage	V_{DD} = 2.7V-3.63V	V_{IL}	-	-	0.3 × V_{DD}	V
Input high-level voltage	V_{DD} = 2.7V-3.63V	V_{IH}	0.55 × V_{DD}	-	-	
Hysteresis of Schmitt trigger inputs		V_{HYS}	0.08 × V_{DD}	-	-	
Output low-level voltage	V_{DD} > 2.0V, I_{OL} = 3mA	V_{OL}	-	-	0.4	
	V_{DD} ≤ 2.0V , I_{OL} = 2mA		-	-	0.2 × V_{DD}	
Output low-level current	V_{OL} = 0.4V Standard, Fast and HS Modes	I_{OL}	3			mA
	V_{OL} = 0.4V Fast Mode +		20	-	-	
	V_{OL} = 0.6V		6	-	-	
SCL clock frequency		f_{SCL}	-	-	3.4	MHz

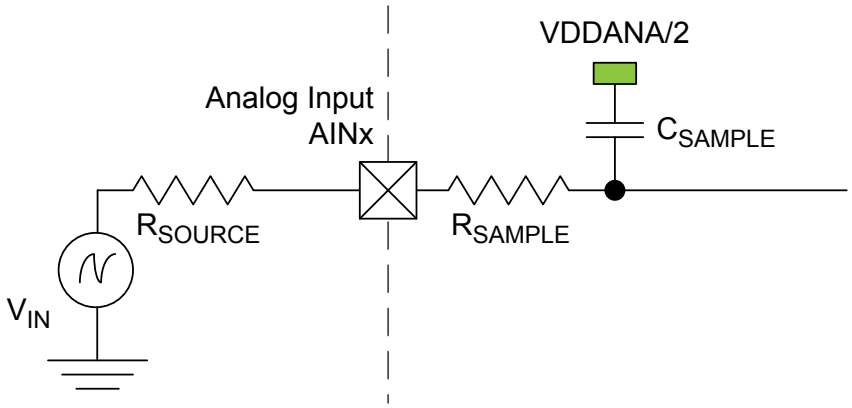
I²C pins timing characteristics can be found in the *SERCOM in I²C Mode Timing* section.

Table 39-13. I²C Pins Characteristics in I/O Configuration

Parameter	Conditions	Symbol	Min.	Typ.	Max.	Unit
Pull-up - Pull-down resistance		R_{PULL}	20	40	60	kΩ
Input low-level voltage	V_{DD} = 2.7V-3.63V	V_{IL}	-	-	0.3 × V_{DD}	V
Input high-level voltage	V_{DD} = 2.7V-3.63V	V_{IH}	0.55 × V_{DD}	-	-	
Output low-level voltage	V_{DD} > 2.7V, IOL max	V_{OL}	-	0.1 × V_{DD}	0.2 × V_{DD}	
Output high-level voltage	V_{DD} > 2.7V, IOH max	V_{OH}	0.8*V_{DD}	0.9 × V_{DD}	-	
Output low-level current	V_{DD} = 2.7V-3V,	I_{OL}				mA
	PORT.PINCFG. DRVSTR=0		-	-	1	
	V_{DD} = 3V-3.63V,					
	PORT.PINCFG. DRVSTR=0		-	-	2.5	
	V_{DD} = 2.7V-3V,					
	PORT.PINCFG. DRVSTR=1		-	-	3	
	V_{DD} = 3V-3.63V,					

calculating the required sample and hold time. The next figure shows the ADC input channel equivalent circuit.

Figure 39-5. ADC Input



To achieve n bits of accuracy, the C_{SAMPLE} capacitor must be charged at least to a voltage of

$$V_{\mathrm{CSAMPLE}} \geq V_{\mathrm{IN}} \times \left(1 + -2^{-(n+1)}\right)$$

The minimum sampling time $t_{\mathrm{SAMPLEHOLD}}$ for a given R_{SOURCE}can be found using this formula:

$$t_{\mathrm{SAMPLEHOLD}} \geq \left(R_{\mathrm{SAMPLE}} + R_{\mathrm{SOURCE}}\right) \times \left(C_{\mathrm{SAMPLE}}\right) \times (n+1) \times \ln(2)$$

for a 12 bits accuracy: $t_{\mathrm{SAMPLEHOLD}} \geq \left(R_{\mathrm{SAMPLE}} + R_{\mathrm{SOURCE}}\right) \times \left(C_{\mathrm{SAMPLE}}\right) \times 9.02$

where

$$t_{\mathrm{SAMPLEHOLD}} = \frac{1}{2 \times f_{\mathrm{ADC}}}$$

39.9.5 Digital to Analog Converter (DAC) Characteristics

Table 39-27. Operating Conditions(1)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DDANA}	Analog supply voltage		2.7	-	3.63	V
AV_{REF}	External reference voltage		1.0	-	V_{DDANA} – 0.6	V
	Internal reference voltage 1		-	1	-	V
	Internal reference voltage 2		-	V_{DDANA}	-	V
	Linear output voltage range		0.05	-	V_{DDANA} – 0.05	V
	Minimum resistive load		5	-	-	kΩ
	Maximum capacitance load		-	-	100	pF
I_{DD}	DC supply current(2)	Voltage pump disabled	-	175	256	µA

1. These values are based on specifications otherwise noted.
2. These values are based on characterization. These values are not covered by test limits in production.

39.9.6 Analog Comparator Characteristics

Table 39-30. Electrical and Timing

Parameter	Conditions	Symbol	Min.	Typ.	Max.	Unit
Positive input voltage range			0	-	V_{DDANA}	V
Negative input voltage range			0	-	V_{DDANA}	
Offset	Hysteresis = 0, Fast mode		–26	0	26	mV
	Hysteresis = 0, Low power mode		–28	0	28	mV
Hysteresis	Hysteresis = 1, Fast mode		8	50	102	mV
	Hysteresis = 1, Low power mode		14	50	75	mV
Propagation delay	Changes for $V_{ACM} = V_{DDANA}/2$ 100mV overdrive, Fast mode			90	180	ns
	Changes for $V_{ACM} = V_{DDANA}/2$ 100mV overdrive, Low power mode			302	534	ns
Startup time	Enable to ready delay Fast mode	$t_{STARTUP}$		1	2	µs
	Enable to ready delay Low power mode		-	14	23	µs
INL(3)		V_{SCALE}	–1.4	0.201	1.4	LSB
DNL(3)			–0.9	0.022	0.9	LSB
Offset Error (1)(2)			–0.2	0.056	0.92	LSB
Gain Error (1)(2)			–0.89	0.079	0.89	LSB

1. According to the standard equation $V(X) = V_{LSB} \times (X + 1)$; $V_{LSB} = V_{DDANA}/64$
2. Data computed with the Best Fit method
3. Data computed using histogram

39.9.7 Internal 1.1V Bandgap Reference Characteristics

Table 39-31. Bandgap and Internal 1.1V Reference Characteristics

Parameter	Conditions	Symbol	Min.	Typ.	Max.	Unit
Internal 1.1V Bandgap reference	After calibration at T= 25°C, over [–40, +105]°C, V_{DD} = 3.3V	INT1V	1.07	1.1	1.12	V
	Over voltage at 25°C		1.08	1.1	1.11	V

Parameter	Conditions	Symbol	Min.	Typ.	Max.	Unit
	at 25°C, over [–40, +105]°C, over [2.7, 3.63]V					
	Calibrated against a 32.768kHz reference at 25°C, at VDD = 3.3V		31.457	32.768	34.078	
	Calibrated against a 32.768kHz reference at 25°C, over [2.7, 3.63]V		31.293	32.768	34.570	
Duty Cycle		Duty	-	50	-	%

1. These values are based on simulation. These values are not covered by test limits in production or characterization.
2. This oscillator is always on.

39.11.6 8MHz RC Oscillator (OSC8M) Characteristics

Table 39-44. Internal 8MHz RC Oscillator Characteristics

Parameter	Conditions	Symbol	Min.	Typ.	Max.	Unit
Output frequency	Calibrated against a 8MHz reference at 25°C, over [–10, +70]C, over [2.7, 3.6]V	f_{OUT}	7.84	8	8.16	MHz
	Calibrated against a 8MHz reference at 25°C, over [–10, +105]°C, over [2.7, 3.6]V		7.80	8	8.20	
	Calibrated against a 8MHz reference at 25°C, over [–40, +105]°C, over [2.7, 3.6]V		7.66	8	8.34	
	Calibrated against a 8MHz reference at 25°C,		7.88	8	8.12	