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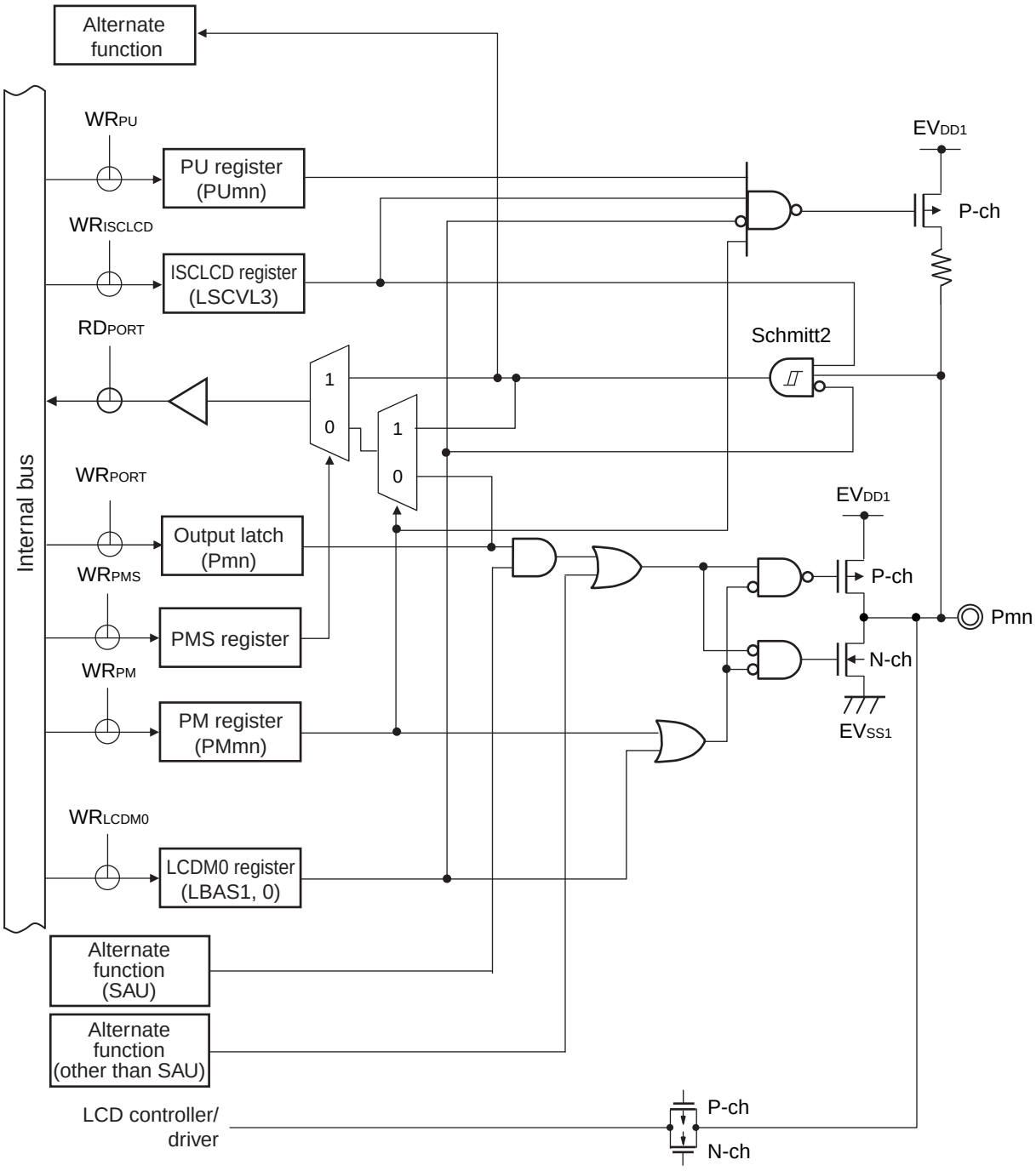
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	RL78
Core Size	16-Bit
Speed	24MHz
Connectivity	CSI, I²C, IrDA, LINbus, UART/USART
Peripherals	Brown-out Detect/Reset, LCD, LVD, POR, PWM, WDT
Number of I/O	53
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	1.9V ~ 5.5V
Data Converters	A/D 4x10b, 3x24b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f10mmedfb-50

Figure 2-11. Pin Block Diagram for Pin Type 7-5-6



Remarks 1. For alternate functions, see **2.1 Port Function**.

2. SAU: Serial array unit

3.4.8 Based indexed addressing

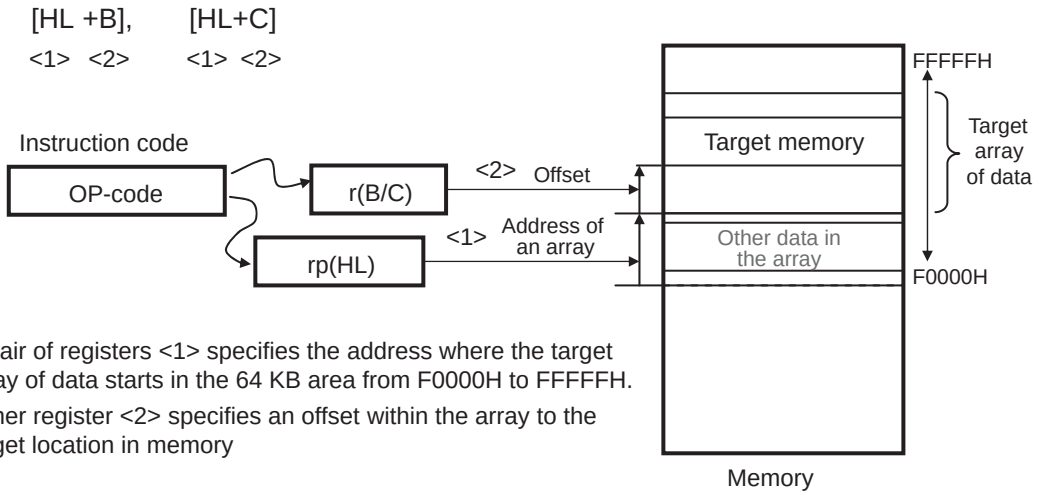
[Function]

Based indexed addressing uses the contents of a register pair specified with the instruction word as the base address, and the content of the B register or C register similarly specified with the instruction word as offset address. The sum of these values is used to specify the target address.

[Operand format]

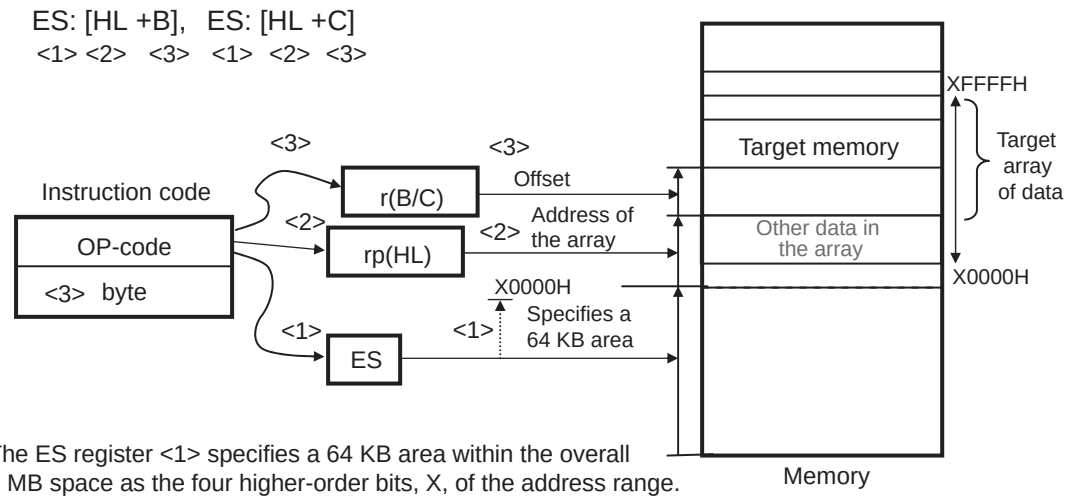
Identifier	Description
–	[HL+B], [HL+C] (only the space from F0000H to FFFFFH is specifiable)
–	ES:[HL+B], ES:[HL+C] (higher 4-bit addresses are specified by the ES register)

Figure 3-31. Example of [HL+B], [HL+C]



- A pair of registers <1> specifies the address where the target array of data starts in the 64 KB area from F0000H to FFFFFH.
- Either register <2> specifies an offset within the array to the target location in memory

Figure 3-32. Example of ES:[HL+B], ES:[HL+C]



- The ES register <1> specifies a 64 KB area within the overall 1 MB space as the four higher-order bits, X, of the address range.
- A pair of registers <2> specifies the address where the target array of data starts in the 64 KB area specified in the ES register <1>.
- Either register <3> specifies an offset within the array to the target location in memory.

4.5.3 Register setting examples for used port and alternate functions

Register setting examples for used port and alternate functions are shown in Table 4-6. The registers used to control the port functions should be set as shown in Table 4-6. See the following remark for legends used in Table 4-6.

Remark –: Not supported
×: don't care
PIORx: Peripheral I/O redirection register
POMxx: Port output mode register
PMxx: Port mode register
Pxx: Port output latch
PUxx: Pull-up resistor option register
PIMcc: Port input mode register
PFSEG××: LCD port function register
ISCLCD: LCD input switch control register

Figure 7-12. Format of Timer Mode Register mn (TMRmn) (2/4)

Address: F0190H, F0191H (TMR00) to F019EH, F019FH (TMR07) After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TMRmn (n = 2, 4, 6)	CKS mn1	CKS mn0	0	CCS mn	MASTERmn	STS mn2	STS mn1	STS mn0	CIS mn1	CIS mn0	0	0	MD mn3	MD mn2	MD mn1	MD mn0

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TMRmn (n = 1, 3)	CKS mn1	CKS mn0	0	CCS mn	SPLIT mn	STS mn2	STS mn1	STS mn0	CIS mn1	CIS mn0	0	0	MD mn3	MD mn2	MD mn1	MD mn0

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TMRmn (n = 0, 5, 7)	CKS mn1	CKS mn0	0	CCS mn	0[Note]	STS mn2	STS mn1	STS mn0	CIS mn1	CIS mn0	0	0	MD mn3	MD mn2	MD mn1	MD mn0

(Bit 11 of TMRmn (n = 2, 4, 6))

MASTER mn	Selection between using channel n independently or simultaneously with another channel(as a slave or master)
0	Operates in independent channel operation function or as slave channel in simultaneous channel operation function.
1	Operates as master channel in simultaneous channel operation function.
Only the channel 2, 4, 6 can be set as a master channel (MASTERmn = 1). Be sure to use channel 0, 5, 7 are fixed to 0 (Regardless of the bit setting, channel 0 operates as master, because it is the highest channel). Clear the MASTERmn bit to 0 for a channel that is used with the independent channel operation function.	

(Bit 11 of TMRmn (n = 1, 3))

SPLITmn	Selection of 8 or 16-bit timer operation for channels 1 and 3
0	Operates as 16-bit timer. (Operates in independent channel operation function or as slave channel in simultaneous channel operation function.)
1	Operates as 8-bit timer.

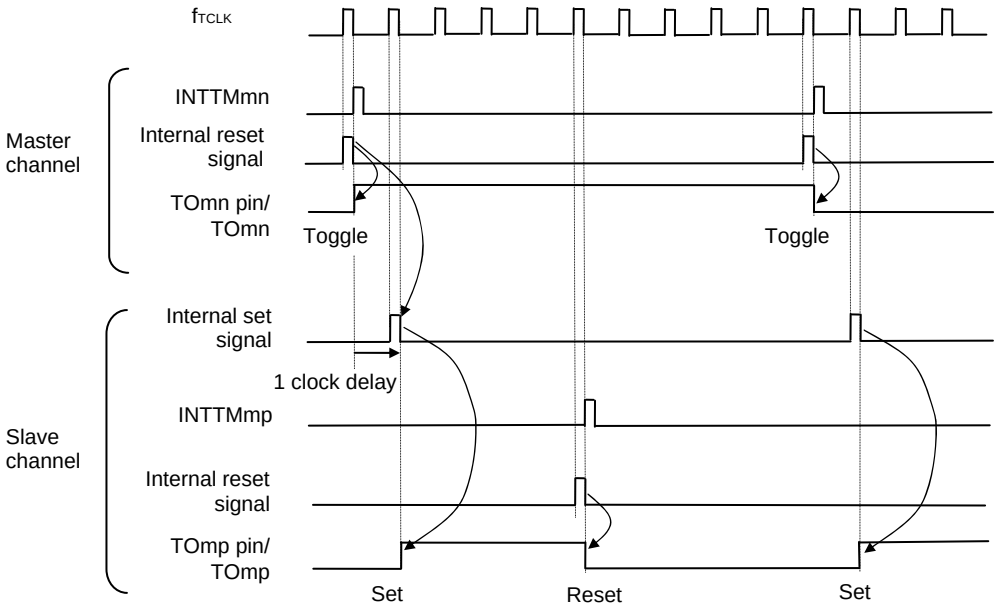
STS mn2	STS mn1	STS mn0	Setting of start trigger or capture trigger of channel n
0	0	0	Only software trigger start is valid (other trigger sources are unselected).
0	0	1	Valid edge of the TImn pin input is used as both the start trigger and capture trigger.
0	1	0	Both the edges of the TImn pin input are used as a start trigger and a capture trigger.
1	0	0	Interrupt signal of the master channel is used (when the channel is used as a slave channel with the simultaneous channel operation function).
Other than above			Setting prohibited

Note Bit 11 is fixed at 0 of read only, write is ignored.

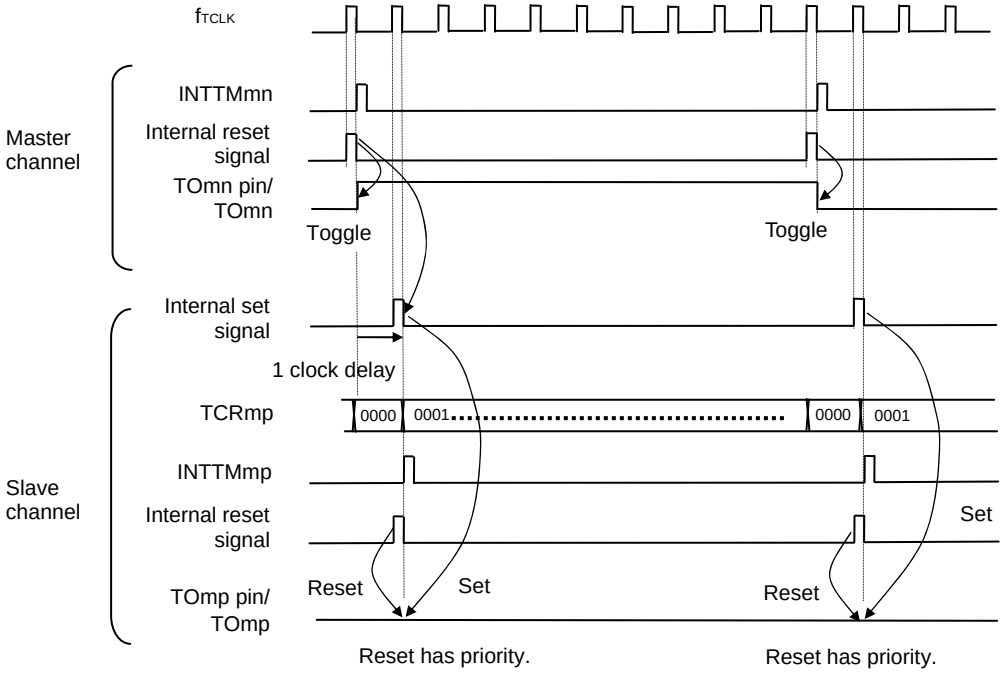
Remark m: Unit number (m = 0), n: Channel number (n = 0 to 7)

Figure 7-36. Set/Reset Timing Operating Statuses

(1) Basic operation timing



(2) Operation timing when 0 % duty



Remarks 1. Internal reset signal: TOmn pin reset/toggle signal
Internal set signal: TOmn pin set signal

2. m: Unit number (m = 0)
n: Channel number
n = 0 to 7 (n = 0, 2, 4, 6 for master channel)
p: Slave channel number
n < p ≤ 7

11.3.1 8-bit interval timer counter register ni (TRTni) (n = 0 or 1, i = 0 or 1)

This is the 8-bit interval timer counter register. It is used as a counter that counts up based on the count clock.

The TRTni register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 11-2. Format of 8-bit Interval Timer Counter Register ni (TRTni)

Address: F0540H (TRT00), F0541H (TRT01), F0548H (TRT10), F0549H (TRT11) After reset: 00H R[Notes 1, 2]

Symbol	7	6	5	4	3	2	1	0
TRTni								

Notes 1. The TRTni register is set to 00H two count clock cycles after the compare register TRTCMPni is write-accessed. See **11.4.4 Timing of updating compare register values**.

2. Can be accessed only when the mode select bit (TCSMDn) in 8-bit interval timer control register n (TRTCRn) is 0.

11.3.2 8-bit interval timer counter register n (TRTn) (n = 0 or 1)

This is a 16-bit counter register when the 8-bit interval timer is used in 16-bit interval timer mode.

The TRTn register can be set by a 16-bit memory manipulation instruction.

Reset signal generation sets this register to 0000H.

Figure 11-3. Format of 8-bit Interval Timer Counter Register n (TRTn)

Address: F0540H (TRT0), F0548H (TRT1) After reset: 0000H R[Notes 1, 2]

	F0541H (TRT01) / F0549H (TRT11)								F0540H (TRT00) / F0548H (TRT10)							
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TRTn																

Notes 1. The TRTn register is set to 0000H two count clock cycles after the compare register TRTCMPn is write-accessed. See **11.4.4 Timing of updating compare register values**.

2. Can be accessed only when the mode select bit (TCSMDn) in 8-bit interval timer control register n (TRTCRn) is 1.

When the count value matches the compare value, the count value is cleared at the next count source cycle. When the compare value in the TRTCMPni register is rewritten, the count value is also cleared two count source cycles after writing.

Table 11-5 lists the interrupt sources in 8-bit and 16-bit counter modes.

Table 11-5. Interrupt Sources in 8-bit and 16-bit Counter Modes

Interrupt Name	Interrupt Source in 8-bit Counter Mode	Interrupt Source in 16-bit Counter Mode
INTITn0	Rising edge of the count source cycle after compare match on channel 0	Rising edge of the count source cycle after compare match
INTITn1	Rising edge of the count source cycle after compare match on channel 1	Not generated

Remark n = 0, 1

(5) Successive approximation register (SAR)

The SAR register is a register that sets voltage tap data whose values from the comparison voltage generator match the voltage values of the analog input pins, 1 bit at a time starting from the most significant bit (MSB).

If data is set in the SAR register all the way to the least significant bit (LSB) (end of A/D conversion), the contents of the SAR register (conversion results) are held in the A/D conversion result register (ADCR). When all the specified A/D conversion operations have ended, an A/D conversion end interrupt request signal (INTAD) is generated.

(6) 10-bit A/D conversion result register (ADCR)

The A/D conversion result is loaded from the successive approximation register to this register each time A/D conversion is completed, and the ADCR register holds the A/D conversion result in its higher 10 bits (the lower 6 bits are fixed to 0).

(7) 8-bit A/D conversion result register (ADCRH)

The A/D conversion result is loaded from the successive approximation register to this register each time A/D conversion is completed, and the ADCRH register stores the higher 8 bits of the A/D conversion result.

(8) Controller

This circuit controls the conversion time of an input analog signal that is to be converted into a digital signal, as well as starting and stopping of the conversion operation. When A/D conversion has been completed, this controller generates INTAD through the A/D conversion result upper limit/lower limit comparator.

(9) AV_{REFP} pin

This pin inputs an external reference voltage (AV_{REFP}).

If using AV_{REFP} as the + side reference voltage of the A/D converter, set the ADREFP1 and ADREFP0 bits of A/D converter mode register 2 (ADM2) to 0 and 1, respectively.

The analog signals input to ANI2 to ANI5 are converted to digital signals based on the voltage applied between AV_{REFP} and the – side reference voltage (AV_{REFM}/V_{SS}).

In addition to AV_{REFP}, it is possible to select V_{DD} or the internal reference voltage (1.45 V) as the + side reference voltage of the A/D converter.

(10) AV_{REFM} pin

This pin inputs an external reference voltage (AV_{REFM}). If using AV_{REFM} as the – side reference voltage of the A/D converter, set the ADREFM bit of the ADM2 register to 1.

In addition to AV_{REFM}, it is possible to select V_{SS} as the – side reference voltage of the A/D converter.

(2) Operation procedure

Figure 18-26. Initial Setting Procedure for Master Transmission

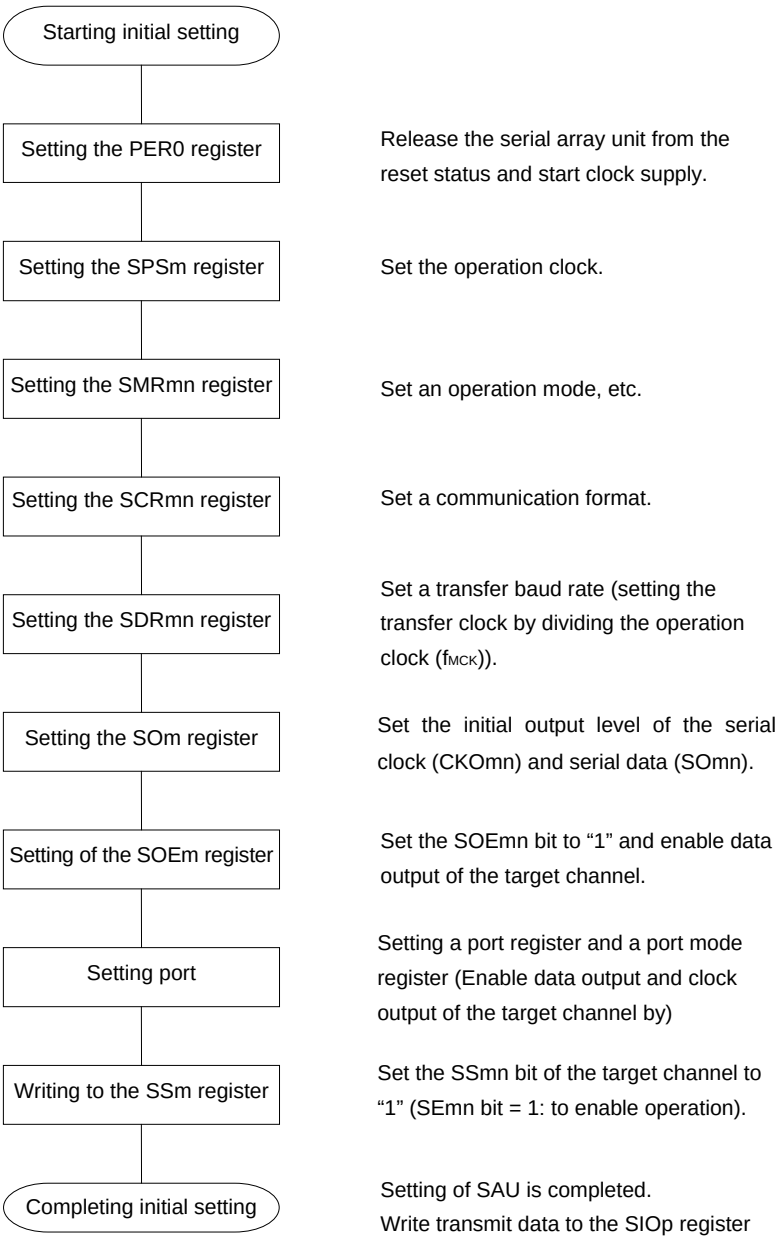
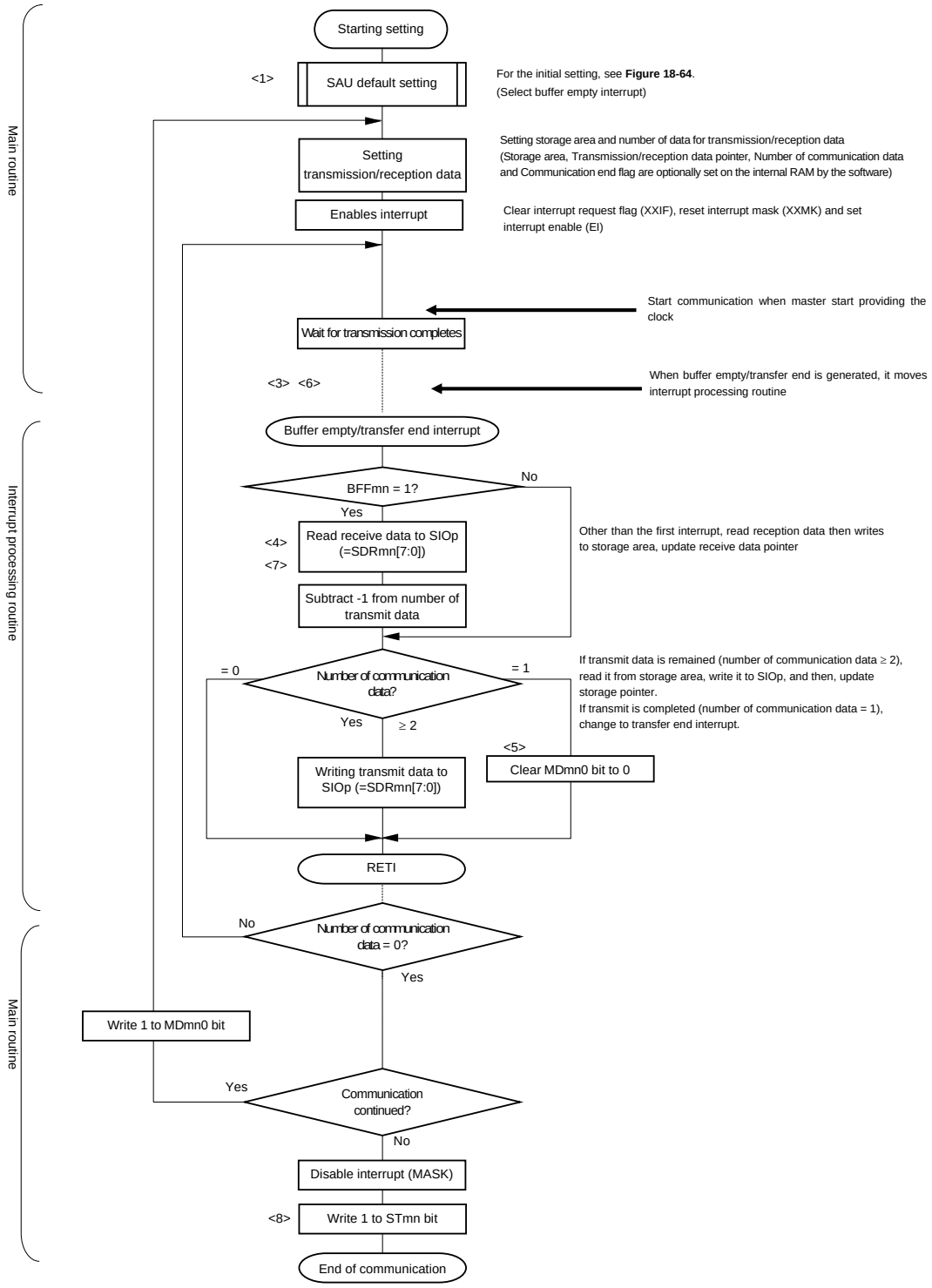


Figure 18-70. Flowchart of Slave Transmission/Reception (in Continuous Transmission/Reception Mode)



Caution Be sure to set transmit data to the SIOp register before the clock from the master is started.

Remark <1> to <8> in the figure correspond to <1> to <8> in **Figure 18-69 Timing Chart of Slave Transmission/Reception (in Continuous Transmission/Reception Mode)**.

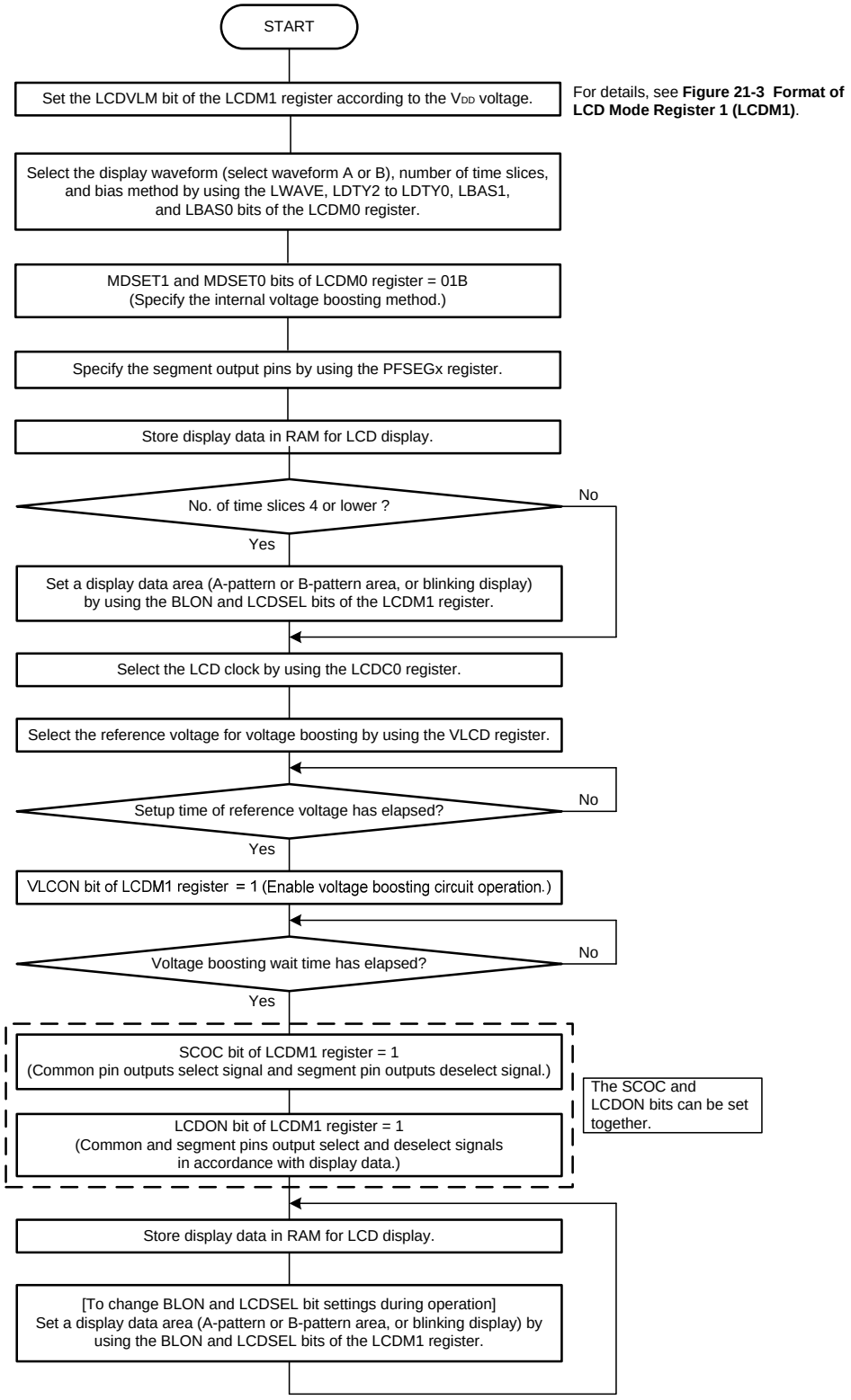
The peripheral functions used for the LIN communication operation are as follows.

<Peripheral functions used>

- External interrupt (INTP0); Wakeup signal detection
  Usage: To detect an edge of the wakeup signal and the start of communication
- Channel 7 of timer array unit; Baud rate error detection, break field detection.
  Usage: To detect the length of the sync field (SF) and divide it by the number of bits in order to detect an error (The interval of the edge input to RxD0 is measured in the capture mode.)
  Measured the low-level width, determine whether break field (BF).
- Channels 0 and 1 (UART0) of serial array unit 0 (SAU0)

(2) Internal voltage boosting method

Figure 21-17. Internal Voltage Boosting Method Setting Procedure



Cautions 1. Wait until the setup time has elapsed even if not changing the setting of the VLCD register.

2. For the specifications of the reference voltage setup time and voltage boosting wait time, see CHAPTER 37 ELECTRICAL SPECIFICATIONS.

22.5 Notes on DTC

22.5.1 Setting DTC control data and vector table

- Do not access the DTC SFRs, the DTC control data area, the DTC vector table area, or the general-register (FFEE0H to FFEFFH) space using a DTC transfer.
- Modify the DTC base address register (DTCBAR) while all DTC activation sources are set to activation disabled.
- Do not rewrite the DTC base address register (DTCBAR) twice or more.
- Modify the data of the DTCCRj, DTBLSj, DTCCTj, DTRLDj, DTSARj, or DTDARj register when the corresponding bit among bits DTCENi0 to DTCENi7 in the DTCENi (i = 0 to 3) register is 0 (DTC activation disabled).
- Modify the start address of the DTC control data area to be set in the vector table when the corresponding bit among bits DTCENi0 to DTCENi7 in the DTCENi (i = 0 to 3) register is 0 (DTC activation disabled).
- Do not allocate RAM addresses which are used as a DTC transfer destination/transfer source to the area FFE20H to FFEDFH when performing self-programming.

22.5.2 Allocation of DTC control data area and DTC vector table area

The areas where the DTC control data and vector table can be allocated differ.

- It is prohibited to use the general-purpose register (FFEE0H to FFEFFH) space as the DTC control data area or DTC vector table area.
- Make sure the stack area, the DTC control data area, and the DTC vector table area do not overlap.
- The internal RAM area in the following products cannot be used as the DTC control data area or DTC vector table area when using the self-programming.
  R5F10MMGDFB, R5F10MPGDFB : FDF00H-FE309H
  R5F10MMEDFB, R5F10MPEDFB : FE700H-FEB09H
- The internal RAM area in the following products cannot be used as the DTC control data area or DTC vector table area when using the on-chip trace function.
  R5F10MME, R5F10MPE, R5F10MMG, R5F10MPG: FE300H to FE6FFH
- Initialize the DTRLD register to 00H even in normal mode when parity error resets are enabled (RPERDIS = 0) using the RAM parity error detection function.

22.5.3 DTC pending instruction

Even if a DTC transfer request is generated, data transfer is held pending immediately after the following instructions. Also, the DTC is not activated between PREFIX instruction code and the instruction immediately after that code.

- Call/return instruction
- Unconditional branch instruction
- Conditional branch instruction
- Read access instruction for code flash memory
- Bit manipulation instructions for IFxx, MKxx, PRxx, and PSW, and an 8-bit manipulation instruction that has the ES register as operand

<R>
- Instruction of Multiply, Divide, Multiply & Accumulate (excluding MULU)

Cautions 1. When a DTC transfer request is acknowledged, all interrupt requests are held pending until DTC transfer is completed.

2. While the DTC is held pending by the DTC pending instruction, all interrupt requests are held pending.

23.4 Interrupt Servicing Operations

23.4.1 Maskable interrupt request acknowledgment

A maskable interrupt request becomes acknowledgeable when the interrupt request flag is set to 1 and the mask (MK) flag corresponding to that interrupt request is cleared to 0. A vectored interrupt request is acknowledged if interrupts are in the interrupt enabled state (when the IE flag is set to 1). However, a low-priority interrupt request is not acknowledged during servicing of a higher priority interrupt request.

The times from generation of a maskable interrupt request until vectored interrupt servicing is performed are listed in Table 23-4 below.

For the interrupt request acknowledgment timing, see **Figures 23-8** and **23-9**.

Table 23-4. Time from Generation of Maskable Interrupt Until Servicing

	Minimum Time	Maximum Time[Note]
Servicing time	9 clocks	16 clocks

Note Maximum time does not apply when an instruction from the internal RAM area is executed.

Remark 1 clock: $1/f_{CLK}$ (f_{CLK}: CPU clock)

If two or more maskable interrupt requests are generated simultaneously, the request with a higher priority level specified in the priority specification flag is acknowledged first. If two or more interrupts requests have the same priority level, the request with the highest default priority is acknowledged first.

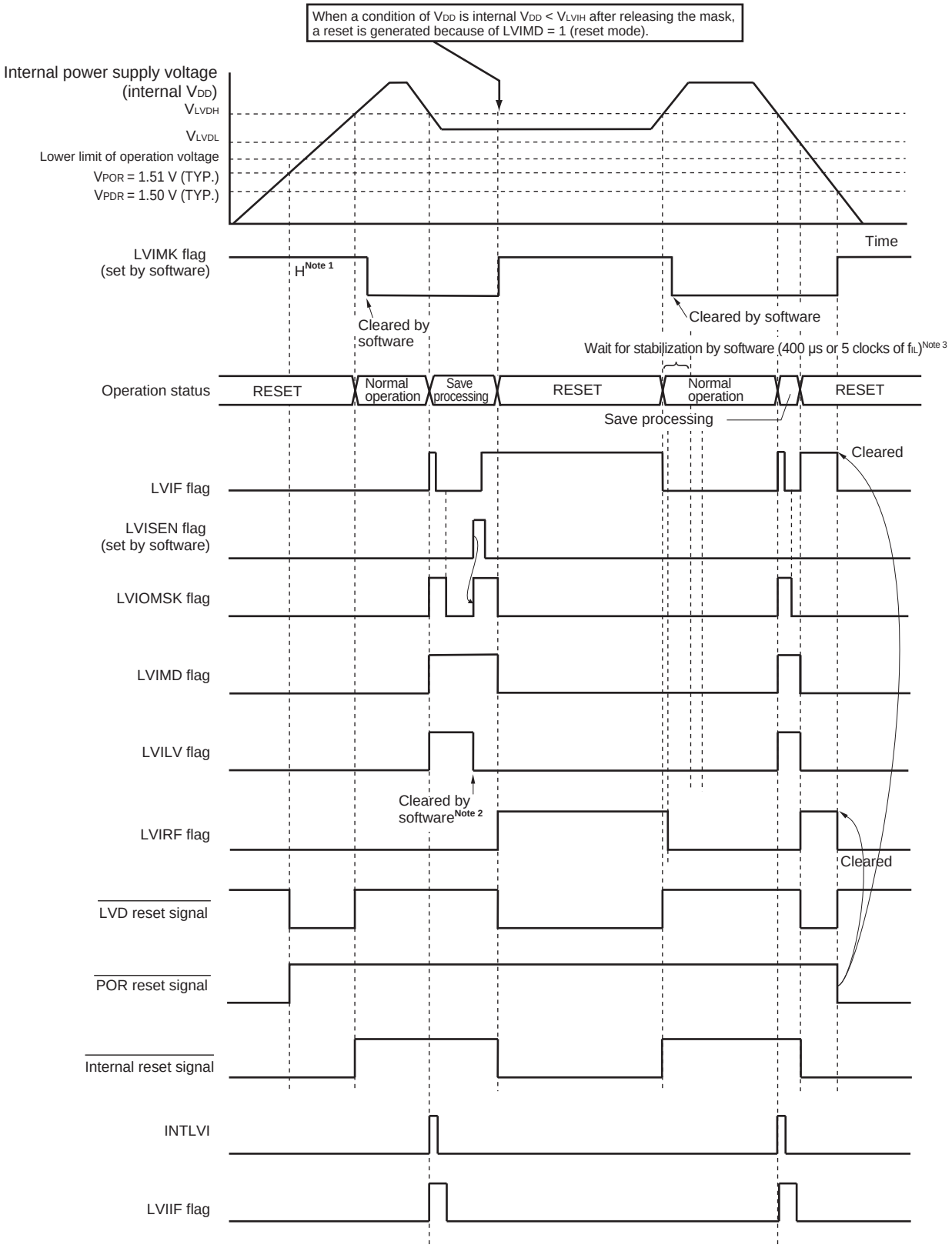
An interrupt request that is held pending is acknowledged when it becomes acknowledgeable.

Figure 23-7 shows the interrupt request acknowledgment algorithm.

If a maskable interrupt request is acknowledged, the contents are saved into the stacks in the order of PSW, then PC, the IE flag is reset (0), and the contents of the priority specification flag corresponding to the acknowledged interrupt are transferred to the ISP1 and ISP0 flags. The vector table data determined for each interrupt request is the loaded into the PC and branched.

Restoring from an interrupt is possible by using the RETI instruction.

Figure 27-7. Timing of Voltage Detector Reset Signal and Interrupt Signal Generation (Option Byte LVIMDS1, LVIMDS0 = 1, 0) (2/2)



(**Notes** and **Remark** are listed on the next page.)

CHAPTER 28 BATTERY BACKUP FUNCTION

28.1 Functions of Battery Backup

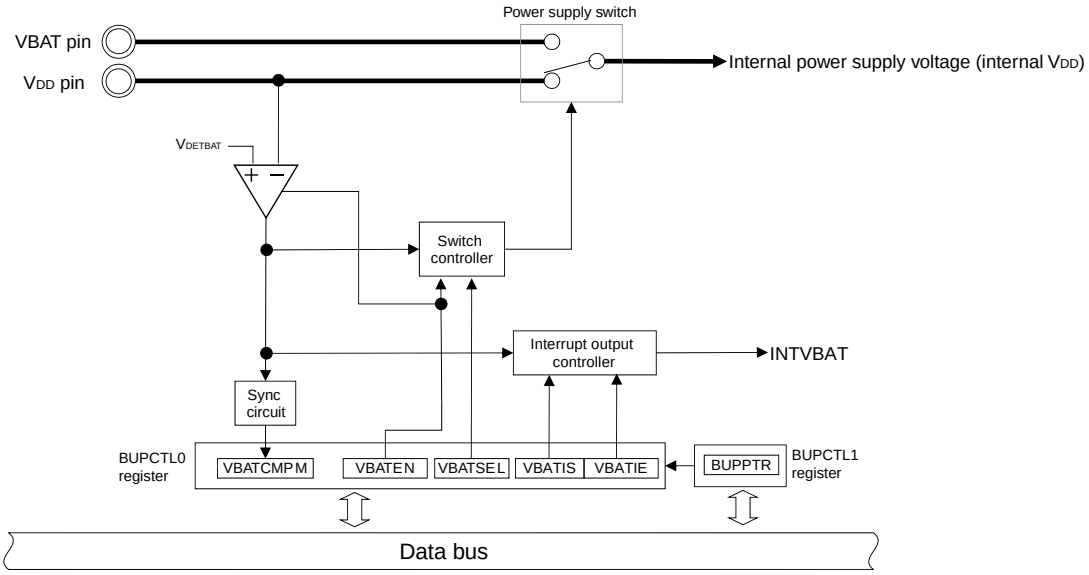
This function monitors the supply voltage at the V_{DD} pin, and switches the internal power supply from the dedicated battery backup power pin (VBAT pin) when the voltage at the V_{DD} pin falls below the detection voltage. The mode used to supply the internal power from the VBAT pin is referred to as battery backup mode. Even if power supply from the V_{DD} pin is cut off due to a power outage, operation of real-time clock 2 (RTC2) can be continued by switching to battery backup mode by hardware. In addition to real-time clock 2 (RTC2), the CPU, the 10-bit A/D converter, the on-chip temperature sensor, the comparator, external interrupts, and V_{DD} power supply system I/O[Note] can be operated in battery backup mode.

- When the voltage at the V_{DD} pin falls to or below the detection voltage, the internal power supply can be switched from V_{DD} supply to VBAT supply. When the voltage at the V_{DD} pin rises to or above the detection voltage again, the internal power supply can be switched from VBAT supply to V_{DD} supply.
- When VBAT ≥ V_{DD}, internal power supply can be switched to VBAT by software.
- A power switching detection interrupt (INTVBAT) can be generated when the power is switched. However, no interrupt is generated when the power is switched by software, and an interrupt is generated when the supply voltage at the V_{DD} pin reaches the detection voltage.

Note P20 to P25, P121 to P124, P137

Figure 28-1 shows the block diagram of the battery backup function.

Figure 28-1. Block Diagram of Battery Backup Function



28.1.1 Pin configuration

Table 28-1 lists the pin configuration of battery backup function.

Table 28-1. Pin Configuration of Battery Backup Function

Name	Function
V_{DD}	Positive power from the pin
VBAT	Power for battery backup

28.2.2 Battery backup power switching control register 1 (BUPCTL1)

The BUPCTL1 register is used to disable or enable rewriting of the BUPCTL0 register. Since rewriting of the BUPCTL0 register is disabled when the BUPPRT bit is 0, the BUPCTL0 register can be prevented from being written inadvertently.

The BUPCTL1 register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 28-3. Format of Battery Backup Power Switching Control Register 1 (BUPCTL1)

Address: F0331H After reset: 00H R/W

Symbol	<7>	6	5	4	3	2	1	0
BUPCTL1	BUPPRT	0	0	0	0	0	0	0

BUPPRT	BUPCTL0 register write protection control
0	The BUPCTL0 register cannot be written, but it can be read.
1	The BUPCTL0 register can be written and read.

Caution Be sure to clear bits 6 to 0 to 0.

28.2.3 Global digital input disable register (GDIDIS)

When EV_{DD} and V_{DD} are used at the same potential, if power supply from the V_{DD} pin is stopped due to power outage, EV_{DD} supply will also stop and drop to 0 V. The GDIDIS register prevents through-current to the input buffer when EV_{DD} = 0 V. Setting the GDIDIS0 bit to 1 disables input to all input buffers[Note] connected to EV_{DD}, and prevents shoot-through current when the power connected to EV_{DD} is turned off. When using the GDIDIS register, set GDIDIS0 to 1 before turning off the power for EV_{DD}, and then set GDIDIS0 to 0 after turning on the power for EV_{DD}.

The GDIDIS register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Note Port pin other than P20 to P25, P121 to P124, and P137.
Because the power supply of the I/O buffer switches to V_{DD} or VBAT pin with the battery backup function, I/O of P20 to P25, P121 to P124, and P137 can be used even when GDIDIS is set to 1.
See **Table 2-1 Pin I/O Buffer Power Supplies** for the I/O buffer power of the pins.

Figure 28-4. Format of Global Digital Input Disable Register (GDIDIS)

Address: F007DH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
GDIDIS	0	0	0	0	0	0	0	GDIDIS0

GDIDIS0	Setting of input buffers using EV_{DD} power supply
0	Input to input buffers permitted (default)
1	Input to input buffers prohibited. No through-current flows to the input buffers.

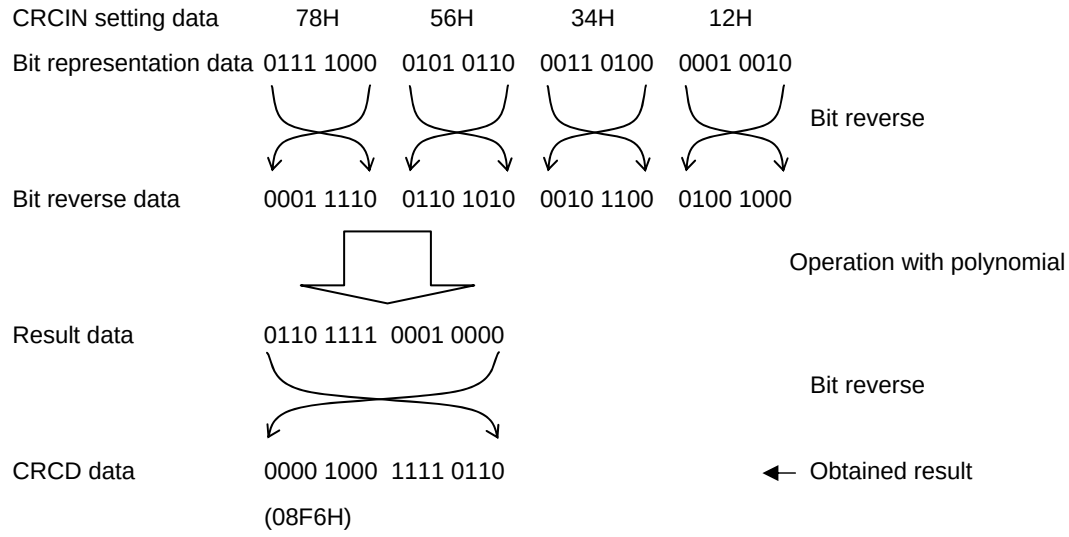
30.3.2 CRC operation function (general-purpose CRC)

In order to guarantee safety during operation, the IEC61508 standard mandates the checking of data even while the CPU is operating.

In the RL78/I1B, a general CRC operation can be executed as a peripheral function while the CPU is operating. The general CRC can be used for checking various data in addition to the code flash memory area. The data to be checked can be specified by using software (a user-created program). CRC calculation function in the HALT mode can be used only during the DTC transmission.

The general CRC operation can be executed in the main system clock operation mode as well as the subsystem clock operation mode.

The CRC generator polynomial used is "$X^{16} + X^{12} + X^5 + 1$" of CRC-16-CCITT. The data to be input is inverted in bit order and then calculated to allow for LSB-first communication. For example, if the data 12345678H is sent from the LSB, values are written to the CRCIN register in the order of 78H, 56H, 34H, and 12H, enabling a value of 08F6H to be obtained from the CRCD register. This is the result obtained by executing a CRC operation on the bit rows shown below, which consist of the data 12345678H inverted in bit order.



Caution Because the debugger rewrites the software break setting line to a break instruction during program execution, the CRC operation result differs if a software break is set in the CRC operation target area.

30.3.2.1 CRC input register (CRCIN)

CRCIN register is an 8-bit register that is used to set the CRC operation data of general-purpose CRC.

The possible setting range is 00H to FFH.

The CRCIN register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 30-4. Format of CRC Input Register (CRCIN)

Address: FFFACH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
CRCIN								

Bits 7 to 0	Function
00H to FFH	Data input.

33.4.4 Communication commands

The RL78 microcontroller executes serial programming through the commands listed in **Table 33-7.**

The signals sent from the dedicated flash memory programmer or external device to the RL78 microcontroller are called commands, and programming functions corresponding to the commands are executed. For details, refer to the **RL78 Microcontrollers (RL78 Protocol A) Programmer Edition Application Note (R01AN0815)**.

Table 33-7. Flash Memory Control Commands

Classification	Command Name	Function
Verify	Verify	Compares the contents of a specified area of the flash memory with data transmitted from the programmer.
Erase	Block Erase	Erases a specified area in the flash memory.
Blank check	Block Blank Check	Checks if a specified block in the flash memory has been correctly erased.
Write	Programming	Writes data to a specified area in the flash memory[Note].
Getting information	Silicon Signature	Gets the RL78 microcontroller information (such as the part number, flash memory configuration, and programming firmware version).
	Checksum	Gets the checksum data for a specified area.
Security	Security Set	Sets security information.
	Security Get	Gets security information.
	Security Release	Release setting of prohibition of writing.
Others	Reset	Used to detect synchronization status of communication.
	Baud Rate Set	Sets baud rate when UART communication mode is selected.

Note Confirm that no data has been written to the write area. Because data cannot be erased after block erase is prohibited, do not write data if the data has not been erased.

Product information (such as product name and firmware version) can be obtained by executing the “Silicon Signature” command.

Table 33-8 is a list of signature data and **Table 33-9** shows an example of signature data.

Table 33-8. Signature Data List

Field Name	Description	Number of Transmit Data
Device code	The serial number assigned to the device	3 bytes
Device name	Device name (ASCII code)	10 bytes
Code flash memory area last address	Last address of code flash memory area (Sent from lower address. Example. 00000H to 0FFFFH (64 KB) → FFH, 1FH, 00H)	3 bytes
Firmware version	Version information of firmware for programming (Sent from upper address. Example. From Ver. 1.23 → 01H, 02H, 03H)	3 bytes

37.2 Oscillator Characteristics

37.2.1 X1, XT1 oscillator characteristics

(T_A = –40 to +85°C, 1.9 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Resonator	Conditions	MIN.	TYP.	MAX.	Unit
X1 clock oscillation frequency (f_X) Notes 1, 2	Ceramic resonator/ crystal resonator	2.7 V ≤ V_{DD} ≤ 5.5 V	1.0		20.0	MHz
		2.4 V ≤ V_{DD} < 2.7 V	1.0		16.0	MHz
		1.9 V ≤ V_{DD} < 2.4 V	1.0		8.0	MHz
XT1 clock oscillation frequency (f_{XT}) Notes 1, 2	Crystal resonator		32	32.768	35	kHz

Notes 1. Indicates only permissible oscillator frequency ranges. See **37.4 AC Characteristics** for instruction execution time. Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

2. Voltage range is the power supply voltage (VBAT pin or V_{DD} pin) selected by the battery backup function.

Caution Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.

Remark When using the X1 oscillator and XT1 oscillator, see **5.4 System Clock Oscillator**.