Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	RL78
Core Size	16-Bit
Speed	24MHz
Connectivity	CSI, I²C, IrDA, LINbus, UART/USART
Peripherals	Brown-out Detect/Reset, LCD, LVD, POR, PWM, WDT
Number of I/O	53
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.9V ~ 5.5V
Data Converters	A/D 4x10b, 3x24b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f10mmgdfb-50

Figure 2-5. Pin Block Diagram for Pin Type 4-3-3

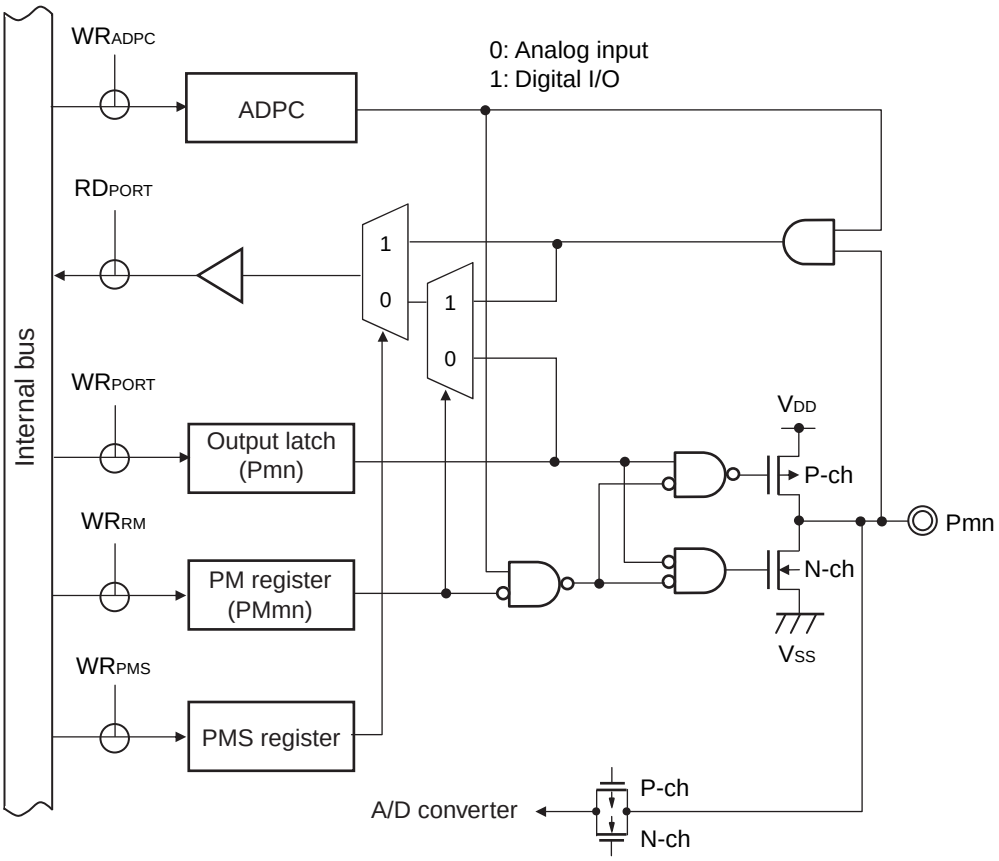
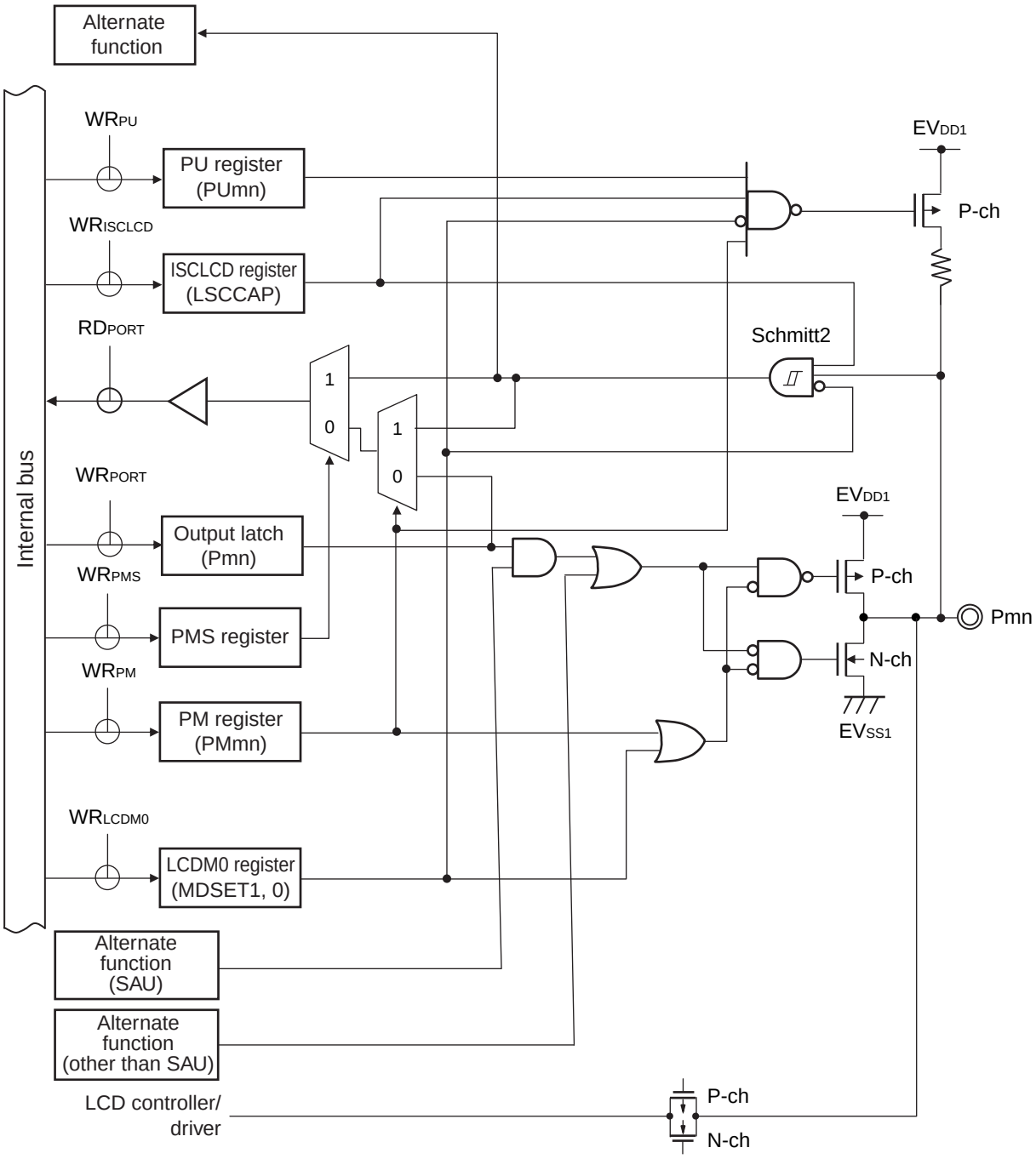


Figure 2-10. Pin Block Diagram for Pin Type 7-5-5



Remarks 1. For alternate functions, see **2.1 Port Function**.

2. SAU: Serial array unit

4.3.1 Port mode registers (PMxx)

These registers specify input or output mode for the port in 1-bit units.

These registers can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets these registers to FFH.

When port pins are used as alternate-function pins, set the port mode register by referencing **4.5 Register Settings When Using Alternate Function**.

Figure 4-1. Format of Port Mode Register

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
PM0	PM07	PM06	PM05	PM04	PM03	PM02	PM01	PM00	FFF20H	FFH	R/W
PM1	PM17	PM16	PM15	PM14	PM13	PM12	PM11	PM10	FFF21H	FFH	R/W
PM2	1	1	PM25	PM24	PM23	PM22	PM21	PM20	FFF22H	FFH	R/W
PM3	PM37	PM36	PM35	PM34	PM33	PM32	PM31	PM30	FFF23H	FFH	R/W
PM4	1	1	1	PM44	PM43	PM42	PM41	PM40	FFF24H	FFH	R/W
PM5	PM57	PM56	PM55	PM54	PM53	PM52	PM51	PM50	FFF25H	FFH	R/W
PM6	1	1	1	1	1	PM62	PM61	PM60	FFF26H	FFH	R/W
PM7	PM77	PM76	PM75	PM74	PM73	PM72	PM71	PM70	FFF27H	FFH	R/W
PM8	1	1	PM85	PM84	PM83	PM82	PM81	PM80	FFF28H	FFH	R/W
PM12	PM127	PM126	PM125	1	1	1	1	1	FFF2CH	FFH	R/W

PMmn	Pmn pin I/O mode selection (m = 0 to 8, 12; n = 0 to 7)
0	Output mode (output buffer on)
1	Input mode (output buffer off)

Caution Be sure to set bits that are not mounted to their initial values.

4.6.2 Notes on specifying the pin settings

If the output function of an alternate function is assigned to a pin that is also used as an output pin, the output of the unused alternate function must be set to its initial state so as to prevent conflicting outputs. This also applies to the functions assigned by using the peripheral I/O redirection register (PIOR). For details about the alternate output function, see **4.5 Register Settings When Using Alternate Function**.

No specific setting is required for input pins because the output function of their alternate functions is disabled (the buffer output is Hi-Z).

Disabling the unused functions, including blocks that are only used for input or do not have output, is recommended to lower power consumption.

Figure 7-11. Format of Timer Clock Select register m (TPSm) (2/2)

Address: F01B6H, F01B7H After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TPSm	0	0	PRS m31	PRS m30	0	0	PRS m21	PRS m20	PRS m13	PRS m12	PRS m11	PRS m10	PRS m03	PRS m02	PRS m01	PRS m00

PRS m21	PRS m20	Selection of operation clock (CKm2)[Note]					
			f_{CLK} = 4 MHz	f_{CLK} = 8 MHz	f_{CLK} = 12 MHz	f_{CLK} = 20 MHz	f_{CLK} = 24 MHz
0	0	$f_{CLK}/2$	2 MHz	4 MHz	6 MHz	10 MHz	12 MHz
0	1	$f_{CLK}/2^2$	1 MHz	2 MHz	3 MHz	5 MHz	6 MHz
1	0	$f_{CLK}/2^4$	250 kHz	500 kHz	750 kHz	1.25 MHz	1.5 MHz
1	1	$f_{CLK}/2^6$	62.5 kHz	125 kHz	188 kHz	313 kHz	375 kHz

PRS m31	PRS m30	Selection of operation clock (CKm3)[Note]					
			f_{CLK} = 4 MHz	f_{CLK} = 8 MHz	f_{CLK} = 12 MHz	f_{CLK} = 20 MHz	f_{CLK} = 24 MHz
0	0	$f_{CLK}/2^8$	15.6 kHz	31.3 kHz	46.9 kHz	78.1 kHz	93.8 kHz
0	1	$f_{CLK}/2^{10}$	3.91 kHz	7.81 kHz	11.7 kHz	19.5 kHz	23.4 kHz
1	0	$f_{CLK}/2^{12}$	976 Hz	1.95 kHz	2.93 kHz	4.88 kHz	5.86 kHz
1	1	$f_{CLK}/2^{14}$	244 Hz	488 Hz	732 Hz	1.22 kHz	1.46 kHz

Note When changing the clock selected for f_{CLK} (by changing the system clock control register (CKC) value), stop timer array unit (TTm = 00FFH).
The timer array unit must also be stopped if the operating clock (f_{MCK}) specified by using the CKSmn0, and CKSmn1 bits or the valid edge of the signal input from the TImn pin is selected as the count clock (f_{TCLK}).

Caution Be sure to clear bits 15, 14, 11, 10 to "0".

By using channels 1 and 3 in the 8-bit timer mode and specifying CKm2 or CKm3 as the operation clock, the interval times shown in Table 7-3 can be achieved by using the interval timer function.

Table 7-3. Interval Times Available for Operation Clock CKSm2 or CKSm3

Clock		Interval time[Note] (f_{CLK} = 20 MHz)			
		16 μs	160 μs	1.6 ms	16 ms
CKm2	$f_{CLK}/2$	√	–	–	–
	$f_{CLK}/2^2$	√	–	–	–
	$f_{CLK}/2^4$	√	√	–	–
	$f_{CLK}/2^6$	√	√	–	–
CKm3	$f_{CLK}/2^8$	–	√	√	–
	$f_{CLK}/2^{10}$	–	√	√	–
	$f_{CLK}/2^{12}$	–	–	√	√
	$f_{CLK}/2^{14}$	–	–	√	√

Note The margin is within 5 %.

Remarks 1. f_{CLK}: CPU/peripheral hardware clock frequency
2. For details of a signal of $f_{CLK}/2^j$ selected with the TPSm register, see **7.5.1 Count clock (f_{TCLK}).**

7.9 Simultaneous Channel Operation Function of Timer Array Unit

7.9.1 Operation as one-shot pulse output function

By using two channels as a set, a one-shot pulse having any delay pulse width can be generated from the signal input to the TImn pin.

The delay time and pulse width can be calculated by the following expressions.

Delay time = {Set value of TDRmn (master) + 2} × Count clock period
Pulse width = {Set value of TDRmp (slave)} × Count clock period

The master channel operates in the one-count mode and counts the delays. Timer count register mn (TCRmn) of the master channel starts operating upon start trigger detection and loads the value of timer data register mn (TDRmn).

The TCRmn register counts down from the value of the TDRmn register it has loaded, in synchronization with the count clock. When TCRmn = 0000H, it outputs INTTMmn and stops counting until the next start trigger is detected.

The slave channel operates in the one-count mode and counts the pulse width. The TCRmp register of the slave channel starts operation using INTTMmn of the master channel as a start trigger, and loads the value of the TDRmp register. The TCRmp register counts down from the value of The TDRmp register it has loaded, in synchronization with the count value. When count value = 0000H, it outputs INTTMmp and stops counting until the next start trigger (INTTMmn of the master channel) is detected. The output level of TOmp becomes active one count clock after generation of INTTMmn from the master channel, and inactive when TCRmp = 0000H.

Instead of using the TImn pin input, a one-shot pulse can also be output using the software operation (TSmn = 1) as a start trigger.

<R> **Caution The timing of loading of timer data register mn (TDRmn) of the master channel is different from that of the TDRmp register of the slave channel. If the TDRmn and TDRmp registers are rewritten during counting, therefore, an illegal waveform may be output in conflict with the timing of loading. Rewrite the TDRmn register after INTTMmn is generated and the TDRmp register after INTTMmp is generated.**

Remark m: Unit number (m = 0), n: Channel number (n = 0, 2, 4, 6)
p: Slave channel number (n < p ≤ 7)

Table 14-3. A/D Conversion Time Selection (2/4)

(2) When there is no A/D power supply stabilization wait time

Low-voltage mode 1, 2 (software trigger mode/hardware trigger no-wait mode)

A/D Converter Mode Register 0 (ADM0)					Mode	Conversion Clock (f_{AD})	Number of Conversion Clock[Note 1]	Conversion Time	Conversion Time Selection at 10-Bit Resolution				
									1.9 V ≤ V_{DD} ≤ 5.5 V			**Note 2**	**Note 3**
FR2	FR1	FR0	LV1	LV0					f_{CLK} = 1 MHz	f_{CLK} = 4 MHz	f_{CLK} = 8 MHz	f_{CLK} = 16 MHz	f_{CLK} = 24 MHz
0	0	0	1	0	Low-voltage 1	f_{CLK}/64	19 f_{AD} (number of sampling clock: 7 f_{AD})	1216/f_{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	
0	0	1				f_{CLK}/32		608/f_{CLK}				38 µs	25.3333 µs
0	1	0				f_{CLK}/16		304/f_{CLK}			38 µs	19 µs	12.6667 µs
0	1	1				f_{CLK}/8		152/f_{CLK}		38 µs	19 µs	9.5 µs	6.3333 µs
1	0	0				f_{CLK}/6		114/f_{CLK}		28.5 µs	14.25 µs	7.125 µs	4.75 µs
1	0	1				f_{CLK}/5		95/f_{CLK}		23.75 µs	11.875 µs	5.938 µs	3.9587 µs
1	1	0				f_{CLK}/4		76/f_{CLK}		19 µs	9.5 µs	4.75 µs	3.1667 µs
1	1	1				f_{CLK}/2		38/f_{CLK}	38 µs	9.5 µs	4.75 µs	2.375 µs	Setting prohibited
0	0	0	1	1	Low-voltage 2	f_{CLK}/64	17 f_{AD} (number of sampling clock: 5 f_{AD})	1088/f_{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	
0	0	1				f_{CLK}/32		544/f_{CLK}				34 µs	22.6667 µs
0	1	0				f_{CLK}/16		272/f_{CLK}			34 µs	17 µs	11.3333 µs
0	1	1				f_{CLK}/8		136/f_{CLK}		34 µs	17 µs	8.5 µs	5.6667 µs
1	0	0				f_{CLK}/6		102/f_{CLK}		25.5 µs	12.75 µs	6.375 µs	4.25 µs
1	0	1				f_{CLK}/5		85/f_{CLK}		21.25 µs	10.625 µs	5.3125 µs	3.5417 µs
1	1	0				f_{CLK}/4		68/f_{CLK}		17 µs	8.5 µs	4.25 µs	2.8333 µs
1	1	1				f_{CLK}/2		34/f_{CLK}	34 µs	8.5 µs	4.25 µs	2.125 µs	Setting prohibited

Notes 1. These are the numbers of clock cycles when conversion is with 10-bit resolution. When eight-bit resolution is selected, the values are shorter by two cycles of the conversion clock (f_{AD}).

2. 2.4 V ≤ V_{DD} ≤ 5.5 V

3. 2.7 V ≤ V_{DD} ≤ 5.5 V

Cautions 1. The A/D conversion time must also be within the relevant range of conversion time (t_{CONV}) described in 37.6.1 A/D converter characteristics.

2. Rewriting the FR2 to FR0, LV1, and LV0 bits to other than the same data while conversion is stopped (ADCS = 0, ADCE = 0).

3. The above conversion time does not include conversion start time. Conversion start time add in the first conversion. Select conversion time, taking clock frequency errors into consideration.

Remark f_{CLK}: CPU/peripheral hardware clock frequency

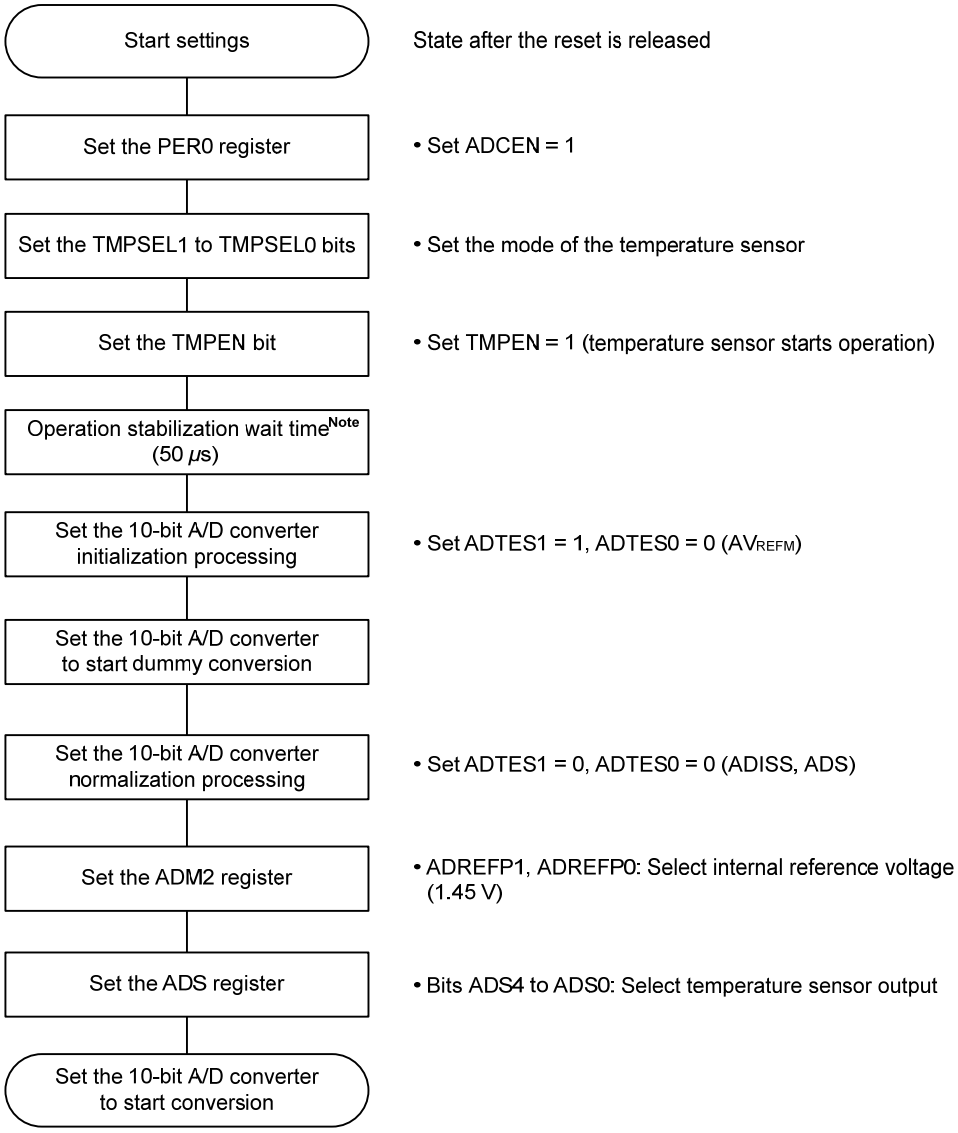
15.3 Setting Procedures

The procedures for setting the temperature sensor are shown below.

15.3.1 A/D converter mode register 0 (ADM0)

Figure 15-4 shows the setting flowchart when starting operation of temperature sensor.

Figure 15-4. Setting Flowchart When Starting Operation of Temperature Sensor



Note Operation stabilization wait time is required until the A/D converter starts conversion.

Caution Select internal reference voltage for 10-bit A/D converter.

(2) Operation procedure

Figure 18-58. Initial Setting Procedure for Slave Reception

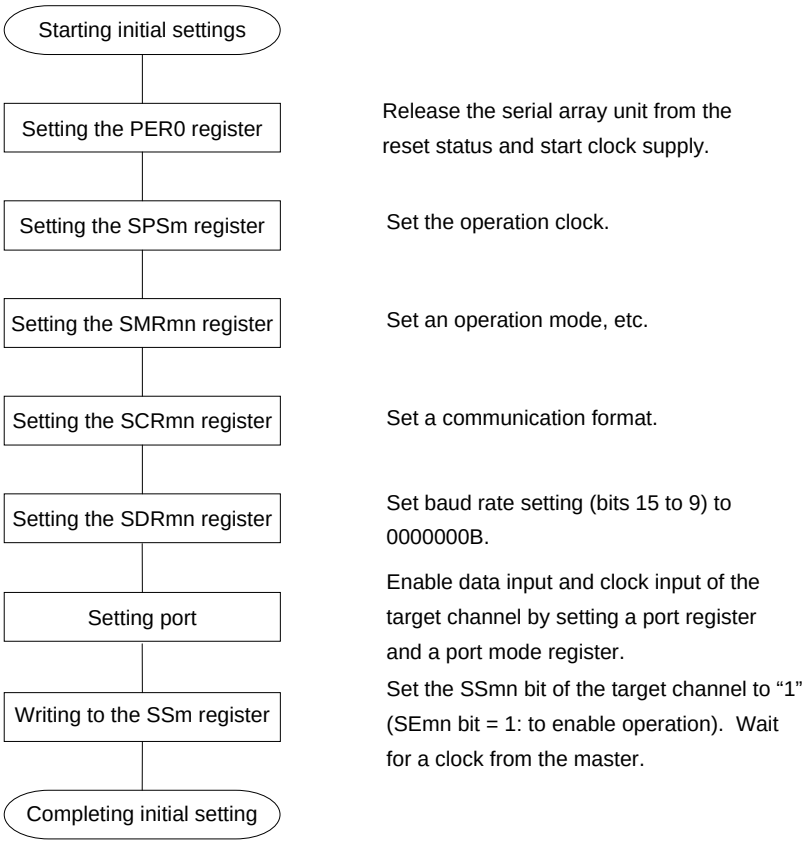
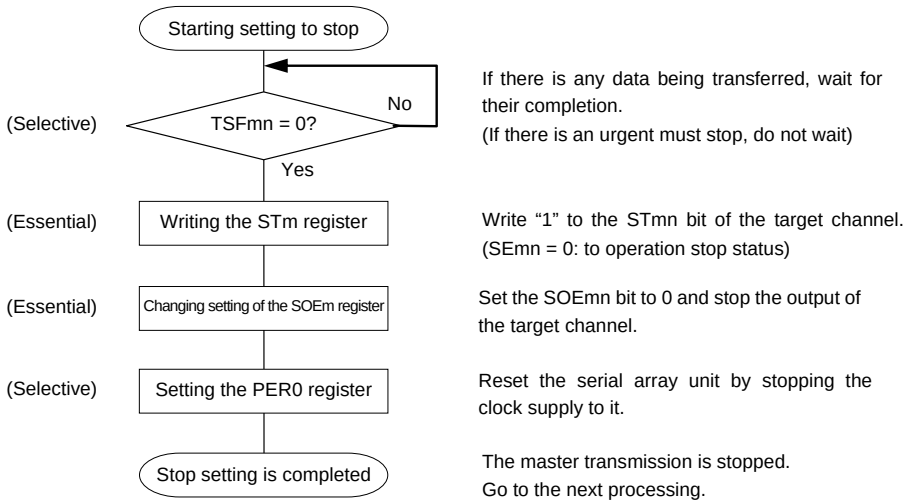
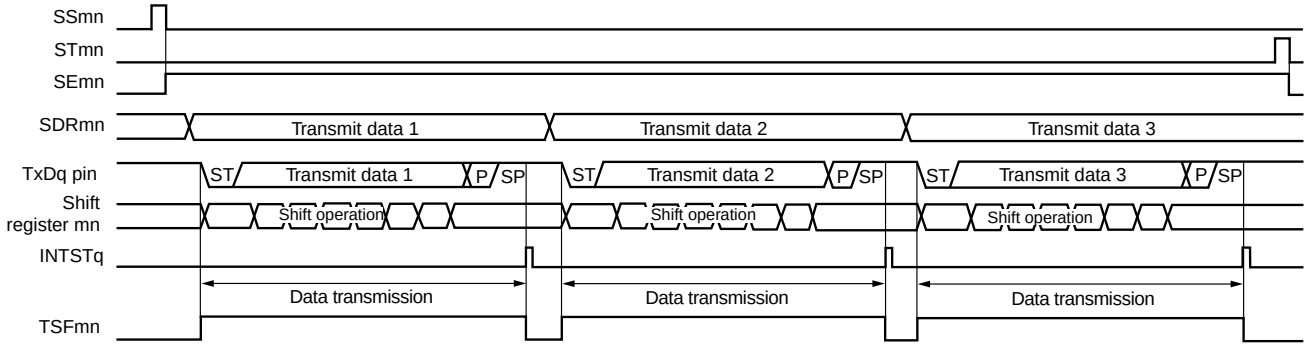


Figure 18-59. Procedure for Stopping Slave Reception



(3) Processing flow (in single-transmission mode)

Figure 18-80. Timing Chart of UART Transmission (in Single-Transmission Mode)



Remark m: Unit number (m = 0, 1), n: Channel number (n = 0, 2), q: UART number (q = 0 to 2)
mn = 00, 02, 10

18.8.5 Calculating transfer rate

The transfer rate for simplified I^2C (IIC00, IIC10) communication can be calculated by the following expressions.

(Transfer rate) = {Operation clock (f_{MCK}) frequency of target channel} ÷ (SDRmn[15:9] + 1) ÷ 2

Caution SDRmn[15:9] must not be set to 00000000B. Be sure to set a value of 00000001B or greater for SDRmn[15:9]. The duty ratio of the SCL signal output by the simplified I^2C is 50%. The I^2C bus specifications define that the low-level width of the SCL signal is longer than the high-level width. If 400 kbps (fast mode) or 1 Mbps (fast mode plus) is specified, therefore, the low-level width of the SCL output signal becomes shorter than the value specified in the I^2C bus specifications. Make sure that the SDRmn[15:9] value satisfies the I^2C bus specifications.

Remarks 1. The value of SDRmn[15:9] is the value of bits 15 to 9 of the SDRmn register (0000001B to 1111111B) and therefore is 1 to 127.

2. m: Unit number (m = 0), n: Channel number (n = 0, 2), mn = 00, 02

The operation clock (f_{MCK}) is determined by serial clock select register m (SPSm) and bit 15 (CKSmn) of serial mode register mn (SMRmn).

CHAPTER 19 SERIAL INTERFACE IICA

19.1 Functions of Serial Interface IICA

Serial interface IICA has the following three modes.

(1) Operation stop mode

This mode is used when serial transfers are not performed. It can therefore be used to reduce power consumption.

(2) I^2C bus mode (multimaster supported)

This mode is used for 8-bit data transfers with several devices via two lines: a serial clock (SCLAn) line and a serial data bus (SDAAn) line.

This mode complies with the I^2C bus format and the master device can generated “start condition”, “address”, “transfer direction specification”, “data”, and “stop condition” data to the slave device, via the serial data bus. The slave device automatically detects these received status and data by hardware. This function can simplify the part of application program that controls the I^2C bus.

Since the SCLAn and SDAAn pins are used for open drain outputs, serial interface IICA requires pull-up resistors for the serial clock line and the serial data bus line.

(3) Wakeup mode

The STOP mode can be released by generating an interrupt request signal (INTIICAn) when an extension code from the master device or a local address has been received while in STOP mode. This can be set by using the WUPn bit of IICA control register n1 (IICCTLn1).

Figure 19-1 shows a block diagram of serial interface IICA.

Remark n = 0

19.5.13 Wakeup function

The I^2C bus slave function is a function that generates an interrupt request signal (INTIICAn) when a local address and extension code have been received.

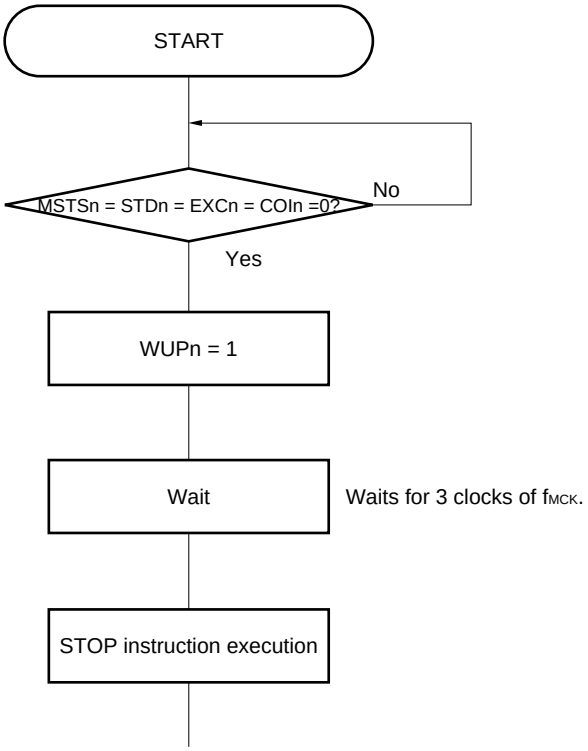
This function makes processing more efficient by preventing unnecessary INTIICAn signal from occurring when addresses do not match.

When a start condition is detected, wakeup standby mode is set. This wakeup standby mode is in effect while addresses are transmitted due to the possibility that an arbitration loss may change the master device (which has generated a start condition) to a slave device.

To use the wakeup function in the STOP mode, set the WUPn bit to 1. Addresses can be received regardless of the operation clock. An interrupt request signal (INTIICAn) is also generated when a local address and extension code have been received. Operation returns to normal operation by using an instruction to clear (0) the WUPn bit after this interrupt has been generated.

Figure 19-22 shows the flow for setting WUPn = 1 and Figure 19-23 shows the flow for setting WUPn = 0 upon an address match.

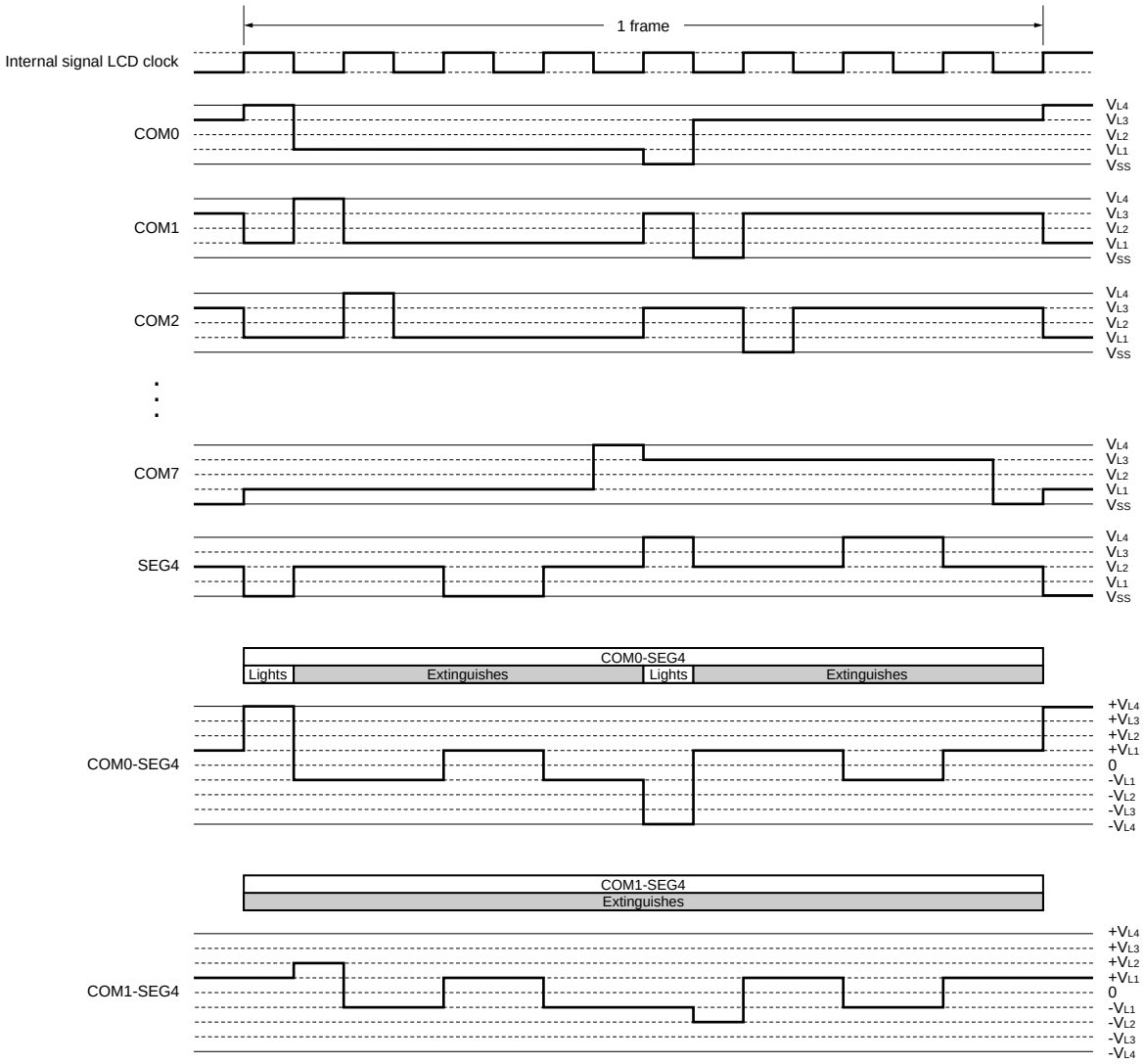
Figure 19-22. Flow When Setting WUPn = 1



Remark n = 0

Figure 21-43. Eight-Time-Slice LCD Drive Waveform Examples Between SEG4 and Each Common Signals (1/4 Bias Method) (2/2)

(b) Waveform B



23.3.3 Priority specification flag registers (PR00L, PR00H, PR01L, PR01H, PR02L, PR02H, PR03L, PR10L, PR10H, PR11L, PR11H, PR12L, PR12H, PR13L)

The priority specification flag registers are used to set the corresponding maskable interrupt priority level.

A priority level is set by using the PR0xy and PR1xy registers in combination (xy = 0L, 0H, 1L, 1H, 2L, or 2H).

The PR00L, PR00H, PR01L, PR01H, PR02L, PR02H, PR03L, PR10L, PR10H, PR11L, PR11H, PR12L, PR12H, and the PR13L registers can be set by a 1-bit or 8-bit memory manipulation instruction. If the PR00L and PR00H registers, the PR01L and PR01H registers, the PR02L and PR02H registers, the PR10L and PR10H registers, the PR11L and PR11H registers, and the PR12L and PR12H registers are combined to form 16-bit registers PR00, PR01, PR02, PR10, PR11, and PR12, they can be set by a 16-bit memory manipulation instruction.

Reset signal generation sets these registers to FFH.

Remark If an instruction that writes data to this register is executed, the number of instruction execution clocks increases by 2 clocks.

Figure 23-4. Format of Priority Specification Flag Registers (PR00L, PR00H, PR01L, PR01H, PR02L, PR02H, PR03L, PR10L, PR10H, PR11L, PR11H, PR12L, PR12H, PR13L) (1/2)

Address: FFFE8H After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
PR00L	PPR05	PPR04	PPR03	PPR02	PPR01	PPR00	LVIPR0	WDTIPR0

Address: FFFECH After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
PR10L	PPR15	PPR14	PPR13	PPR12	PPR11	PPR10	LVIPR1	WDTIPR1

Address: FFFE9H After reset: FFH R/W

Symbol	<7>	<6>	<5>	4	3	<2>	<1>	<0>
PR00H	SRPR00	TMPR000	STPR00 CSIPR000 IICPR000	1	1	SREPR02	SRPR02	STPR02

Address: FFFEDH After reset: FFH R/W

Symbol	<7>	<6>	<5>	4	3	<2>	<1>	<0>
PR10H	SRPR10	TMPR100	STPR10 CSIPR100 IICPR100	1	1	SREPR12	SRPR12	STPR12

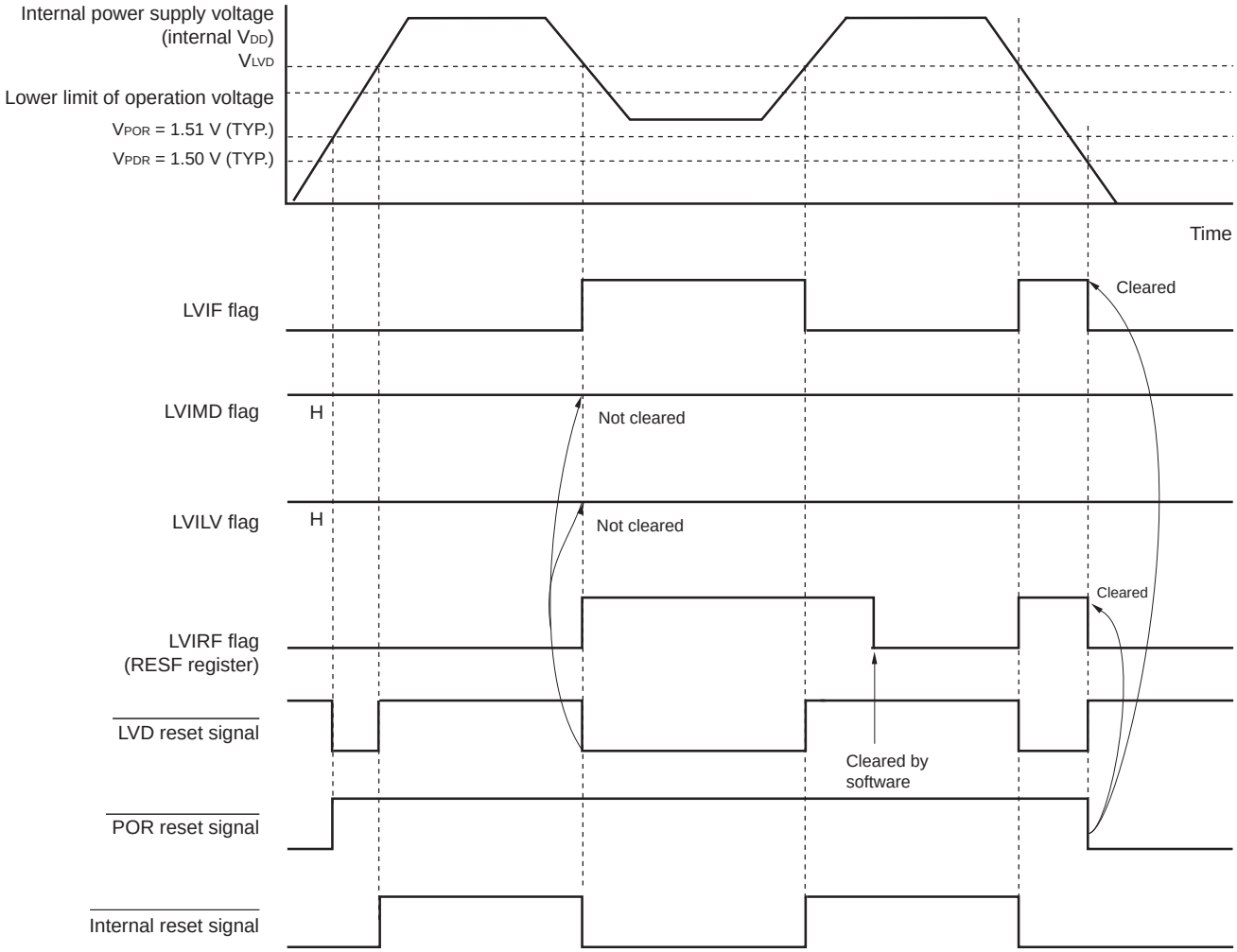
Address: FFFEAH After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
PR01L	TMPR001	FMPR0	RTITPR0	IICAPR00	SREPR01 TMPR003H	SRPR01	STPR01 IICPR010	SREPR00 TMPR001H

Address: FFFEEH After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
PR11L	TMPR101	FMPR1	RTITPR1	IICAPR10	SREPR11 TMPR103H	SRPR11	STPR11 IICPR110	SREPR10 TMPR101H

Figure 27-5. Timing of Voltage Detector Internal Reset Signal Generation (Option Byte LVIMDS1, LVIMDS0 = 1, 1)



Remark V_{POR}: POR power supply rise detection voltage
V_{PDR}: POR power supply fall detection voltage

33.4.2 Flash memory programming mode

To rewrite the contents of the code flash memory through serial programming, specify the flash memory programming mode. To enter the mode, set as follows.

<Serial programming using the dedicated flash memory programmer >

Connect the RL78 microcontroller to a dedicated flash memory programmer. Communication from the dedicated flash memory programmer is performed to automatically switch to the flash memory programming mode.

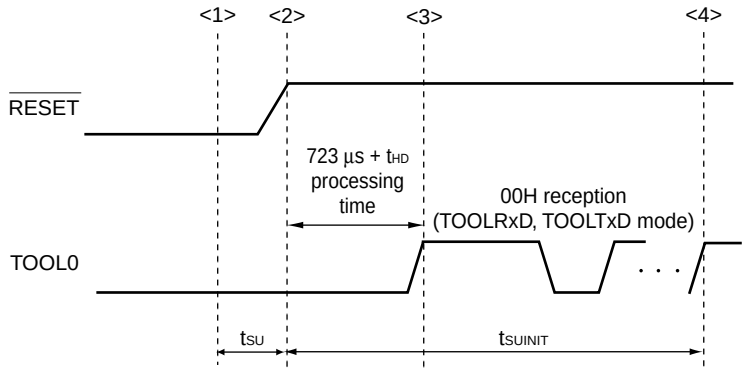
<Serial programming using an external device (UART communication)>

Set the TOOL0 pin to the low level, and then cancel the reset (see **Table 33-4**). After that, enter flash memory programming mode according to the procedures <1> to <4> shown in **Figure 33-7**. For details, refer to the **RL78 Microcontrollers (RL78 Protocol A) Programmer Edition Application Note (R01AN0815)**.

Table 33-4. Relationship Between TOOL0 Pin and Operation Mode After Reset Release

TOOL0	Operation Mode
EV_{DD}	Normal operation mode
0	Flash memory programming mode

Figure 33-7. Setting of Flash Memory Programming Mode



<1> The low level is input to the TOOL0 pin.

<2> The pins reset ends (POR and LVD reset must end before the pin reset ends.).

<3> The TOOL0 pin is set to the high level.

<4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

Remark t_{SUINIT}: The segment shows that it is necessary to finish specifying the initial communication settings within 100 ms from when the resets end.

t_{SU}: How long from when the TOOL0 pin is placed at the low level until a pin reset ends

t_{HD}: How long to keep the TOOL0 pin at the low level from when the external and internal resets end (the flash firmware processing time is excluded)

For details, see **37.12 Timing Specs for Switching Flash Memory Programming Modes**.

36.1.2 Description of operation column

The operation when the instruction is executed is shown in the “Operation” column using the following symbols.

Table 36-2. Symbols in “Operation” Column

Symbol	Function
A	A register; 8-bit accumulator
X	X register
B	B register
C	C register
D	D register
E	E register
H	H register
L	L register
ES	ES register
CS	CS register
AX	AX register pair; 16-bit accumulator
BC	BC register pair
DE	DE register pair
HL	HL register pair
PC	Program counter
SP	Stack pointer
PSW	Program status word
CY	Carry flag
AC	Auxiliary carry flag
Z	Zero flag
RBS	Register bank select flag
IE	Interrupt request enable flag
()	Memory contents indicated by address or register contents in parentheses
X_H, X_L X_S, X_H, X_L	16-bit registers: X_H = higher 8 bits, X_L = lower 8 bits 20-bit registers: X_S = (bits 19 to 16), X_H = (bits 15 to 8), X_L = (bits 7 to 0)
∧	Logical product (AND)
∨	Logical sum (OR)
∀	Exclusive logical sum (exclusive OR)
¯	Inverted data
addr5	16-bit immediate data (even addresses only in 0080H to 00BFH)
addr16	16-bit immediate data
addr20	20-bit immediate data
jdisp8	Signed 8-bit data (displacement value)
jdisp16	Signed 16-bit data (displacement value)

Notes 1. Total current flowing into V_{DD} and EV_{DD}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, EV_{DD} or V_{SS}, EV_{SS}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the LCD controller/driver, A/D converter, ΔΣ A/D converter, LVD circuit, comparator, battery backup circuit, I/O port, and on-chip pull-up/pull-down resistors. When the VBAT pin (pin for battery backup) is selected, current flowing into VBAT.

2. When high-speed on-chip oscillator and subsystem clock are stopped.

3. When high-speed system clock and subsystem clock are stopped.

4. When high-speed on-chip oscillator and high-speed system clock are stopped. When setting ultra-low current consumption (AMPHS1 = 1). However, not including the current flowing into real-time clock 2, 12-bit interval timer, and watchdog timer.

5. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: $2.7\ V \leq V_{DD} \leq 5.5\ V$@1 MHz to 24 MHz

$2.4\ V \leq V_{DD} \leq 5.5\ V$@1 MHz to 16 MHz

LS (low-speed main) mode: $1.9\ V \leq V_{DD} \leq 5.5\ V$@1 MHz to 8 MHz

Remarks 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

2. f_{IH}: High-speed on-chip oscillator clock frequency

3. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

4. Except subsystem clock operation, temperature condition of the TYP. value is $T_A = 25°C$

(4/6)

Edition	Description	Chapter
Rev.1.00	Change of **37.1 Absolute Maximum Ratings**	**CHAPTER 37 ELECTRICAL SPECIFICATIONS**
	Change of **37.2 Oscillator Characteristics**	
	Change of **37.3 DC Characteristics**	
	Change of **37.4 AC Characteristics**	
	Change of **37.5 Peripheral Functions Characteristics**	
	Change of **37.6 Analog Characteristics**	
	Change of **37.7 Battery Backup Function**	
	Change of **37.8 LCD Characteristics**	
	Addition of **37.11 Dedicated Flash Memory Programmer Communication (UART)**	
	Change of **37.12 Timing Specs for Switching Flash Memory Programming Modes**	
Rev.2.00	Change of high accuracy RTC to RTC2, and high accuracy real-time clock to real-time clock 2	Throughout
	Change of high accuracy temperature sensor to temperature sensor 2	
	Modification of **1.1 Features**	**CHAPTER 1 OUTLINE**
	Modification of **1.2 List of Part Numbers**	
	Modification of **1.3 Pin Configuration (Top View)**	
	Modification of **2.1 Port Function List**	**CHAPTER 2 PIN FUNCTIONS**
	Modification of **2.2 Functions Other than Port Pins**	
	Modification of **2.3 Connection of Unused Pins**	
	Addition of **2.4 Block Diagrams of Pins**	
	Modification of **3.1 Memory Space**	**CHAPTER 3 CPU ARCHITECTURE**
	Modification of **3.2 Processor Registers**	
	Modification of **3.3 Instruction Address Addressing**	
	Modification of **3.4 Addressing for Processing Data Addresses**	
	Modification of **4.2 Port Configuration**	**CHAPTER 4 PORT FUNCTIONS**
	Modification of **4.3 Registers Controlling Port Function**	
	Modification of **4.4 Port Function Operations**	
	Modification of **4.5 Register Settings When Using Alternate Function**	
	Modification of **4.6 Cautions When Using Port Function**	
	Modification of **5.3 Registers Controlling Clock Generator**	**CHAPTER 5 CLOCK GENERATOR**
	Modification of **5.4 System Clock Oscillator**	
	Modification of **5.6 Controlling the Clock**	
	Addition of **5.7 Resonator and Oscillator Constants**	
	Modification of **7.2 Configuration of Timer Array Unit**	**CHAPTER 7 TIMER ARRAY UNIT**
	Modification of **7.3 Registers Controlling Timer Array Unit**	
	Modification of **7.5 Operation of Counter**	
	Modification of **7.6 Channel Output (TOmn Pin) Control**	
	Addition of **7.7 Timer Input (TImn) Control**	
	Modification of **7.8 Independent Channel Operation Function of Timer Array Unit**	
	Modification of **7.9 Simultaneous Channel Operation Function of Timer Array Unit**	
	Modification of **8.1 Functions of Real-time Clock 2**	**CHAPTER 8 REAL-TIME CLOCK 2**
	Modification of **8.2 Configuration of Real-time Clock 2**	
	Modification of **8.3 Registers Controlling Real-time Clock 2**	
	Modification of **8.4 Real-time Clock 2 Operation**	