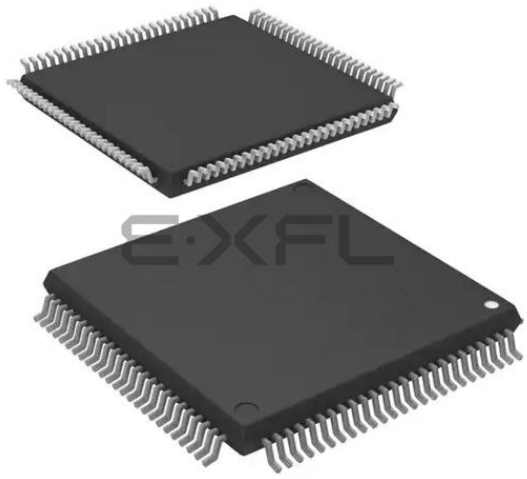

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	RL78
Core Size	16-Bit
Speed	24MHz
Connectivity	CSI, I²C, IrDA, LINbus, UART/USART
Peripherals	Brown-out Detect/Reset, LCD, LVD, POR, PWM, WDT
Number of I/O	69
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	1.9V ~ 5.5V
Data Converters	A/D 6x10b, 4x24b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f10mpedfb-50

NOTES FOR CMOS DEVICES

(1) VOLTAGE APPLICATION WAVEFORM AT INPUT PIN: Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between VIL (MAX) and VIH (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (MAX) and VIH (MIN).

(2) HANDLING OF UNUSED INPUT PINS: Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

(3) PRECAUTION AGAINST ESD: A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

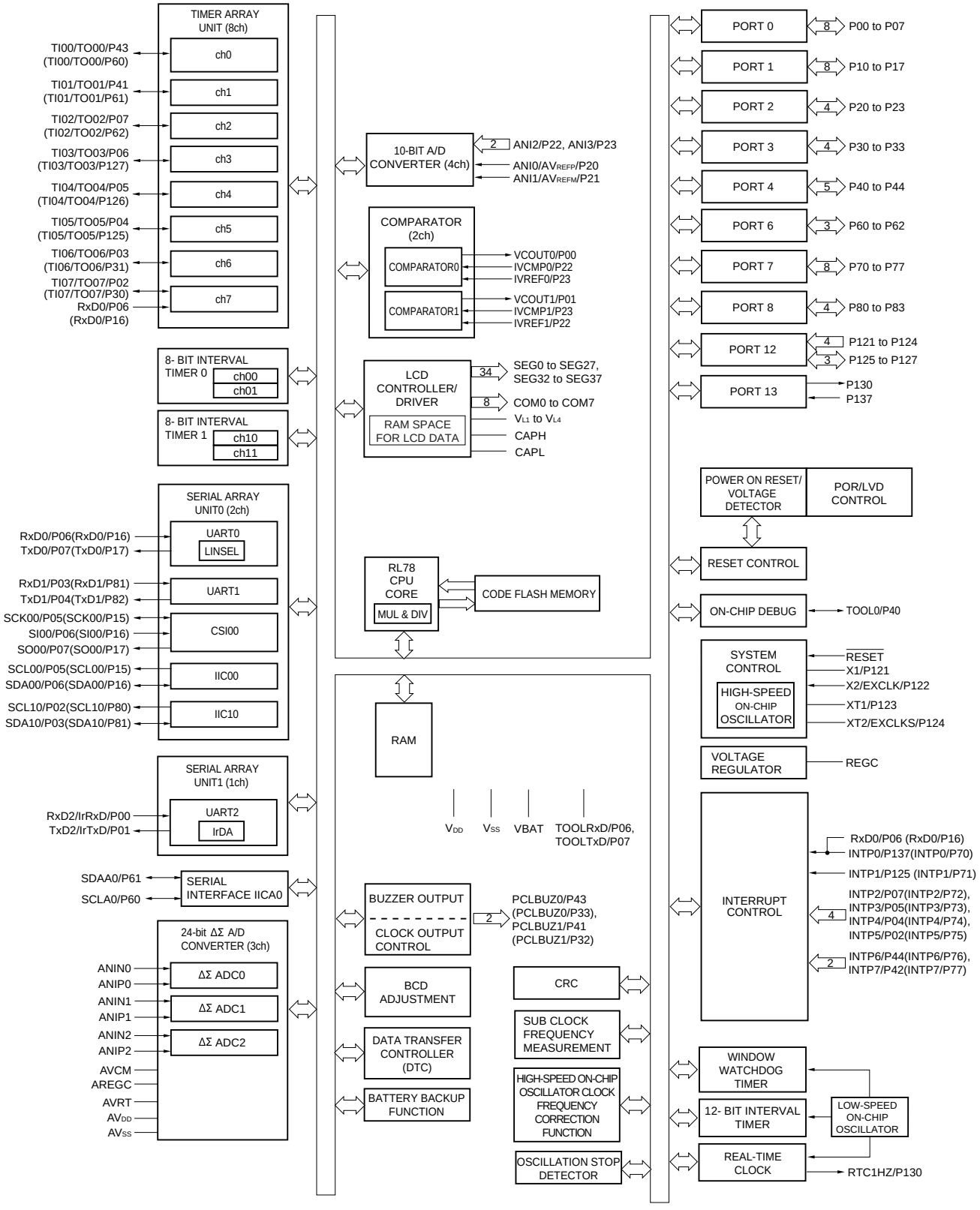
(4) STATUS BEFORE INITIALIZATION: Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

(5) POWER ON/OFF SEQUENCE: In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

(6) INPUT OF SIGNAL DURING POWER OFF STATE : Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

1.5 Block Diagram

1.5.1 80-pin products



Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). See **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)**.

3.1.2 Mirror area

The RL78/I1B mirrors the code flash area of 00000H to 0FFFFH, to F0000H to FFFFFH. The products with 128 KB flash memory mirror the code flash area of 00000H to 0FFFFH or 10000H to 1FFFFH, to F0000H to FFFFFH (the code flash area to be mirrored is set by the processor mode control register (PMC)).

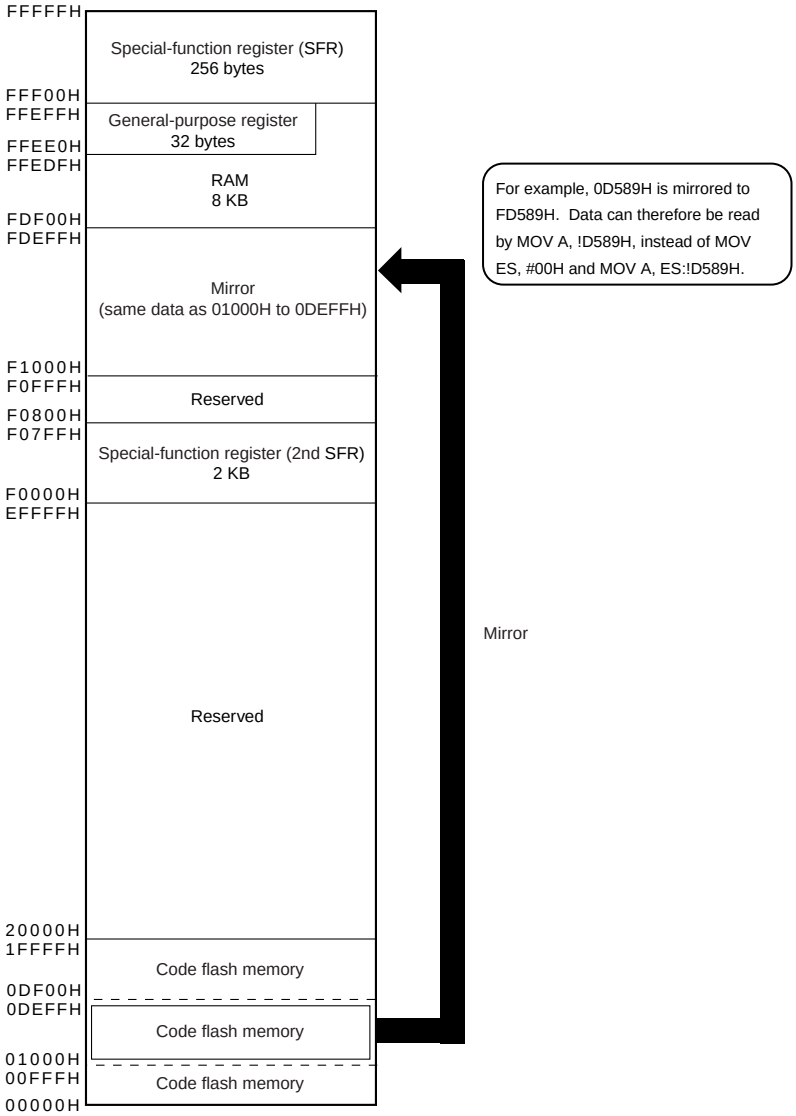
By reading data from F0000H to FFFFFH, an instruction that does not have the ES register as an operand can be used, and thus the contents of the code flash can be read with the shorter code. However, the code flash area is not mirrored to the SFR, extended SFR, RAM, and use prohibited areas.

See **3.1 Memory Space** for the mirror area of each product.

The mirror area can only be read and no instruction can be fetched from this area.

The following show examples.

Example R5F10MMG, R5F10MPG (Flash memory: 128 KB, RAM: 8 KB)



The PMC register is described below.

Table 3-5. SFR List (3/5)

Address	Special Function Register (SFR) Name	Symbol	R/W	Manipulable Bit Range			After Reset
				1-bit	8-bit	16-bit	
FFF90H FFF91H	12-bit interval timer control register	ITMC	R/W	–	–	√	0FFFH
FFF92H	Second count register	SEC	R/W	–	√	–	Undefined
FFF93H	Minute count register	MIN	R/W	–	√	–	Undefined
FFF94H	Hour count register	HOUR	R/W	–	√	–	Undefined
FFF95H	Week count register	WEEK	R/W	–	√	–	Undefined
FFF96H	Day count register	DAY	R/W	–	√	–	Undefined
FFF97H	Month count register	MONTH	R/W	–	√	–	Undefined
FFF98H	Year count register	YEAR	R/W	–	√	–	Undefined
FFF9AH	Alarm minute register	ALARMWM	R/W	–	√	–	Undefined
FFF9BH	Alarm hour register	ALARMWH	R/W	–	√	–	Undefined
FFF9CH	Alarm week register	ALARMWW	R/W	–	√	–	Undefined
FFF9DH	Real-time clock control register 0	RTCC0	R/W	√	√	–	00H Note 1
FFF9EH	Real-time clock control register 1	RTCC1	R/W	√	√	–	00H Note 1
FFFA0H	Clock operation mode control register	CMC	R/W	–	√	–	00H Note 1
FFFA1H	Clock operation status control register	CSC	R/W	√	√	–	C0H Note 1
FFFA2H	Oscillation stabilization time counter status register	OSTC	R	√	√	–	00H
FFFA3H	Oscillation stabilization time select register	OSTS	R/W	–	√	–	07H
FFFA4H	System clock control register	CKC	R/W	√	√	–	00H
FFFA5H	Clock output select register 0	CKS0	R/W	√	√	–	00H
FFFA6H	Clock output select register 1	CKS1	R/W	√	√	–	00H
FFFA8H	Reset control flag register	RESF	R	–	√	–	Undefined Note 2
FFFA9H	Voltage detection register	LVIM	R/W	√	√	–	00H Note 2
FFFAAH	Voltage detection level register	LVIS	R/W	√	√	–	00H/01H/81H Note 2
FFFABH	Watchdog timer enable register	WDTE	R/W	–	√	–	1AH/9AH Note 3
FFFACH	CRC input register	CRCIN	R/W	–	√	–	00H

Notes 1. This register is reset only by a power-on reset.

2. The reset values of the registers vary depending on the reset source as shown below.

Register \ Reset Source		$\overline{\text{RESET}}$ Input	Reset by POR	Reset by Execution of Illegal Instruction	Reset by WDT	Reset by RAM Parity Error	Reset by Illegal-Memory Access	Reset by LVD
RESF	TRAP	Cleared (0)		Set (1)	Held			Held
	WDTRF			Held	Set (1)	Held		
	RPERF			Held		Set (1)	Held	
	IAWRF			Held			Set (1)	
	LVIRF			Held				Set (1)
LVIM	LVISEN	Cleared (0)						Held
	LVIOMSK	Held						
	LVIF							
LVIS		Cleared (00H/01H/81H)						Clear (00H/81H) Note 4

3. The reset value of the WDTE register is determined by the setting of the option byte.

4. When option byte LVIMDS1, LVIMDS0 = 0, 1: LVD reset is not generated.

Table 3-6. Extended SFR (2nd SFR) List (8/8)

Address	Special Function Register (SFR) Name	Symbol		R/W	Manipulable Bit Range			After Reset
					1-bit	8-bit	16-bit	
F040BH	LCD display data memory 11	SEG11		R/W	–	√	–	00H
F040CH	LCD display data memory 12	SEG12		R/W	–	√	–	00H
F040DH	LCD display data memory 13	SEG13		R/W	–	√	–	00H
F040EH	LCD display data memory 14	SEG14		R/W	–	√	–	00H
F040FH	LCD display data memory 15	SEG15		R/W	–	√	–	00H
F0410H	LCD display data memory 16	SEG16		R/W	–	√	–	00H
F0411H	LCD display data memory 17	SEG17		R/W	–	√	–	00H
F0412H	LCD display data memory 18	SEG18		R/W	–	√	–	00H
F0413H	LCD display data memory 19	SEG19		R/W	–	√	–	00H
F0414H	LCD display data memory 20	SEG20		R/W	–	√	–	00H
F0415H	LCD display data memory 21	SEG21		R/W	–	√	–	00H
F0416H	LCD display data memory 22	SEG22		R/W	–	√	–	00H
F0417H	LCD display data memory 23	SEG23		R/W	–	√	–	00H
F0418H	LCD display data memory 24	SEG24		R/W	–	√	–	00H
F0419H	LCD display data memory 25	SEG25		R/W	–	√	–	00H
F041AH	LCD display data memory 26	SEG26		R/W	–	√	–	00H
F041BH	LCD display data memory 27	SEG27		R/W	–	√	–	00H
F041CH	LCD display data memory 28	SEG28		R/W	–	√	–	00H
F041DH	LCD display data memory 29	SEG29		R/W	–	√	–	00H
F041EH	LCD display data memory 30	SEG30		R/W	–	√	–	00H
F041FH	LCD display data memory 31	SEG31		R/W	–	√	–	00H
F0420H	LCD display data memory 32	SEG32		R/W	–	√	–	00H
F0421H	LCD display data memory 33	SEG33		R/W	–	√	–	00H
F0422H	LCD display data memory 34	SEG34		R/W	–	√	–	00H
F0423H	LCD display data memory 35	SEG35		R/W	–	√	–	00H
F0424H	LCD display data memory 36	SEG36		R/W	–	√	–	00H
F0425H	LCD display data memory 37	SEG37		R/W	–	√	–	00H
F0426H	LCD display data memory 38	SEG38		R/W	–	√	–	00H
F0427H	LCD display data memory 39	SEG39		R/W	–	√	–	00H
F0428H	LCD display data memory 40	SEG40		R/W	–	√	–	00H
F0429H	LCD display data memory 41	SEG41		R/W	–	√	–	00H
F0540H	8-bit interval timer count register 00	TRT00	TRT0	R	–	√	√	00H
F0541H	8-bit interval timer count register 01	TRT01		R	–	√		00H
F0548H	8-bit interval timer count register 10	TRT10	TRT1	R	–	√	√	00H
F0549H	8-bit interval timer count register 11	TRT11		R	–	√		00H

Remark For SFRs in the SFR area, see **Table 3-5 SFR List**.

11.3.6 8-bit interval timer division register n (TRTMDn) (n = 0 or 1)

This register is used to select the division ratio of the count source used by the 8-bit interval timer.

The TRTMDn register can be set by an 8-bit memory manipulation instruction.

Reset signal generation sets this register to 00H.

Figure 11-7. Format of 8-bit Interval Timer Division Register n (TRTMDn)

Address: F0353H (TRTMD0), F035BH (TRTMD1) After reset: 00H R/W[Note 4]

Symbol	7	6	5	4	3	2	1	0
TRTMDn	0	TCKn1			0	TCKn0		

TCKn1			Selection of division ratio for 8-bit interval timer 1[Notes 1, 2, 3]
Bit 6	Bit 5	Bit 4	
0	0	0	f_{SUB}
0	0	1	$f_{SUB}/2$
0	1	0	$f_{SUB}/4$
0	1	1	$f_{SUB}/8$
1	0	0	$f_{SUB}/16$
1	0	1	$f_{SUB}/32$
1	1	0	$f_{SUB}/64$
1	1	1	$f_{SUB}/128$
In 8-bit interval timer mode, TRTn1 counts based on the count clock specified by TCKn1. In 16-bit interval timer mode, set these bits to 000B because they are not used. See **11.4 Operation** for details.			

TCKn0			Selection of division ratio for 8-bit interval timer 0[Notes 1, 2, 3]
Bit 2	Bit 1	Bit 0	
0	0	0	f_{SUB}
0	0	1	$f_{SUB}/2$
0	1	0	$f_{SUB}/4$
0	1	1	$f_{SUB}/8$
1	0	0	$f_{SUB}/16$
1	0	1	$f_{SUB}/32$
1	1	0	$f_{SUB}/64$
1	1	1	$f_{SUB}/128$
In 8-bit interval timer mode, TRTn0 counts based on the count clock specified by TCKn0. In 16-bit interval timer mode, TRTn counts based on the count clock specified by TCKn0. See **11.4 Operation** for details.			

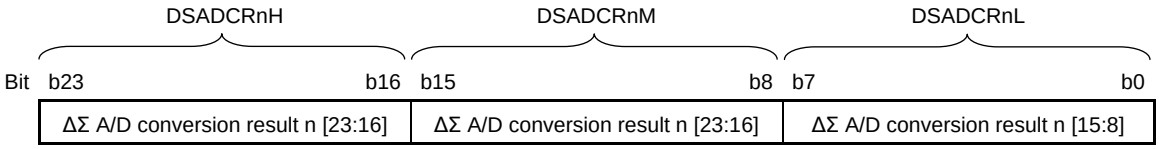
Notes 1. Do not switch the count source during counting. When switching the count source, set these bits while the TSTARTni bit in the TRTCRn register is 0 (counting is stopped).

2. Set TCKni (i = 0, 1) of the unused channel to 000B.

3. Be sure to set the TCKni (i = 0, 1) bit before setting the TRTCMPni register.

4. Bits 7 and 3 are read-only. When writing, write 0. When reading, 0 is read.

- When 16-bit resolution is set (DSADTYP in the DSADMR register = 1)



Bit	Symbol	Conversion result of channel n
b7 to b0	DSADCRnL [7:0]	Conversion result bits 15 to 8 of channel n
b15 to b8	DSADCRnM [7:0]	Conversion result bits 23 to 16 of channel n
b23 to b16	DSADCRnH [7:0]	Conversion result bits 23 to 16 of channel n

Caution Be sure to read the ΔΣ A/D converter conversion result register within its maximum pending time after the ΔΣ A/D conversion end interrupt is generated.

18.3.5 Serial data register mn (SDRmn)

<R> The SDRmn register is the transmit/receive data register (16 bits) of channel n. Bits 8 to 0 (lower 9 bits) of SDR00, SDR01, SDR10 and SDR11 or bits 7 to 0 (lower 8 bits) of SDR02 and SDR03 function as a transmit/receive buffer register, and bits 15 to 9 (higher 7 bits) are used as a register that sets the division ratio of the operation clock (f_{MCK}).

If the CCSmn bit of serial mode register mn (SMRmn) is cleared to 0, the clock set by dividing the operating clock by bits 15 to 9 (higher 7 bits) of the SDRmn register is used as the transfer clock.

If the CCSmn bit of serial mode register mn (SMRmn) is set to 1, set bits 15 to 9 (upper 7 bits) of SDR00 to 0000000B. The input clock f_{SCK} (slave transfer in CSI mode) from the SCKp pin is used as the transfer clock.

The lower 8/9 bits of the SDRmn register function as a transmit/receive buffer register. During reception, the parallel data converted by the shift register is stored in the lower 8/9 bits, and during transmission, the data to be transmitted to the shift register is set to the lower 8/9 bits.

The SDRmn register can be read or written in 16-bit units.

However, the higher 7 bits can be written or read only when the operation is stopped (SEmn = 0). During operation (SEmn = 1), a value is written only to the lower 8/9 bits of the SDRmn register. When the SDRmn register is read during operation, the higher 7 bits are always read as 0.

Reset signal generation clears the SDRmn register to 0000H.

Figure 18-9. Format of Serial Data Register mn (SDRmn)

Address: FFF10H, FFF11H (SDR00), FFF12H, FFF13H (SDR01) After reset: 0000H R/W

	FFF11H (SDR00)								FFF10H (SDR00)							
Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SDRmn								0								

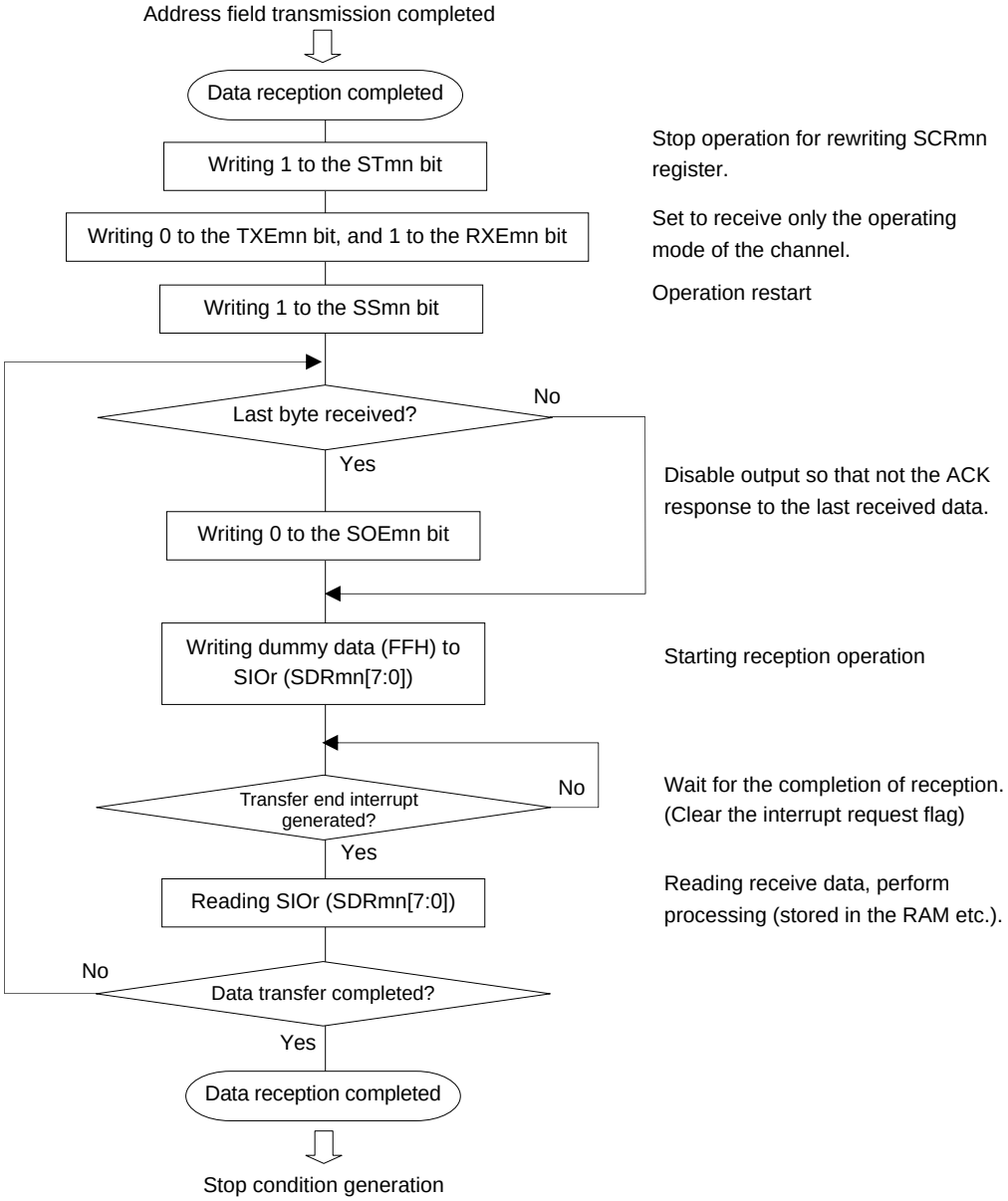
Address: FFF44H, FFF45H (SDR02), FFF46H, FFF47H (SDR03) After reset: 0000H R/W
FFF48H, FFF49H (SDR10), FFF4AH, FFF4BH (SDR11)

	FFF45H (SDR02)								FFF44H (SDR02)							
Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SDRmn								0								

SDRmn[15:9]							Transfer clock setting by dividing the operating clock (f_{MCK})
0	0	0	0	0	0	0	f_{MCK}/2
0	0	0	0	0	0	1	f_{MCK}/4
0	0	0	0	0	1	0	f_{MCK}/6
0	0	0	0	0	1	1	f_{MCK}/8
• • •	• • •	• • •	• • •	• • •	• • •	• • •	• • •
1	1	1	1	1	1	0	f_{MCK}/254
1	1	1	1	1	1	1	f_{MCK}/256

(**Cautions** and **Remarks** are listed on the next page.)

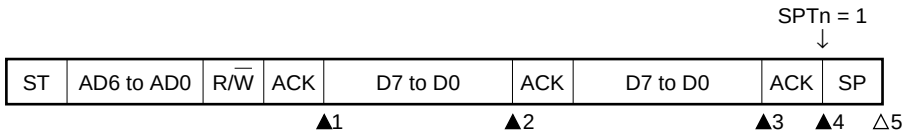
Figure 18-112. Flowchart of Data Reception



Caution ACK is not output when the last data is received (NACK). Communication is then completed by setting "1" to the STmn bit of serial channel stop register m (STm) to stop operation and generating a stop condition.

(c) Start ~ Code ~ Data ~ Data ~ Stop (extension code transmission)

(i) When WTIMn = 0

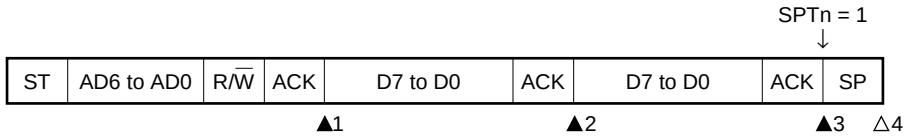


▲1: IICSn = 1010×110B
▲2: IICSn = 1010×000B
▲3: IICSn = 1010×000B (Sets the WTIMn bit to 1)[Note]
▲4: IICSn = 1010××00B (Sets the SPTn bit to 1)
△5: IICSn = 00000001B

Note To generate a stop condition, set the WTIMn bit to 1 and change the timing for generating the INTIICAn interrupt request signal.

Remark ▲: Always generated
△: Generated only when SPIEn = 1
×: Don't care

(ii) When WTIMn = 1



▲1: IICSn = 1010×110B
▲2: IICSn = 1010×100B
▲3: IICSn = 1010××00B (Sets the SPTn bit to 1)
△4: IICSn = 00001001B

Remark ▲: Always generated
△: Generated only when SPIEn = 1
×: Don't care

Remark n = 0

The meanings of <8> to <19> in (3) Data ~ data ~ stop condition in Figure 19-33 are explained below.

<8> The master device sets a wait status (SCLAn = 0) at the falling edge of the 8th clock, and issues an interrupt (INTIICAn: end of transfer). Because of ACKEn = 0 in the master device, the master device then sends an ACK by hardware to the slave device.

<9> The master device reads the received data and releases the wait status (WRELn = 1).

<10> The ACK is detected by the slave device (ACKDn = 1) at the rising edge of the 9th clock.

<11> The slave device set a wait status (SCLAn = 0) at the falling edge of the 9th clock, and the slave device issue an interrupt (INTIICAn: end of transfer).

<12> By the slave device writing the data to transmit to the IICA register, the wait status set by the slave device is released. The slave device then starts transferring data to the master device.

<13> The master device issues an interrupt (INTIICAn: end of transfer) at the falling edge of the 8th clock, and sets a wait status (SCLAn = 0). Because ACK control (ACKEn = 1) is performed, the bus data line is at the low level (SDAAn = 0) at this stage.

<14> The master device sets NACK as the response (ACKEn = 0) and changes the timing at which it sets the wait status to the 9th clock (WTIMn = 1).

<15> If the master device releases the wait status (WRELn = 1), the slave device detects the NACK (ACK = 0) at the rising edge of the 9th clock.

<16> The master device and slave device set a wait status (SCLAn = 0) at the falling edge of the 9th clock, and both the master device and slave device issue an interrupt (INTIICAn: end of transfer).

<17> When the master device issues a stop condition (SPTn = 1), the bus data line is cleared (SDAAn = 0) and the master device releases the wait status. The master device then waits until the bus clock line is set (SCLAn = 1).

<18> The slave device acknowledges the NACK, halts transmission, and releases the wait status (WRELn = 1) to end communication. Once the slave device releases the wait status, the bus clock line is set (SCLAn = 1).

<19> Once the master device recognizes that the bus clock line is set (SCLAn = 1) and after the stop condition setup time has elapsed, the master device sets the bus data line (SDAAn = 1) and issues a stop condition (i.e. SCLAn =1 changes SDAAn from 0 to 1). The slave device detects the generated stop condition and slave device issue an interrupt (INTIICAn: stop condition).

Remarks 1. <1> to <19> in Figure 19-33 represent the entire procedure for communicating data using the I^2C bus.

Figure 19-33 (1) Start condition ~ address ~ data shows the processing from <1> to <7>, Figure 19-33 (2) Address ~ data ~ data shows the processing from <3> to <12>, and Figure 19-33 (3) Data ~ data ~ stop condition shows the processing from <8> to <19>.

2. n = 0

CHAPTER 21 LCD CONTROLLER/DRIVER

The number of LCD display function pins of the RL78/I1B differs depending on the product. The following table shows the number of pins of each product.

Table 21-1. Number of LCD Display Function Pins of Each Product

Item		RL78/I1B															
		80 pins (R5F10MMx (x = G, E))								100 pins (R5F10MPx (x = G, E))							
LCD controller/ driver		Segment signal outputs: 34 (30)[Note] Common signal outputs: 8								Segment signal outputs: 42 (38)[Note] Common signal outputs: 8							
Multiplexed I/O port		bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Segment	P0	SEG 37	SEG 36	SEG 35	SEG 34	SEG 33	SEG 32	–	–	–	–	–	–	–	–	–	–
	P1	SEG 11	SEG 10	SEG 9	SEG 8	SEG 7	SEG 6	SEG 5	SEG 4	SEG 11	SEG 10	SEG 9	SEG 8	SEG 7	SEG 6	SEG 5	SEG 4
	P3	–	–	–	–	SEG 27	SEG 26	SEG 25	SEG 24	SEG 31	SEG 30	SEG 29	SEG 28	SEG 27	SEG 26	SEG 25	SEG 24
	P5	–	–	–	–	–	–	–	–	SEG 39	SEG 38	SEG 37	SEG 36	SEG 35	SEG 34	SEG 33	SEG 32
	P7	SEG 23	SEG 22	SEG 21	SEG 20	SEG 19	SEG 18	SEG 17	SEG 16	SEG 23	SEG 22	SEG 21	SEG 20	SEG 19	SEG 18	SEG 17	SEG 16
	P8	–	–	–	–	SEG 15	SEG 14	SEG 13	SEG 12	–	–	SEG 41	SEG 40	SEG 15	SEG 14	SEG 13	SEG 12
Alternate relationship between COM signal output pins and I/O pots		–															
Alternate relationship between COM signal output pins and LCD display function pins	COM4	SEG0								SEG0							
	COM5	SEG1								SEG1							
	COM6	SEG2								SEG2							
	COM7	SEG3								SEG3							

Note ( ) indicates the number of signal output pins when 8 com is used.

Figure 21-43. Eight-Time-Slice LCD Drive Waveform Examples Between SEG4 and Each Common Signals (1/4 Bias Method) (1/2)

(a) Waveform A

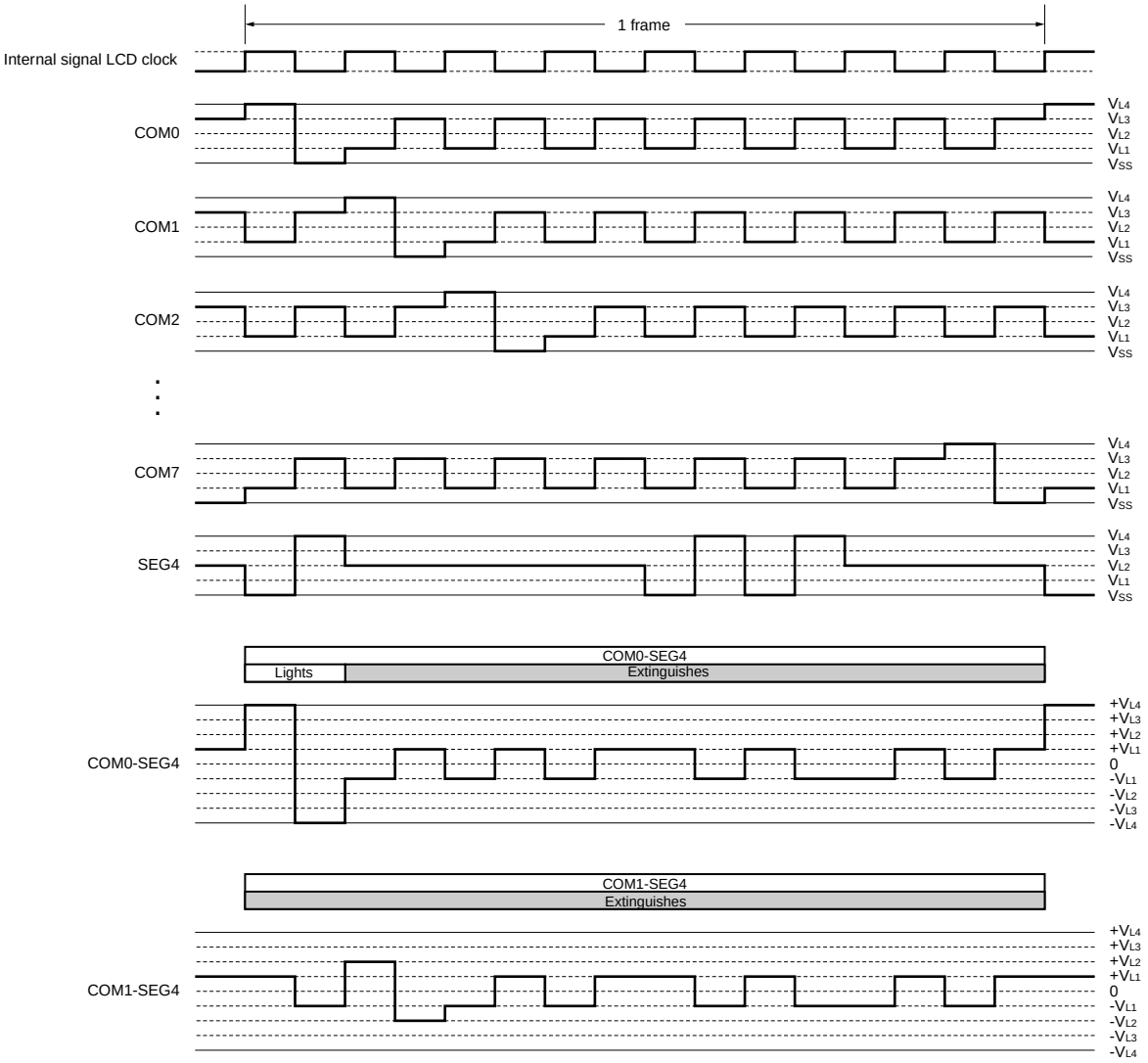


Table 24-1. Operating Statuses in HALT Mode (2/2)

HALT Mode Setting / Item			When HALT Instruction Is Executed While CPU Is Operating on Subsystem Clock	
			When CPU Is Operating on XT1 Clock (f_{XT})	When CPU Is Operating on External Subsystem Clock (f_{EXS})
System clock			Clock supply to the CPU is stopped	
	Main system clock	f_{IH}	Operation disabled	
		f_X		
		f_{EX}		
	Subsystem clock	f_{XT}	Operation continues (cannot be stopped)	Cannot operate
		f_{EXS}	Cannot operate	Operation continues (cannot be stopped)
	f_{IL}		Set by bits 0 (WDSTBYON) and 4 (WDTON) of option byte (000C0H), and WUTMMCK0 bit of subsystem clock supply mode control register (OSMC) (However, WUTMMCK0 cannot be set to 1 while the CPU is operating with subsystem clock) • WUTMMCK0 = 0 and WDTON = 0: Stops • WUTMMCK0 = 0, WDTON = 1, and WDSTBYON = 1: Oscillates • WUTMMCK0 = 0, WDTON = 1, and WDSTBYON = 0: Stops	
CPU			Operation stopped	
Code flash memory				
<R> RAM			Operation stopped (Operable while in the DTC is executed)	
Port (latch)			Status before HALT mode was set is retained	
Timer array unit			Operable when the RTCLPC bit is 0 (operation is disabled when the RTCLPC bit is not 0).	
Real-time clock 2			Operable (Operation in high-accuracy 1 Hz output mode is disabled.)	
Subsystem clock frequency measurement circuit			Operation disabled	
High-speed on-chip oscillator clock frequency correction function				
Oscillation stop detection				
Battery backup function			Operable (when VBATEN = 1 and VBATSEL = 0)	
12-bit interval timer			Operable	
8-bit interval timer				
Watchdog timer			Operable (See **CHAPTER 13 WATCHDOG TIMER**)	
Clock output/buzzer output			Operable	
A/D converter			Operation disabled	
ΔΣ A/D Converter				
Temperature sensor 2				
Comparator			Operable when external input (IVREFn) is selected for comparator reference voltage.	
Serial array unit (SAU)			Operable when the RTCLPC bit is 0 (operation is disabled when the RTCLPC bit is not 0).	
IrDA			Operation disabled	
Serial interface (IICA)			Operation disabled	
LCD controller/driver			Operable (However, this depends on the status of the clock selected as the LCD source clock: operation is possible if the selected clock is operating, but operation will stop if the selected clock is stopped.)	
Data transfer controller (DTC)			Operable when the RTCLPC bit is 0 (operation is disabled when the RTCLPC bit is not 0).	
Power-on-reset function			Operable	
Voltage detection function				
External interrupt				
CRC operation function	High-speed CRC		Operation disabled	
	General-purpose CRC		In the calculation of the RAM area, operable when DTC is executed	
RAM parity error detection function			Operation stopped (Operable when DTC is executed only)	
RAM guard function				
SFR guard function				
Illegal-memory access detection function				

(**Remark** is listed on the next page.)

27.3.2 Voltage detection level register (LVIS)

This register selects the voltage detection level.

This register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation input sets this register to 00H/01H/81H[Note 1].

Figure 27-3. Format of Voltage Detection Level Select Register (LVIS)

Address: FFFAAH After reset: 00H/01H/81H[Note 1] R/W

Symbol	<7>	6	5	4	3	2	1	<0>
LVIS	LVIMD[Note 2]	0	0	0	0	0	0	LVILV[Note 2]

LVIMD[Note 2]	Operation mode of voltage detection
0	Interrupt mode
1	Reset mode

LVILV[Note 2]	LVD detection level
0	High-voltage detection level (V_{LVDH})
1	Low-voltage detection level (V_{LVDL} or V_{LVDL})

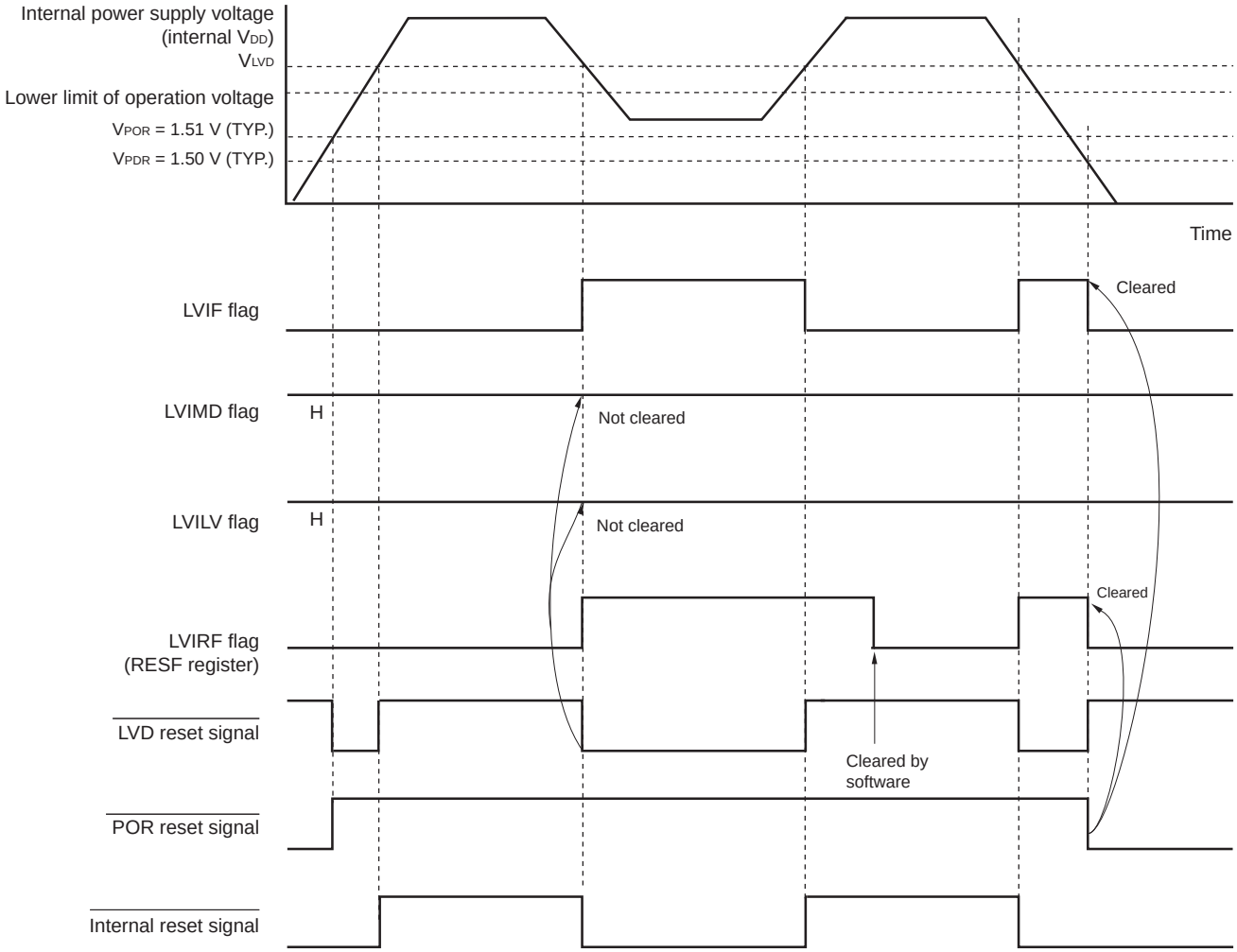
Notes 1. The reset value changes depending on the reset source and the setting of the option byte.
This register is not cleared (00H) by LVD reset.
The generation of reset signal other than an LVD reset sets as follows.
- When option byte LVIMDS1, LVIMDS0 = 1, 0: 00H
- When option byte LVIMDS1, LVIMDS0 = 1, 1: 81H
- When option byte LVIMDS1, LVIMDS0 = 0, 1: 01H

2. Writing “0” can only be allowed in the interrupt & reset mode (option byte LVIMDS1, LVIMDS0 = 1, 0). Do not set LVIMD and LVILV in other cases. The value is switched automatically when reset or interrupt is generated in the interrupt & reset mode.

Cautions 1. Rewrite the value of the LVIS register according to Figures 27-8 and 27-9.

2. Specify the LVD operation mode and detection voltage (V_{LVDH}, V_{LVDL}, V_{LVD}) of each mode by using the option byte 000C1H. Figure 27-4 shows the format of the user option byte (000C1H/010C1H). For details about the option byte, see CHAPTER 32 OPTION BYTE.

Figure 27-5. Timing of Voltage Detector Internal Reset Signal Generation (Option Byte LVIMDS1, LVIMDS0 = 1, 1)



Remark V_{POR}: POR power supply rise detection voltage
V_{PDR}: POR power supply fall detection voltage

30.3.1.1 Flash memory CRC control register (CRC0CTL)

This register is used to control the operation of the high-speed CRC ALU, as well as to specify the operation range.

The CRC0CTL register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 30-1. Format of Flash Memory CRC Control Register (CRC0CTL)

Address: F02F0H After reset: 00H R/W

Symbol	<7>	6	5	4	3	2	1	0
CRC0CTL	CRC0EN	0	0	0	0	FEA2[Note]	FEA1	FEA0

CRC0EN	Control of CRC ALU operation
0	Stop the operation.
1	Start the operation according to HALT instruction execution.

FEA2[Note]	FEA1	FEA0	High-speed CRC operation range
0	0	0	0000H to 3FFBH (16 K-4 bytes)
0	0	1	0000H to 7FFBH (32 K-4 bytes)
0	1	0	0000H to BFFBH (48 K-4 bytes)
0	1	1	0000H to FFFBH (64 K-4 bytes)
1	0	0	00000H to 13FFBH (80 K-4 bytes)
1	0	1	00000H to 17FFBH (96 K-4 bytes)
1	1	0	00000H to 1BFFBH (112 K-4 bytes)
1	1	1	00000H to 1FFFBH (128 K-4 bytes)

Note Be sure to set FEA2 bit to “0” on R5F10MME and R5F10MPE.

Remark Input the expected CRC operation result value to be used for comparison in the lowest 4 bytes of the flash memory. Note that the operation range will thereby be reduced by 4 bytes.

37.4 AC Characteristics

(T_A = –40 to +85°C, 1.9 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Items	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Instruction cycle (minimum instruction execution time)	T_{CY}	Main system clock (f_{MAIN}) operation	HS (high-speed main) mode	2.7 V ≤ V_{DD} Note 1 ≤ 5.5 V	0.0417		1	μs
				2.4 V ≤ V_{DD} Note 1 < 2.7 V	0.0625		1	μs
			LS (low-speed main) mode	1.9 V ≤ V_{DD} Note 1 ≤ 5.5 V	0.125		1	μs
		Subsystem clock (f_{SUB}) operation		1.9 V ≤ V_{DD} Note 1 ≤ 5.5 V	28.5	30.5	31.3	μs
		In the self programming mode	HS (high-speed main) mode	2.7 V ≤ V_{DD} Note 1 ≤ 5.5 V	0.0417		1	μs
				2.4 V ≤ V_{DD} Note 1 < 2.7 V	0.0625		1	μs
			LS (low-speed main) mode	1.9 V ≤ V_{DD} Note 1 ≤ 5.5 V	0.125		1	μs
External system clock frequency	f_{EX}	2.7 V ≤ V_{DD} Note 1 ≤ 5.5 V			1.0		20.0	MHz
		2.4 V ≤ V_{DD} Note 1 < 2.7 V			1.0		16.0	MHz
		1.9 V ≤ V_{DD} Note 1 < 2.4 V			1.0		8.0	MHz
	f_{EXS}				32		35	kHz
External system clock input high-level width, low-level width	t_{EXH}, t_{EXL}	2.7 V ≤ V_{DD} Note 1 ≤ 5.5 V			24			ns
		2.4 V ≤ V_{DD} Note 1 < 2.7 V			30			ns
		1.9 V ≤ V_{DD} Note 1 < 2.4 V			60			ns
	t_{EXHS}, t_{EXLS}				13.7			μs
TI00 to TI07 input high-level width, low-level width	t_{TIH}, t_{TIL}				1/f_{MCK}+10			ns Note 2
TO00 to TO07 output frequency	f_{TO}	HS (high-speed main) mode		4.0 V ≤ EV_{DD} ≤ 5.5 V			12	MHz
				2.7 V ≤ EV_{DD} < 4.0 V			8	MHz
				2.4 V ≤ EV_{DD} < 2.7 V			4	MHz
		LS (low-speed main) mode		1.9 V ≤ EV_{DD} ≤ 5.5 V			4	MHz
PCLBUZ0, PCLBUZ1 output frequency	f_{PCL}	HS (high-speed main) mode		4.0 V ≤ EV_{DD} ≤ 5.5 V			16	MHz
				2.7 V ≤ EV_{DD} < 4.0 V			8	MHz
				2.4 V ≤ EV_{DD} < 2.7 V			4	MHz
		LS (low-speed main) mode		1.9 V ≤ EV_{DD} ≤ 5.5 V			4	MHz
Interrupt input high-level width, low-level width	t_{INTH}, t_{INTL}	INTP0		1.9 V ≤ V_{DD} Note 1 ≤ 5.5 V	1			μs
		INTP1 to INTP7		1.9 V ≤ EV_{DD} ≤ 5.5 V	1			μs
$\overline{\text{RESET}}$ low-level width	t_{RSL}				10			μs

Notes 1. The power supply voltage (VBAT pin or V_{DD} pin) selected by the battery backup feature.

2. The following conditions are required for low voltage interface:
1.9 V ≤ V_{DD} < 2.7 V: MIN. 125 ns

Remark f_{MCK}: Timer array unit operation clock frequency
(Operation clock to be set by the CKSmn0, CKSmn1 bits of timer mode register mn (TMRmn)
m: Unit number (m = 0), n: Channel number (n = 0 to 7))

37.5.2 Serial interface IICA

(1) I^2C standard mode

(T_A = –40 to +85°C, 1.9 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f_{SCL}	Standard mode: f_{CLK} ≥ 1 MHz	2.7 V ≤ EV_{DD} ≤ 5.5 V	0	100	0	100	kHz
			1.9 V[Note 3] ≤ EV_{DD} ≤ 5.5 V	0	100	0	100	kHz
Setup time of restart condition	$t_{SU:STA}$	2.7 V ≤ EV_{DD} ≤ 5.5 V		4.7		4.7		μs
		1.9 V[Note 3] ≤ EV_{DD} ≤ 5.5 V		4.7		4.7		μs
Hold time[Note 1]	$t_{HD:STA}$	2.7 V ≤ EV_{DD} ≤ 5.5 V		4.0		4.0		μs
		1.9 V[Note 3] ≤ EV_{DD} ≤ 5.5 V		4.0		4.0		μs
Hold time when SCLA0 = “L”	t_{LOW}	2.7 V ≤ EV_{DD} ≤ 5.5 V		4.7		4.7		μs
		1.9 V[Note 3] ≤ EV_{DD} ≤ 5.5 V		4.7		4.7		μs
Hold time when SCLA0 = “H”	t_{HIGH}	2.7 V ≤ EV_{DD} ≤ 5.5 V		4.0		4.0		μs
		1.9 V[Note 3] ≤ EV_{DD} ≤ 5.5 V		4.0		4.0		μs
Data setup time (reception)	$t_{SU:DAT}$	2.7 V ≤ EV_{DD} ≤ 5.5 V		250		250		ns
		1.9 V[Note 3] ≤ EV_{DD} ≤ 5.5 V		250		250		ns
Data hold time (transmission)[Note 2]	$t_{HD:DAT}$	2.7 V ≤ EV_{DD} ≤ 5.5 V		0	3.45	0	3.45	μs
		1.9 V[Note 3] ≤ EV_{DD} ≤ 5.5 V		0	3.45	0	3.45	μs
Setup time of stop condition	$t_{SU:STO}$	2.7 V ≤ EV_{DD} ≤ 5.5 V		4.0		4.0		μs
		1.9 V[Note 3] ≤ EV_{DD} ≤ 5.5 V		4.0		4.0		μs
Bus-free time	t_{BUF}	2.7 V ≤ EV_{DD} ≤ 5.5 V		4.7		4.7		μs
		1.9 V[Note 3] ≤ EV_{DD} ≤ 5.5 V		4.7		4.7		μs

Notes 1. The first clock pulse is generated after this period when the start/restart condition is detected.

2. The maximum value (MAX.) of $t_{HD:DAT}$ is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

3. When HS (high-speed main) mode, this value becomes 2.4 V.

Remark The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.

Standard mode: C_b = 400 pF, R_b = 2.7 kΩ

(3) 4 kHz sampling mode

(T_A = –40 to +85°C, $AV_{DD} \leq V_{DD}$ + 0.3 V, 2.4 V ≤ AV_{DD} ≤ 5.5 V, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Operation clock	f_{DSAD}	f_X oscillation clock, input external clock or high-speed on-chip oscillator clock is used		12		MHz
Sampling frequency	f_S			3906.25		Hz
Oversampling frequency	f_{OS}			1.5		MHz
Output data rate	T_{DATA}			256		µs
Data width	RES			24		bit
SNDR	SNDR	x1 gain High-speed system clock is selected as operating clock of 24-bit ΔΣ A/D converter (bit 0 of PCKC register (DSADCK) = 1)		80		dB
		x16 gain High-speed system clock is selected as operating clock of 24-bit ΔΣ A/D converter (bit 0 of PCKC register (DSADCK) = 1)	69	74		
		x32 gain High-speed system clock is selected as operating clock of 24-bit ΔΣ A/D converter (bit 0 of PCKC register (DSADCK) = 1)	65	69		
Passband (low pass band)	f_{Chpf}	At –3 dB (phase in high pass filter not adjusted) Bits 7 and 6 of DSADHPFCR register (DSADCOF1, DSADCOF0) = 00		0.607		Hz
		At –3 dB (phase in high pass filter not adjusted) Bits 7 and 6 of DSADHPFCR register (DSADCOF1, DSADCOF0) = 01		1.214		Hz
		At –3 dB (phase in high pass filter not adjusted) Bits 7 and 6 of DSADHPFCR register (DSADCOF1, DSADCOF0) = 10		2.429		Hz
		At –3 dB (phase in high pass filter not adjusted) Bits 7 and 6 of DSADHPFCR register (DSADCOF1, DSADCOF0) = 11		4.857		Hz
In-band ripple 1	rp1	45 Hz to 55 Hz @50 Hz 54 Hz to 66 Hz @60 Hz	–0.01		0.01	dB
In-band ripple 2	rp2	45 Hz to 275 Hz @50 Hz 54 Hz to 330 Hz @60 Hz	–0.1		0.1	
In-band ripple 3	rp3	45 Hz to 1100 Hz @50 Hz 54 Hz to 1320 Hz @60 Hz	–0.1		0.1	
Passband (high pass band)	f_{Clpf}	–3 dB		1672		Hz
Stopband (high pass band)	fatt	–80 dB		2545		Hz
Out-band attenuation	ATT1	f_S	–80			dB
	ATT2	2 f_S	–80			dB