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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details	
Product Status	Obsolete
Architecture	MCU, FPGA
Core Processor	ARM® Cortex®-M3
Flash Size	128KB
RAM Size	16KB
Peripherals	DMA, POR, WDT
Connectivity	EBI/EMI, I²C, SPI, UART/USART
Speed	100MHz
Primary Attributes	ProASIC®3 FPGA, 60K Gates, 1536D-Flip-Flops
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	288-TFBGA, CSPBGA
Supplier Device Package	288-CSP (11x11)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/a2f060m3e-1cs288i

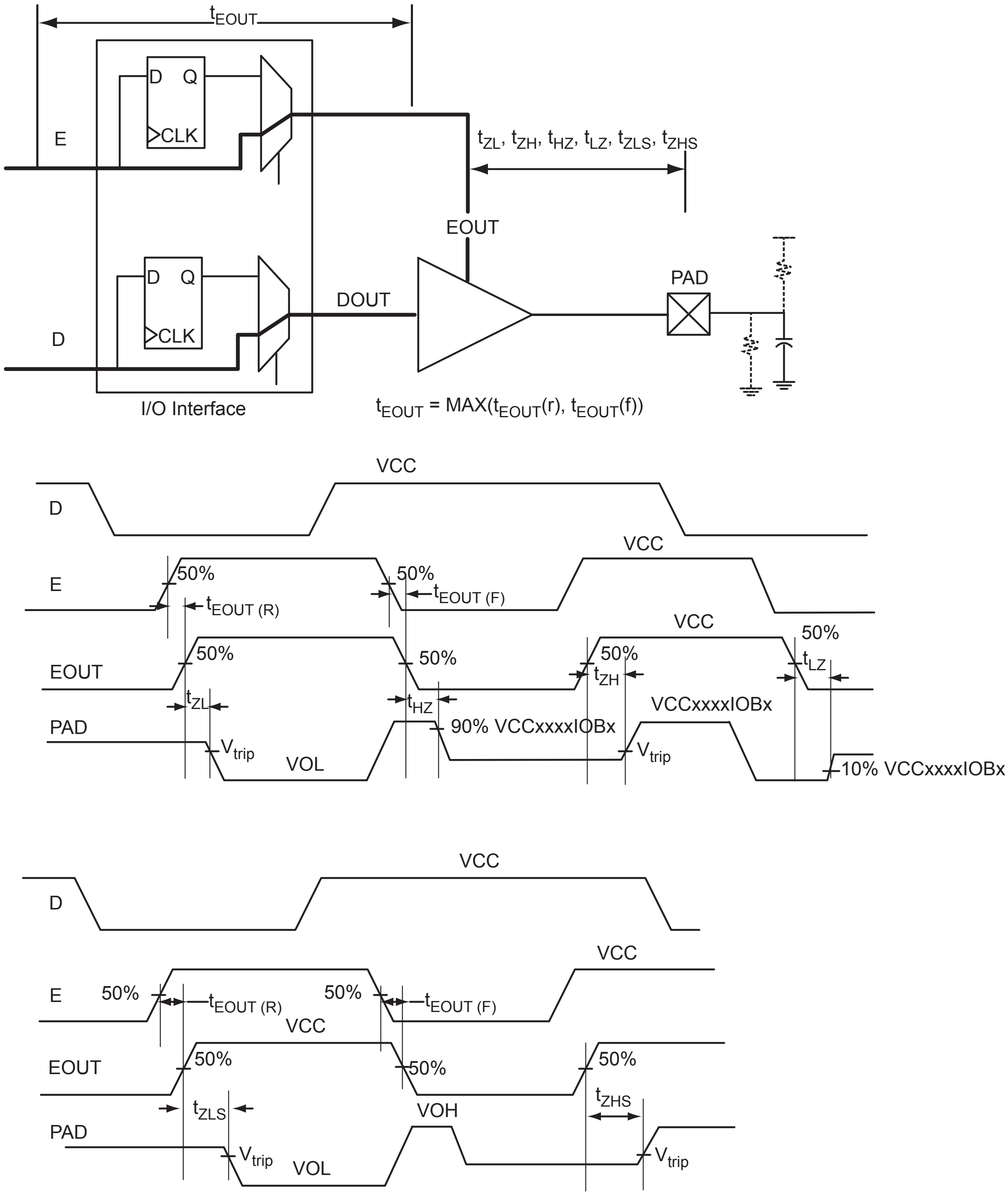


Figure 2-5 • **Tristate Output Buffer Timing Model and Delays (example)**

Detailed I/O DC Characteristics

***Table 2-26* • Input Capacitance**

Symbol	Definition	Conditions	Min.	Max.	Units
C_{IN}	Input capacitance	V_{IN} = 0, f = 1.0 MHz		8	pF
C_{INCLK}	Input capacitance on the clock pin	V_{IN} = 0, f = 1.0 MHz		8	pF

***Table 2-27* • I/O Output Buffer Maximum Resistances[1]**
Applicable to FPGA I/O Banks

Standard	Drive Strength	$R_{PULL\text{-}DOWN}$ (Ω)[2]	$R_{PULL\text{-}UP}$ (Ω)[3]
3.3 V LVTTL / 3.3 V LVCMOS	2 mA	100	300
	4 mA	100	300
	6 mA	50	150
	8 mA	50	150
	12 mA	25	75
	16 mA	17	50
	24 mA	11	33
2.5 V LVCMOS	2 mA	100	200
	4 mA	100	200
	6 mA	50	100
	8 mA	50	100
	12 mA	25	50
	16 mA	20	40
	24 mA	11	22
1.8 V LVCMOS	2 mA	200	225
	4 mA	100	112
	6 mA	50	56
	8 mA	50	56
	12 mA	20	22
	16 mA	20	22
1.5 V LVCMOS	2 mA	200	224
	4 mA	100	112
	6 mA	67	75
	8 mA	33	37
	12 mA	33	37
3.3 V PCI/PCI-X	Per PCI/PCI-X specification	25	75

Notes:

1. *These maximum values are provided for information only. Minimum output buffer resistance values depend on VCCxxxxIOBx, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website (also generated by the SoC Products Group Libero SoC toolset).*
2. $R_{(PULL\text{-}DOWN\text{-}MAX)} = (V_{OLspec}) / I_{OLspec}$
3. $R_{(PULL\text{-}UP\text{-}MAX)} = (V_{CCImax} - V_{OHspec}) / I_{OHspec}$

The length of time an I/O can withstand I_{OSH}/I_{OSL} events depends on the junction temperature. The reliability data below is based on a 3.3 V, 12 mA I/O setting, which is the worst case for this type of analysis.

For example, at 100°C, the short current condition would have to be sustained for more than 2200 operation hours to cause a reliability concern. The I/O design does not contain any short circuit protection, but such protection would only be needed in extremely prolonged stress conditions.

***Table 2-32* • Duration of Short Circuit Event before Failure**

Temperature	Time before Failure
–40°C	> 20 years
0°C	> 20 years
25°C	> 20 years
70°C	5 years
85°C	2 years
100°C	6 months

***Table 2-33* • Schmitt Trigger Input Hysteresis**
Hysteresis Voltage Value (typical) for Schmitt Mode Input Buffers

Input Buffer Configuration	Hysteresis Value (typical)
3.3 V LVTTL / LVCMOS / PCI / PCI-X (Schmitt trigger mode)	240 mV
2.5 V LVCMOS (Schmitt trigger mode)	140 mV
1.8 V LVCMOS (Schmitt trigger mode)	80 mV
1.5 V LVCMOS (Schmitt trigger mode)	60 mV

***Table 2-34* • I/O Input Rise Time, Fall Time, and Related I/O Reliability**

Input Buffer	Input Rise/Fall Time (min.)	Input Rise/Fall Time (max.)	Reliability
LVTTL/LVCMOS	No requirement	10 ns *	20 years (100°C)
LVDS/B-LVDS/ M-LVDS/LVPECL	No requirement	10 ns *	10 years (100°C)

Note: **The maximum input rise/fall time is related to the noise induced into the input buffer trace. If the noise is low, then the rise time and fall time of input buffers can be increased beyond the maximum value. The longer the rise/fall times, the more susceptible the input signal is to the board noise. Microsemi SoC Products Group recommends signal integrity evaluation/characterization of the system to ensure that there is no excessive noise coupling into input signals.*

3.3 V PCI, 3.3 V PCI-X

Peripheral Component Interface for 3.3 V standard specifies support for 33 MHz and 66 MHz PCI Bus applications.

***Table 2-59* • Minimum and Maximum DC Input and Output Levels**

3.3 V PCI/PCI-X	VIL		VIH		VOL	VOH	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	**Min. V**	**Max. V**	**Min. V**	**Max. V**	**Max. V**	**Min. V**	**mA**	**mA**	**Max. mA**[1]	**Max. mA**[1]	**µA**[2]	**µA**[2]
Per PCI specification	Per PCI curves										15	15

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*

AC loadings are defined per the PCI/PCI-X specifications for the datapath; SoC Products Group loadings for enable path characterization are described in Figure 2-10.

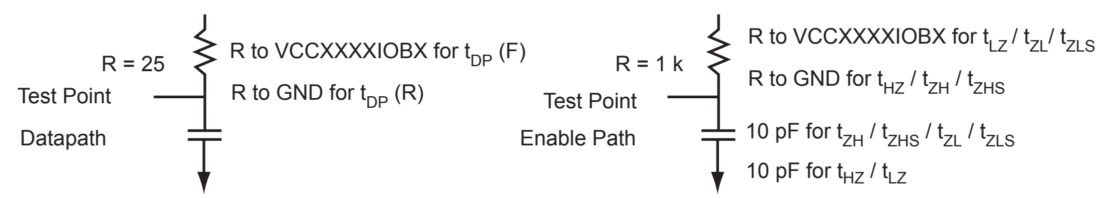


***Figure 2-10* • AC Loading**

AC loadings are defined per PCI/PCI-X specifications for the datapath; SoC Products Group loading for tristate is described in Table 2-60.

***Table 2-60* • AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	V_{REF} (typ.) (V)	C_{LOAD} (pF)
0	3.3	0.285 * VCCxxxxIOBx for $t_{DP(R)}$ 0.615 * VCCxxxxIOBx for $t_{DP(F)}$	–	10

* *Measuring point = $V_{trip.}$ See Table 2-22 on page 2-24 for a complete table of trip points.*

Timing Characteristics

***Table 2-61* • 3.3 V PCI**
Worst Commercial-Case Conditions: T_J = 85°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCxxxxIOBx = 3.0 V
Applicable to FPGA I/O Banks, I/O Assigned to EMC I/O Pins

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.60	2.54	0.04	0.82	0.39	2.58	1.88	3.06	3.39	4.64	3.94	ns
–1	0.50	2.11	0.03	0.68	0.32	2.15	1.57	2.55	2.82	3.87	3.28	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.

***Table 2-62* • 3.3 V PCI-X**
Worst Commercial-Case Conditions: T_J = 85°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCxxxxIOBx = 3.0 V
Applicable to FPGA I/O Banks, I/O Assigned to EMC I/O Pins

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.60	2.54	0.04	0.77	0.39	2.58	1.88	3.06	3.39	4.64	3.94	ns
–1	0.50	2.11	0.03	0.64	0.32	2.15	1.57	2.55	2.82	3.87	3.28	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.

DDR Module Specifications

Input DDR Module

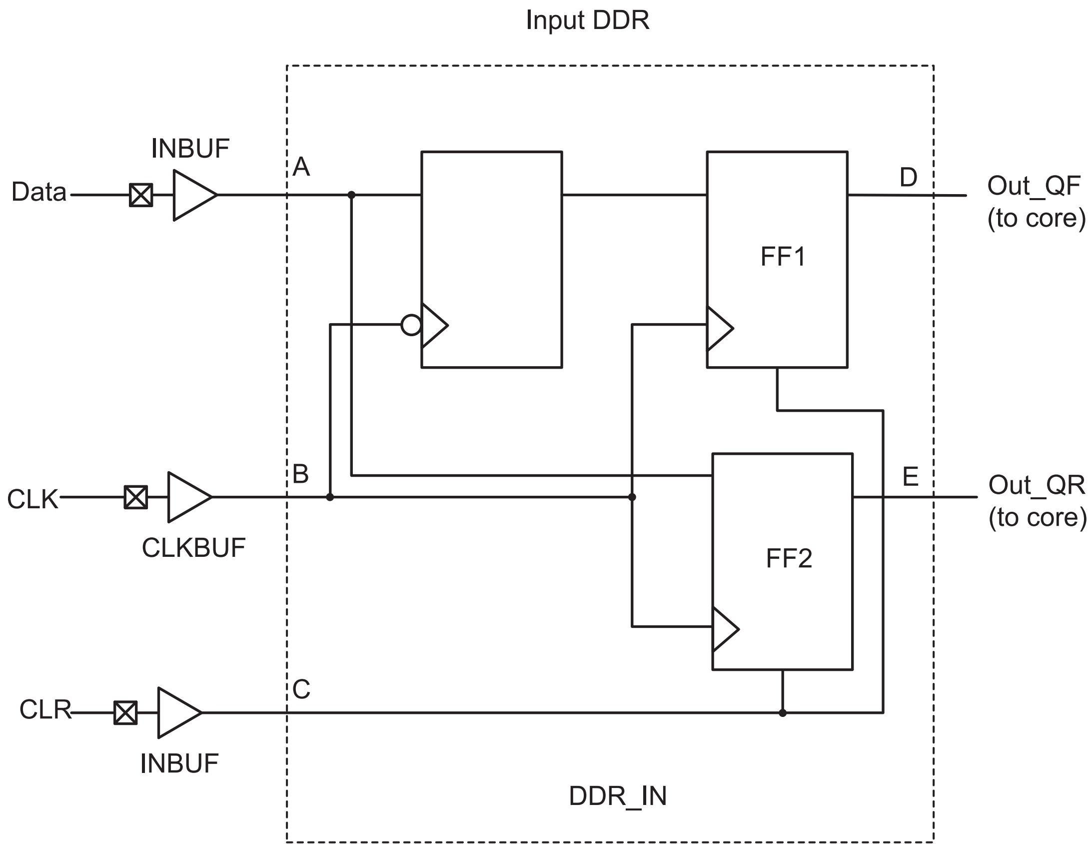
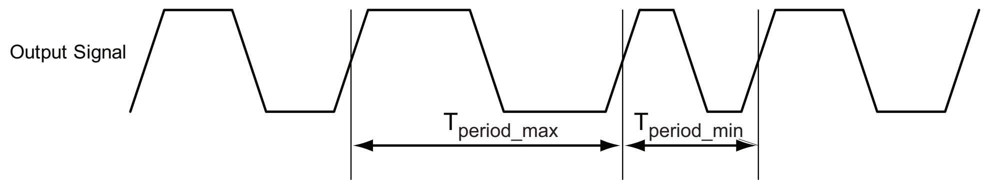


***Figure 2-19* • Input DDR Timing Model**

***Table 2-74* • Parameter Definitions**

Parameter Name	Parameter Definition	Measuring Nodes (from, to)
$t_{DDRICLKQ1}$	Clock-to-Out Out_QR	B, D
$t_{DDRICLKQ2}$	Clock-to-Out Out_QF	B, E
$t_{DDRISUD}$	Data Setup Time of DDR input	A, B
t_{DDRIHD}	Data Hold Time of DDR input	A, B
$t_{DDRICLR2Q1}$	Clear-to-Out Out_QR	C, D
$t_{DDRICLR2Q2}$	Clear-to-Out Out_QF	C, E
$t_{DDRIREMCLR}$	Clear Removal	C, B
$t_{DDRIRECCLR}$	Clear Recovery	C, B



Note: *Peak-to-peak jitter measurements are defined by $T_{peak\text{-}to\text{-}peak} = T_{period\_max} – T_{period\_min}$.*

Figure 2-28 • **Peak-to-Peak Jitter Definition**

FPGA Fabric SRAM and FIFO Characteristics

FPGA Fabric SRAM

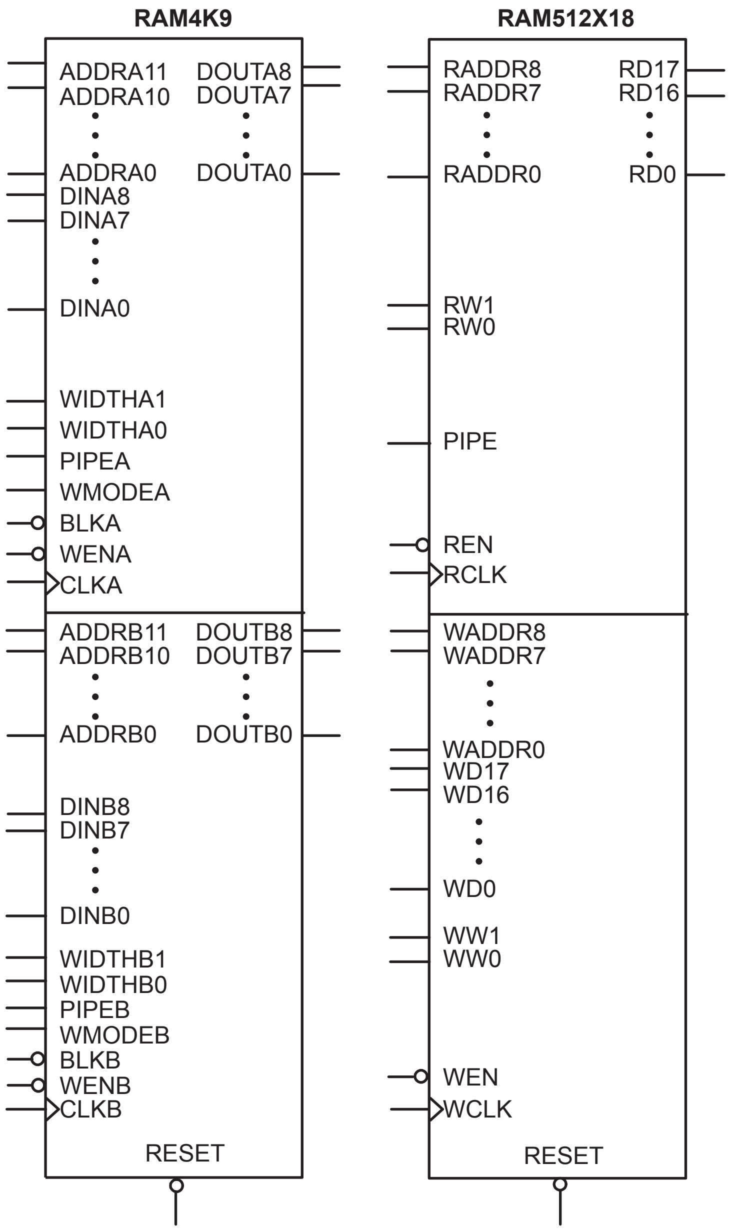


Figure 2-29 • **RAM Models**

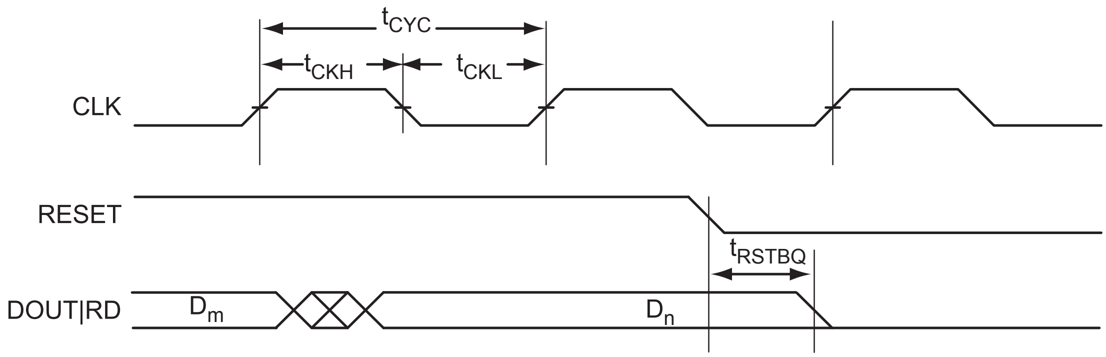


Figure 2-34 **• RAM Reset. Applicable to both RAM4K9 and RAM512x18.**

***Table 2-92* • JTAG 1532**
Worst Commercial-Case Conditions: T_J = 85°C, Worst-Case VCC = 1.425 V

Parameter	Description	–1	Std.	Units
t_{RSTB2Q}	Reset to Q (data out)	26.67	30.67	ns
F_{TCKMAX}	TCK Maximum Frequency	19.00	21.85	MHz
$t_{TRSTREM}$	ResetB Removal Time	0.00	0.00	ns
$t_{TRSTREC}$	ResetB Recovery Time	0.27	0.31	ns
$t_{TRSTMPW}$	ResetB Minimum Pulse	TBD	TBD	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.

Programmable Analog Specifications

Current Monitor

Unless otherwise noted, current monitor performance is specified at 25°C with nominal power supply voltages, with the output measured using the internal voltage reference with the internal ADC in 12-bit mode and 91 Ksps, after digital compensation. All results are based on averaging over 16 samples.

***Table 2-93* • Current Monitor Performance Specification**

Specification	Test Conditions	Min.	Typical	Max.	Units
Input voltage range (for driving ADC over full range)		0 – 48	0 – 50	1 – 51	mV
Analog gain	From the differential voltage across the input pads to the ADC input		50		V/V
Input referred offset voltage	Input referred offset voltage	0	0.1	0.5	mV
	–40ºC to +100ºC	0	0.1	0.5	mV
Gain error	Slope of BFSL vs. 50 V/V		±0.1	±0.5	% nom.
	–40ºC to +100ºC			±0.5	% nom.
Overall Accuracy	Peak error from ideal transfer function, 25°C		±(0.1 + 0.25%)	±(0.4 + 1.5%)	mV plus % reading
Input referred noise	0 VDC input (no output averaging)	0.3	0.4	0.5	mVrms
Common-mode rejection ratio	0 V to 12 VDC common-mode voltage	–86	–87		dB
Analog settling time	To 0.1% of final value (with ADC load)				
	From CM_STB (High)	5			µs
	From ADC_START (High)	5		200	µs
Input capacitance			8		pF
Input biased current	CM[n] or TM[n] pad, –40°C to +100°C over maximum input voltage range (plus is into pad)				
	Strobe = 0; IBIAS on CM[n]		0		µA
	Strobe = 1; IBIAS on CM[n]		1		µA
	Strobe = 0; IBIAS on TM[n]		2		µA
	Strobe = 1; IBIAS on TM[n]		1		µA
Power supply rejection ratio	DC (0 – 10 KHz)	41	42		dB
Incremental operational current monitor power supply current requirements (per current monitor instance, not including ADC or VAREFx)	VCC33A		150		µA
	VCC33AP		140		µA
	VCC15A		50		µA

Note: Under no condition should the TM pad ever be greater than 10 mV above the CM pad. This restriction is applicable only if current monitor is used.

***Table 2-98* • Analog Sigma-Delta DAC (continued)**

Specification	Test Conditions	Min.	Typ.	Max.	Units
Sigma-delta DAC power supply current requirements (not including VAREFx)	Input = 0, EN = 1 (operational mode)				
	VCC33SDDx		30	35	µA
	VCC15A		3	5	µA
	Input = Half scale, EN = 1 (operational mode)				
	VCC33SDDx		160	165	µA
	VCC15A		33	35	µA
	Input = Full scale, EN = 1 (operational mode)				
	VCC33SDDx		280	285	µA
	VCC15A		70	75	µA

*Note: *FS is full-scale error, defined as the difference between the actual value that triggers the transition to full-scale and the ideal analog full-scale transition value. Full-scale error equals offset error plus gain error. Refer to the Analog-to-Digital Converter chapter of the SmartFusion Programmable Analog User's Guide for more information.*

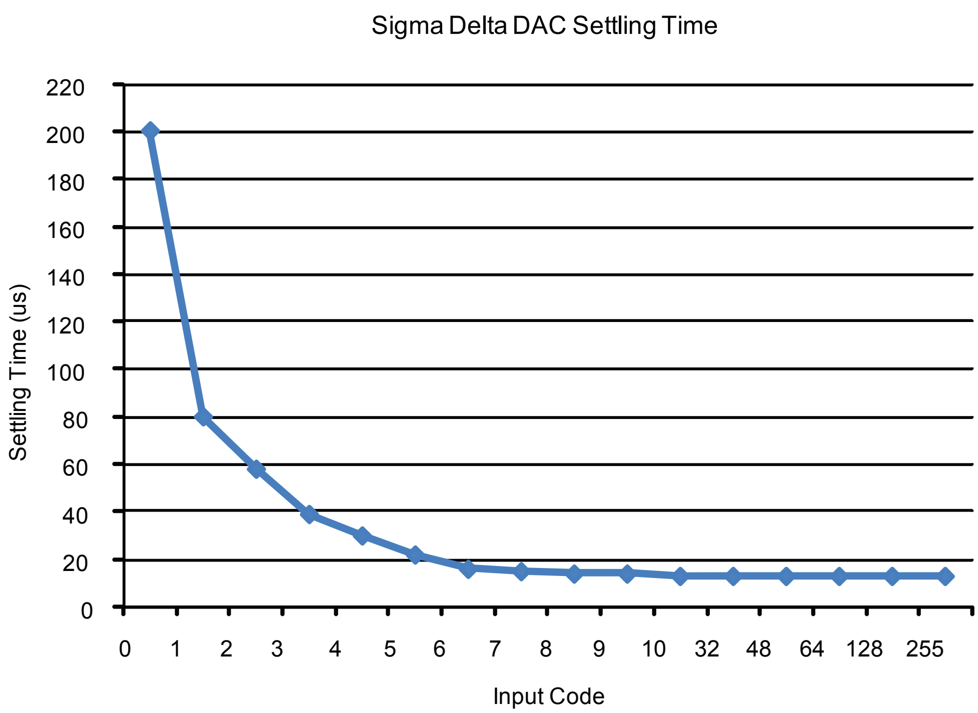


***Figure 2-44* • Sigma-Delta DAC Setting Time**

SmartFusion Ecosystem

The Microsemi SoC Products Group has a long history of supplying comprehensive FPGA development tools and recognizes the benefit of partnering with industry leaders to deliver the optimum usability and productivity to customers. Taking the same approach with processor development, Microsemi has partnered with key industry leaders in the microcontroller space to provide the robust SmartFusion ecosystem.

Microsemi is partnering with Keil and IAR to provide Software IDE support to SmartFusion system designers. The result is a robust solution that can be easily adopted by developers who are already doing embedded design. The learning path is straightforward for FPGA designers.

Support for the SoC Products Group device and ecosystem resources is represented in Figure 3-3.

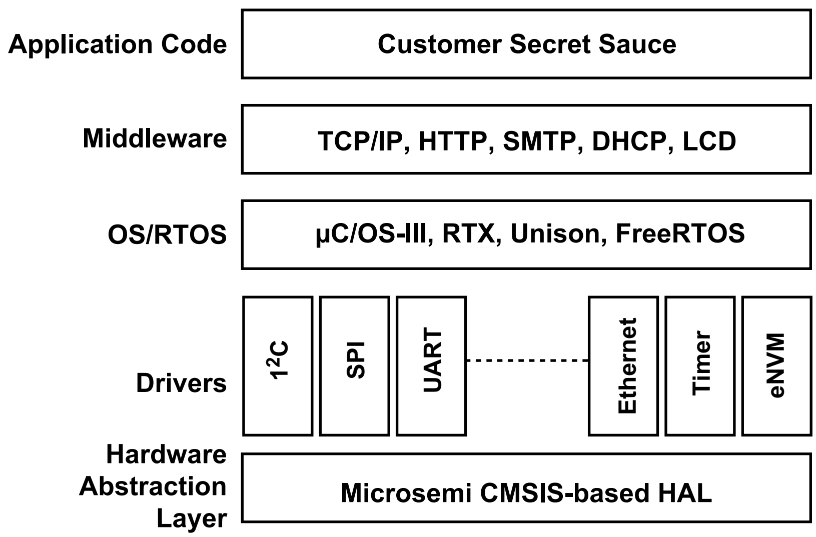


Figure 3-3 • **SmartFusion Ecosystem**

Figure 3-3 shows the SmartFusion stack with examples of drivers, RTOS, and middleware from Microsemi and partners. By leveraging the SmartFusion stack, designers can decide at which level to add their own customization to their design, thus speeding time to market and reducing overhead in the design.

ARM

Because an ARM processor was chosen for SmartFusion cSoCs, Microsemi's customers can benefit from the extensive ARM ecosystem. By building on Microsemi supplied hardware abstraction layer (HAL) and drivers, third party vendors can easily port RTOS and middleware for the SmartFusion cSoC.

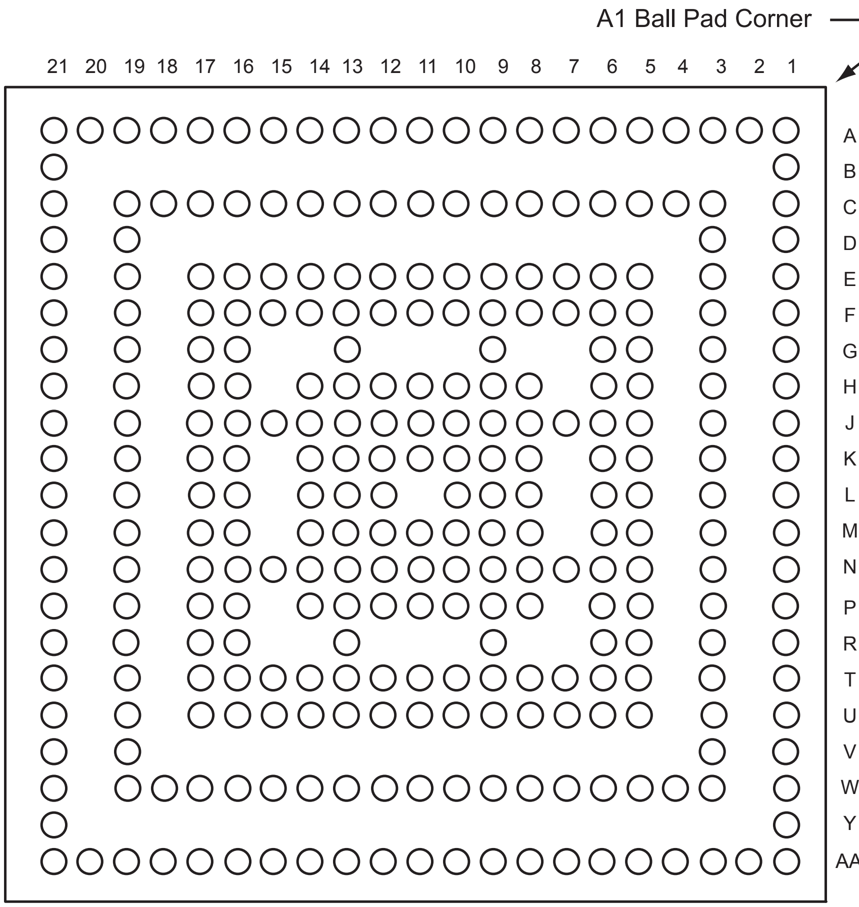
- ARM Cortex-M Series Processors
- ARM Cortex-M3 Processor Resource
- ARM Cortex-M3 Technical Reference Manual
- *ARM Cortex-M3 Processor Software Development for ARM7TDMI Processor Programmers* White Paper

Name	Type	Polarity/ Bus Size	Description
SPI_1_DO	Out	1	Data output. Second SPI. Can also be used as an MSS GPIO (see "GPIO_x" on page 5-6).
SPI_1_SS	Out	1	Slave select (chip select). Second SPI. Can also be used as an MSS GPIO (see "GPIO_x" on page 5-6).
Universal Asynchronous Receiver/Transmitter (UART) Peripherals			
UART_0_RXD	In	1	Receive data. First UART. Can also be used as an MSS GPIO (see "GPIO_x" on page 5-6).
UART_0_TXD	Out	1	Transmit data. First UART. Can also be used as an MSS GPIO (see "GPIO_x" on page 5-6).
UART_1_RXD	In	1	Receive data. Second UART. Can also be used as an MSS GPIO (see "GPIO_x" on page 5-6).
UART_1_TXD	Out	1	Transmit data. Second UART. Can also be used as an MSS GPIO (see "GPIO_x" on page 5-6).
Ethernet MAC			
MAC_CLK	In	Rise	Receive clock. 50 MHz ± 50 ppm clock source received from RMII PHY. Can be left floating when unused.
MAC_CRSDV	In	High	Carrier sense/receive data valid for RMII PHY Can also be used as an FPGA User IO (see "IO" on page 5-6).
MAC_MDC	Out	Rise	RMII management clock Can also be used as an FPGA User IO (see "IO" on page 5-6).
MAC_MDIO	In/Out	1	RMII management data input/output Can also be used as an FPGA User IO (see "IO" on page 5-6).
MAC_RXDx	In	2	Ethernet MAC receive data. Data recovered and decoded by PHY. The RXD[0] signal is the least significant bit. Can also be used as an FPGA User I/O (see "IO" on page 5-6).
MAC_RXER	In	HIGH	Ethernet MAC receive error. If MACRX_ER is asserted during reception, the frame is received and status of the frame is updated with MACRX_ER. Can also be used as an FPGA user I/O (see "IO" on page 5-6).
MAC_TXDx	Out	2	Ethernet MAC transmit data. The TXD[0] signal is the least significant bit. Can also be used as an FPGA user I/O (see "IO" on page 5-6).
MAC_TXEN	Out	HIGH	Ethernet MAC transmit enable. When asserted, indicates valid data for the PHY on the TXD port. Can also be used as an FPGA User I/O (see "IO" on page 5-6).

TQ144	
Pin Number	**A2F060 Function**
1	VCCPLL0
2	VCOMPLA0
3	GNDQ
4	GFA2/IO42PDB5V0
5	GFB2/IO42NDB5V0
6	GFC2/IO41PDB5V0
7	IO41NDB5V0
8	VCC
9	GND
10	VCCFPGAIOB5
11	IO38PDB5V0
12	IO38NDB5V0
13	IO36PDB5V0
14	IO36NDB5V0
15	GND
16	GNDRCOSC
17	VCCRCOSC
18	MSS_RESET_N
19	GPIO_0/IO33RSB4V0
20	GPIO_1/IO32RSB4V0
21	GPIO_2/IO31RSB4V0
22	GPIO_3/IO30RSB4V0
23	GPIO_4/IO29RSB4V0
24	GND
25	VCCMSSIOB4
26	VCC
27	GPIO_5/IO28RSB4V0
28	GPIO_6/IO27RSB4V0
29	GPIO_7/IO26RSB4V0
30	GPIO_8/IO25RSB4V0
31	VCCESRAM
32	GNDSDD0
33	VCC33SDD0
34	VCC15A
35	PCAP
36	NCAP

TQ144	
Pin Number	**A2F060 Function**
73	VCC33A
74	PTEM
75	PTBASE
76	SPI_0_DO/GPIO_16
77	SPI_0_DI/GPIO_17
78	SPI_0_CLK/GPIO_18
79	SPI_0_SS/GPIO_19
80	UART_0_RXD/GPIO_21
81	UART_0_TXD/GPIO_20
82	UART_1_RXD/GPIO_29
83	UART_1_TXD/GPIO_28
84	VCC
85	VCCMSSIOB2
86	GND
87	I2C_1_SDA/GPIO_30
88	I2C_1_SCL/GPIO_31
89	I2C_0_SDA/GPIO_22
90	I2C_0_SCL/GPIO_23
91	GNDENVM
92	VCCENVM
93	JTAGSEL
94	TCK
95	TDI
96	TMS
97	TDO
98	TRSTB
99	VJTAG
100	VDDBAT
101	VCCLPXTAL
102	LPXOUT
103	LPXIN
104	GNDLPXTAL
105	GNDMAINXTAL
106	MAINXOUT
107	MAINXIN
108	VCCMAINXTAL

CS288



Note: *Bottom view*

Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx.

Pin Number	FG484	
	A2F200 Function	A2F500 Function
L9	VCC	VCC
L10	GND	GND
L11	VCC	VCC
L12	GND	GND
L13	VCC	VCC
L14	GND	GND
L15	VCC	VCC
L16	GND	GND
L17	GNDQ	GNDQ
L18	GDA2/IO33NDB1V0	GDA2/IO42NDB1V0
L19	VCCFPGAIOB1	VCCFPGAIOB1
L20	GDB1/IO30PDB1V0	GDB1/IO39PDB1V0
L21	GDB0/IO30NDB1V0	GDB0/IO39NDB1V0
L22	GDC2/IO32PDB1V0	GDC2/IO41PDB1V0
M1	NC	IO71PDB5V0
M2	NC	IO71NDB5V0
M3	VCCFPGAIOB5	VCCFPGAIOB5
M4	NC	IO72NPB5V0
M5	GNDQ	GNDQ
M6	NC	IO68PDB5V0
M7	GND	GND
M8	VCC	VCC
M9	GND	GND
M10	VCC	VCC
M11	GND	GND
M12	VCC	VCC
M13	GND	GND
M14	VCC	VCC
M15	GND	GND
M16	VCCFPGAIOB1	VCCFPGAIOB1
M17	NC	NC
M18	GDB2/IO33PDB1V0	GDB2/IO42PDB1V0
M19	VJTAG	VJTAG
M20	GND	GND

Notes:

1. *Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.*
2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*

Revision	Changes	Page
Revision 7 (continued)	The following sentence was removed from the "I/O Power-Up and Supply Voltage Thresholds for Power-On Reset (Commercial and Industrial)" section because it is incorrect (SAR 31047): "The many different supplies can power up in any sequence with minimized current spikes or surges."	2-4
	Table 2-8 • Quiescent Supply Current Characteristics was divided into two tables: one for power supplies configurations and one for quiescent supply current. SoC mode was added to both tables (SAR 26378) and VCOMPLAx was removed from Table 2-8 • Power Supplies Configuration (SAR 29591). Quiescent supply current values were updated in Table 2-9 • Quiescent Supply Current Characteristics (SAR 33067).	2-10
	The "Total Static Power Consumption—P_{STAT}" section was revised: "$N_{eNVM-BLOCKS}$ * P_{DC4}" was removed from the equation for P_{STAT} (SAR 33067).	2-14
	Table 2-14 • Different Components Contributing to Dynamic Power Consumption in SmartFusion cSoCs and Table 2-15 • Different Components Contributing to the Static Power Consumption in SmartFusion cSoCs were revised to reflect updates in the SmartFusion power calculator (SARs 26405, 33067).	2-12, 2-13
	Table 2-82 • A2F060 Global Resource is new (SAR 33132).	2-61
	Output duty cycle was corrected to 50% in Table 2-83 • Electrical Characteristics of the RC Oscillator. It was incorrectly noted as 1% previously. Operating current for 3.3 domain was added (SAR 32940).	2-61
	Table 2-86 • SmartFusion CCC/PLL Specification was revised to add information and measurements regarding CCC output peak-to-peak period jitter (SAR 32996).	2-63
	The port names in the SRAM "Timing Waveforms", SRAM "Timing Characteristics" tables, Figure 2-38 • FIFO Reset, and the FIFO "Timing Waveforms" tables were revised to ensure consistency with the software names (SAR 29991).	2-66 to 2-75
	Table 2-90 • eNVM Block Timing, Worst Commercial Case Conditions: T_J = 85°C, VCC = 1.425 V was revised to correct the maximum frequencies (SAR 32410).	2-76
	Table 2-97 • Comparator Performance Specifications was moved to the "SmartFusion DC and Switching Characteristics" section from the SmartFusion Programmable Analog User's Guide because the information is extracted from characterization (SAR 24298).	2-84
	The hysteresis section in Table 2-97 • Comparator Performance Specifications was revised (SAR 33158).	2-84
	The "SmartFusion Development Tools" was extensively updated (SAR 33216).	3-1
	The text following Table 4-2 • JTAG Pin Descriptions was updated to add information on control of the JTAGSEL pin. Manual jumpers on the evaluation and development kits allow manual selection of this function for J-Link and ULINK debuggers (SAR 25592).	4-7

Revision	Changes	Page
Revision 6 (continued)	Dynamic power values were updated in the following tables. The table subtitles changed where FPGA I/O banks were involved to note "I/O assigned to EMC I/O pins" (SAR 30987). Table 2-10 • Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings Table 2-13 • Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings.	2-10 2-11
	The "Timing Model" was updated (SAR 30986).	2-19
	Values in the timing tables for the following sections were updated. Table subtitles were updated for FPGA I/O banks to note "I/O assigned to EMC I/O pins" (SAR 30986). "Overview of I/O Performance" section: Table 2-24, Table 2-25 "Detailed I/O DC Characteristics" section: Table 2-38, Table 2-39, Table 2-40, Table 2-44, Table 2-45, Table 2-46, Table 2-50, Table 2-51, Table 2-52, Table 2-56, Table 2-57, Table 2-58, Table 2-61, Table 2-62 "LVDS" section: Table 2-65 "LVPECL" section: Table 2-68 "Global Tree Timing Characteristics" section: Table 2-80, Table 2-81	2-23 2-26 2-40 2-42 2-59
	The "PQ208" section and pin tables are new (SAR 31005).	5-34
	Global clocks were removed from the A2F060 pin table for the "CS288" and "FG256" packages, resulting in changed function names for affected pins (SAR 31033).	5-43
Revision 5 (December 2010)	Table 2-2 • Analog Maximum Ratings was revised. The recommended CM[n] pad voltage (relative to ground) was changed from –11 to –0.3 (SAR 28219).	2-2
	Table 2-7 • Temperature and Voltage Derating Factors for Timing Delays was revised to change the values for 100ºC.	2-9
	Power-down and Sleep modes, and all associated notes, were removed from Table 2-8 • Power Supplies Configuration (SAR 29479). IDC3 and IDC4 were renamed to IDC1 and IDC2 (SAR 29478). These modes are no longer supported. A note was added to the table stating that current monitors and temperature monitors should not be used when Power-down and/or Sleep mode are required by the application.	2-10
	The "Power-Down and Sleep Mode Implementation" section was deleted (SAR 29479).	N/A
	Values for PAC9 and PAC10 for LVDS and LVPECL were revised in Table 2-10 • Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings and Table 2-12 • Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings*.	2-10, 2-11
	Values for PAC1 through PAC4, PDC1, and PDC2 were added for A2F500 in Table 2-14 • Different Components Contributing to Dynamic Power Consumption in SmartFusion cSoCs and Table 2-15 • Different Components Contributing to the Static Power Consumption in SmartFusion cSoCs	2-12, 2-13
	The equation for "Total Dynamic Power Consumption—P_{DYN}" in "SoC Mode" was revised to add P_{MSS}. The "Microcontroller Subsystem Dynamic Contribution—P_{MSS}" section is new (SAR 29462).	2-14, 2-18
	Information in Table 2-24 • Summary of I/O Timing Characteristics—Software Default Settings (applicable to FPGA I/O banks) and Table 2-25 • Summary of I/O Timing Characteristics—Software Default Settings (applicable to MSS I/O banks) was updated.	2-25

Revision	Changes	Page
Revision 3 (continued)	In Table 2-3 • Recommended Operating Conditions[5,6], the VDDBAT recommended operating range was changed from "2.97 to 3.63" to "2.7 to 3.63" (SAR 25246). Recommended operating range was changed to "3.15 to 3.45" for the following voltages: VCC33A VCC33ADCx VCC33AP VCC33SDDx VCCMAINXTAL VCCLPXTAL Two notes were added to the table (SAR 27109): *1. The following 3.3 V supplies should be connected together while following proper noise filtering practices: VCC33A, VCC33ADCx, VCC33AP, VCC33SDDx, VCCMAINXTAL, and VCCLPXTAL.* *2. The following 1.5 V supplies should be connected together while following proper noise filtering practices: VCC, VCC15A, and VCC15ADCx.*	2-3
	In Table 2-3 • Recommended Operating Conditions[5,6], the description for VCCLPXTAL was corrected to change "32 Hz" to "32 KHz" (SAR 27110).	2-3
	The "Power Supply Sequencing Requirement" section is new (SAR 27178).	2-4
	Table 2-8 • Power Supplies Configuration was revised to change most on/off entries to voltages. Note 5 was added, stating that "on" means proper voltage is applied. The values of 6 µA and 16 µA were removed for IDC1 and IDC2 for 3.3 V. A note was added for IDC1 and IDC2: "Power mode and Sleep mode are consuming higher current than expected in the current version of silicon. These specifications will be updated when new version of the silicon is available" (SAR 27926).	2-10
	The "Power-Down and Sleep Mode Implementation" section is new (SAR 27178).	2-11
	A note was added to Table 2-86 • SmartFusion CCC/PLL Specification, pertaining to f_{out_CCC}, stating that "one of the CCC outputs (GLA0) is used as an MSS clock and is limited to 100 MHz (maximum) by software" (SAR 26388).	2-63
	Table 2-90 • eNVM Block Timing, Worst Commercial Case Conditions: T_J = 85°C, VCC = 1.425 V was revised. Values were included for A2F200 and A2F500, for –1 and Std. speed grades. A note was added to define 6:1:1:1 and 5:1:1:1 (SAR 26166).	2-76
	The units were corrected (mV instead of V) for input referred offset voltage, GDEC[1:0] = 00 in Table 2-96 • ABPS Performance Specifications (SAR 25381).	2-82
	The test condition values for operating current (ICC33A, typical) were changed in Table 2-99 • Voltage Regulator (SAR 26465).	2-87
	Figure 2-45 • Typical Output Voltage was revised to add legends for the three curves, stating the load represented by each (SAR 25247).	2-88
	The "SmartFusion Programming" chapter was moved to this document from the SmartFusion Subsystem Microcontroller User's Guide (SAR 26542). The "Typical Programming and Erase Times" section was added to this chapter.	4-7
	Figure 4-1 • TRSTB Logic was revised to change 1.5 V to "VJTAG (1.5 V to 3.3 V nominal)" (SAR 24694).	4-8