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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

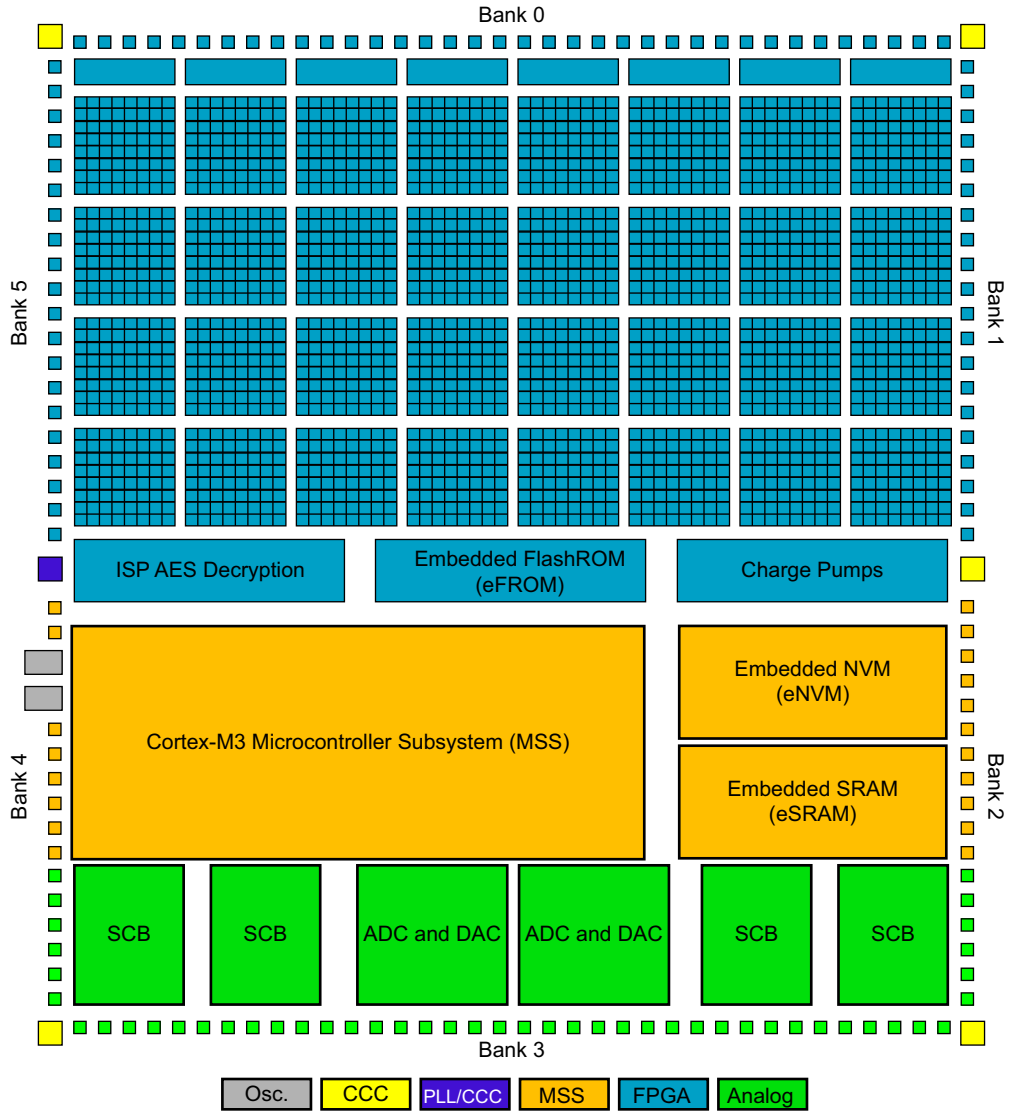
Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details	
Product Status	Obsolete
Architecture	MCU, FPGA
Core Processor	ARM® Cortex®-M3
Flash Size	128KB
RAM Size	16KB
Peripherals	DMA, POR, WDT
Connectivity	EBI/EMI, I²C, SPI, UART/USART
Speed	100MHz
Primary Attributes	ProASIC®3 FPGA, 60K Gates, 1536D-Flip-Flops
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	288-TFBGA, CSPBGA
Supplier Device Package	288-CSP (11x11)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/a2f060m3e-1csg288i

SmartFusion cSoC System Architecture



Note: Architecture for A2F200

$$P = \frac{T_J - T_A}{\theta_{JA}} = \frac{100°C - 70°C}{17.00\ W} = 1.76\ W$$

EQ 6

The 1.76 W power is less than the required 3.00 W. The design therefore requires a heat sink, or the airflow where the device is mounted should be increased. The design's total junction-to-air thermal resistance requirement can be estimated by EQ 7:

$$\theta_{JA(total)} = \frac{T_J - T_A}{P} = \frac{100°C - 70°C}{3.00\ W} = 10.00°C/W$$

EQ 7

Determining the heat sink's thermal performance proceeds as follows:

$$\theta_{JA(TOTAL)} = \theta_{JC} + \theta_{CS} + \theta_{SA}$$

EQ 8

where

θ_{JA} = 0.37°C/W

= Thermal resistance of the interface material between the case and the heat sink, usually provided by the thermal interface manufacturer

θ_{SA} = Thermal resistance of the heat sink in °C/W

$$\theta_{SA} = \theta_{JA(TOTAL)} - \theta_{JC} - \theta_{CS}$$

EQ 9

$$\theta_{SA} = 13.33°C/W - 8.28°C/W - 0.37°C/W = 5.01°C/W$$

A heat sink with a thermal resistance of 5.01°C/W or better should be used. Thermal resistance of heat sinks is a function of airflow. The heat sink performance can be significantly improved with increased airflow.

Carefully estimating thermal resistance is important in the long-term reliability of an FPGA. Design engineers should always correlate the power consumption of the device with the maximum allowable power dissipation of the package selected for that device.

Note: The junction-to-air and junction-to-board thermal resistances are based on JEDEC standard (JESD-51) and assumptions made in building the model. It may not be realized in actual application and therefore should be used with a degree of caution. Junction-to-case thermal resistance assumes that all power is dissipated through the case.

Temperature and Voltage Derating Factors

Table 2-7 • **Temperature and Voltage Derating Factors for Timing Delays (normalized to T_J = 85°C, worst-case VCC = 1.425 V)**

Array Voltage VCC (V)	Junction Temperature (°C)					
	–40°C	**0°C**	**25°C**	**70°C**	**85°C**	**100°C**
1.425	0.86	0.91	0.93	0.98	1.00	1.02
1.500	0.81	0.86	0.88	0.93	0.95	0.96
1.575	0.78	0.83	0.85	0.90	0.91	0.93

User I/O Characteristics

Timing Model

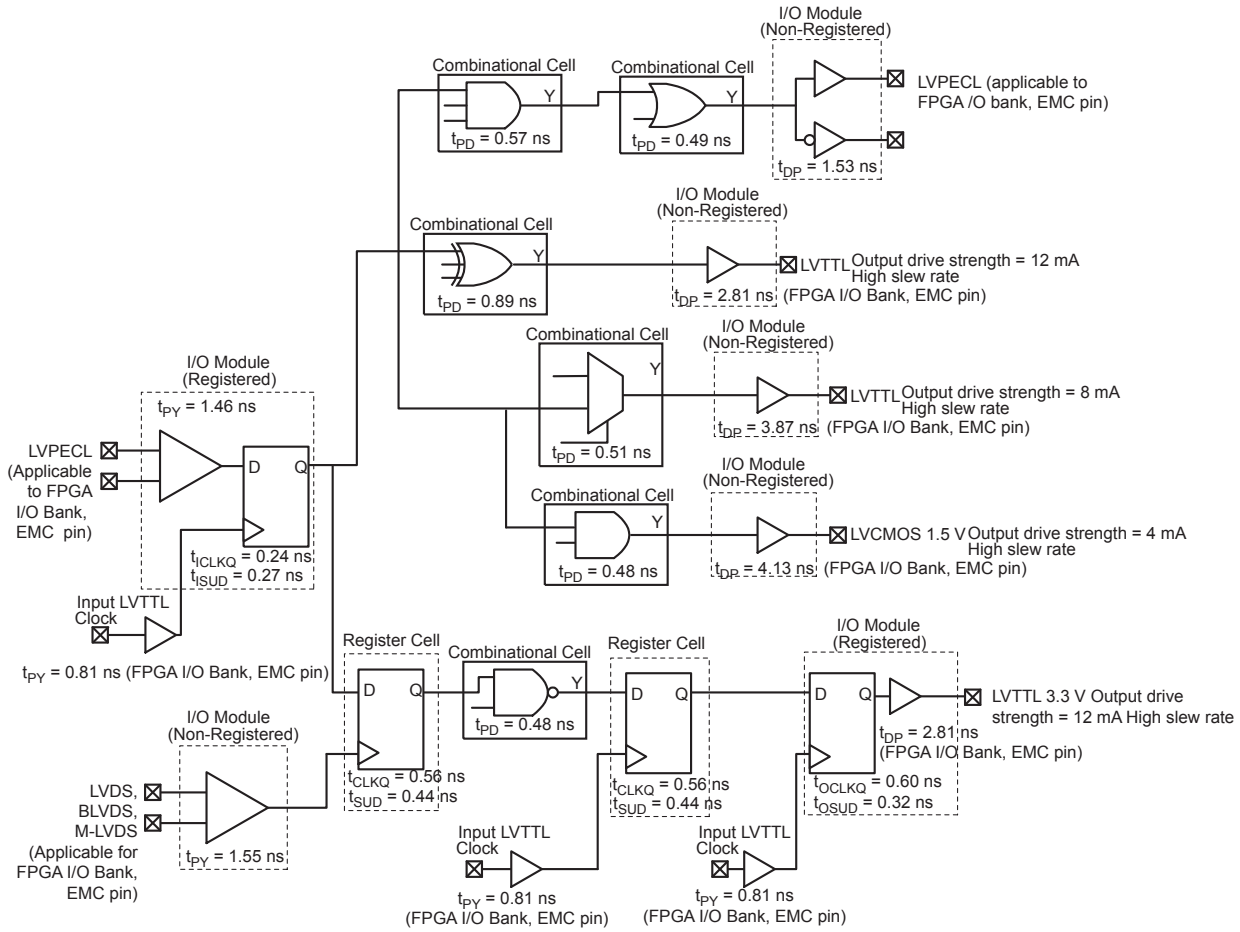


Figure 2-2 • **Timing Model**
Operating Conditions: –1 Speed, Commercial Temperature Range (T_J = 85°C), Worst Case VCC = 1.425 V

VersaTile Characteristics

VersaTile Specifications as a Combinatorial Module

The SmartFusion library offers all combinations of LUT-3 combinatorial functions. In this section, timing characteristics are presented for a sample of the library. For more details, refer to the *IGLOO/e, Fusion, ProASIC3/E, and SmartFusion Macro Library Guide*.

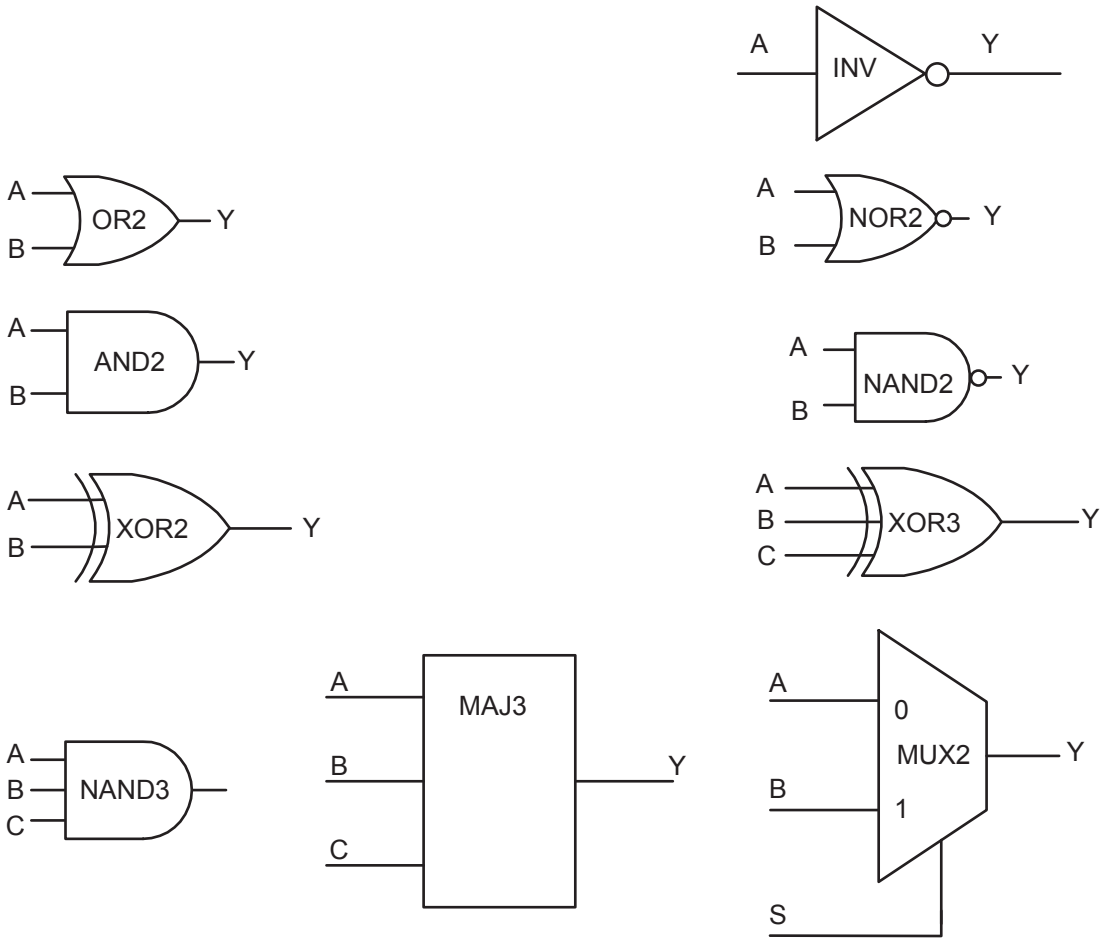


Figure 2-23 • **Sample of Combinatorial Cells**

Timing Characteristics

Table 2-78 • Combinatorial Cell Propagation Delays
Worst Commercial-Case Conditions: T_J = 85°C, Worst-Case VCC = 1.425 V

Combinatorial Cell	Equation	Parameter	–1	Std.	Units
INV	Y = !A	t_{PD}	0.41	0.49	ns
AND2	Y = A · B	t_{PD}	0.48	0.57	ns
NAND2	Y = !(A · B)	t_{PD}	0.48	0.57	ns
OR2	Y = A + B	t_{PD}	0.49	0.59	ns
NOR2	Y = !(A + B)	t_{PD}	0.49	0.59	ns
XOR2	Y = A ⊕ B	t_{PD}	0.75	0.90	ns
MAJ3	Y = MAJ(A, B, C)	t_{PD}	0.71	0.85	ns
XOR3	Y = A ⊕ B ⊕ C	t_{PD}	0.89	1.07	ns
MUX2	Y = A !S + B S	t_{PD}	0.51	0.62	ns
AND3	Y = A · B · C	t_{PD}	0.57	0.68	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.

VersaTile Specifications as a Sequential Module

The SmartFusion library offers a wide variety of sequential cells, including flip-flops and latches. Each has a data input and optional enable, clear, or preset. In this section, timing characteristics are presented for a representative sample from the library. For more details, refer to the *IGLOO/e, Fusion, ProASIC3/E, and SmartFusion Macro Library Guide*.

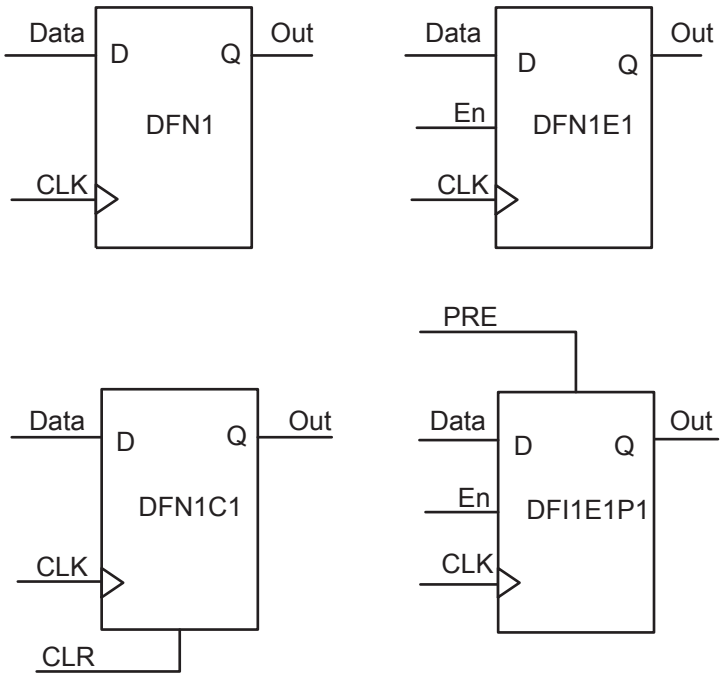


Figure 2-25 • Sample of Sequential Cells

FPGA Fabric SRAM and FIFO Characteristics

FPGA Fabric SRAM

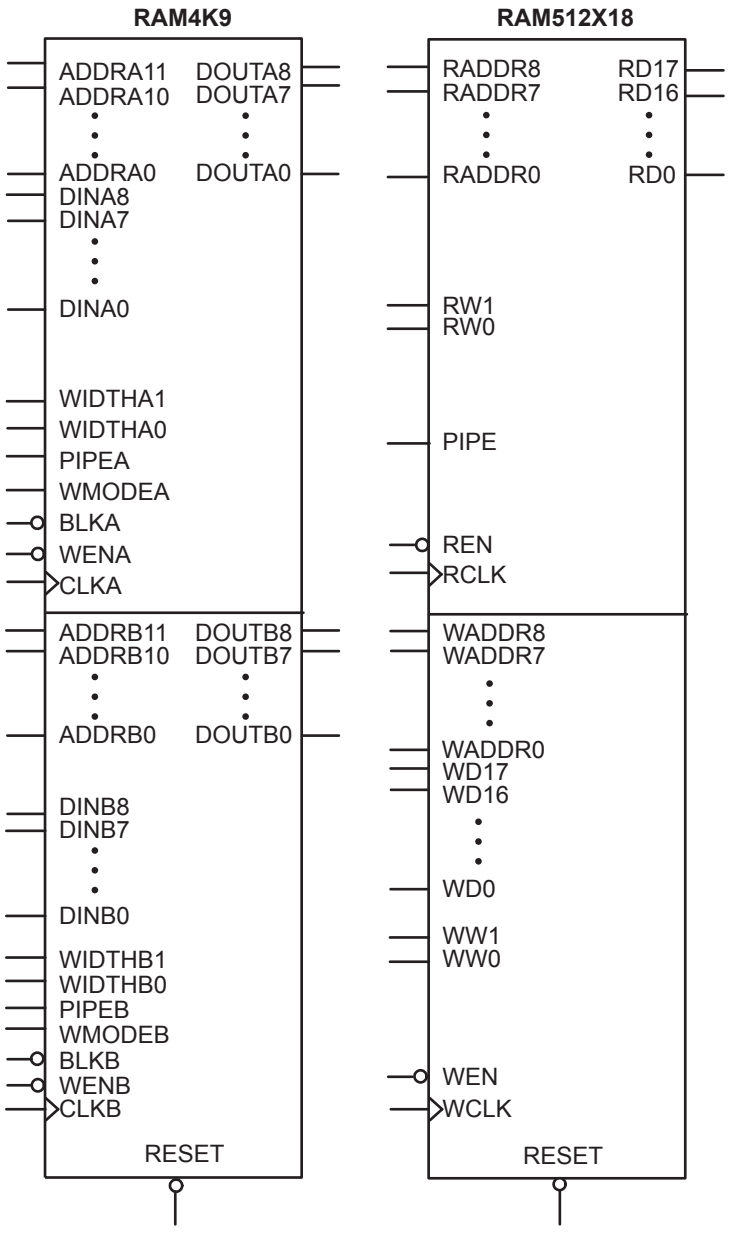


Figure 2-29 • **RAM Models**

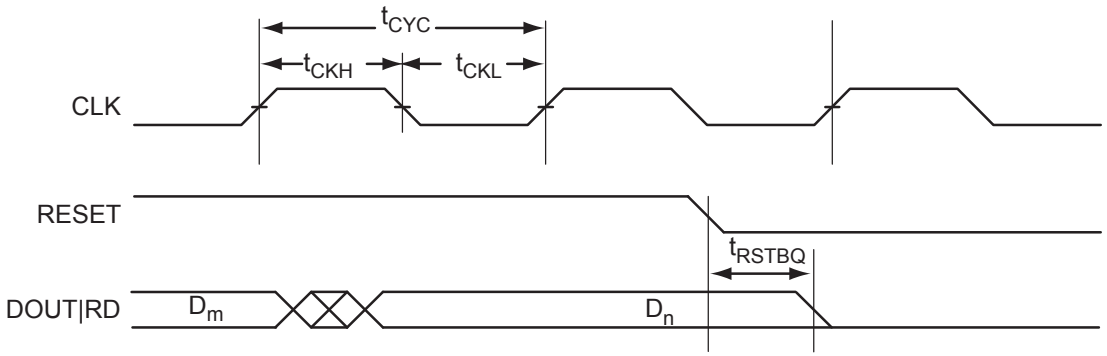


***Figure 2-34* • RAM Reset. Applicable to both RAM4K9 and RAM512x18.**

Table 2-88 • RAM512X18
Worst Commercial-Case Conditions: T_J = 85°C, Worst-Case VCC = 1.425 V

Parameter	Description	–1	Std.	Units
t_{AS}	Address setup time	0.25	0.30	ns
t_{AH}	Address hold time	0.00	0.00	ns
t_{ENS}	REN, WEN setup time	0.09	0.11	ns
t_{ENH}	REN, WEN hold time	0.06	0.07	ns
t_{DS}	Input data (WD) setup time	0.19	0.22	ns
t_{DH}	Input data (WD) hold time	0.00	0.00	ns
t_{CKQ1}	Clock High to new data valid on RD (output retained, WMODE = 0)	2.19	2.63	ns
t_{CKQ2}	Clock High to new data valid on RD (pipelined)	0.91	1.09	ns
t_{C2CRWH} [1]	Address collision clk-to-clk delay for reliable read access after write on same address—applicable to opening edge	0.38	0.43	ns
t_{C2CWRH} [1]	Address collision clk-to-clk delay for reliable write access after read on same address—applicable to opening edge	0.44	0.50	ns
t_{RSTBQ}	RESET Low to data out Low on RD (flow-through)	0.94	1.12	ns
	RESET Low to data out Low on RD (pipelined)	0.94	1.12	ns
$t_{REMRSTB}$	RESET removal	0.29	0.35	ns
$t_{RECRSTB}$	RESET recovery	1.52	1.83	ns
$t_{MPWRSTB}$	RESET minimum pulse width	0.22	0.22	ns
t_{CYC}	Clock cycle time	3.28	3.28	ns
F_{MAX}	Maximum clock frequency	305	305	MHz

Notes:

1. *For more information, refer to the Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs application note.*
2. *For the derating values at specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.*

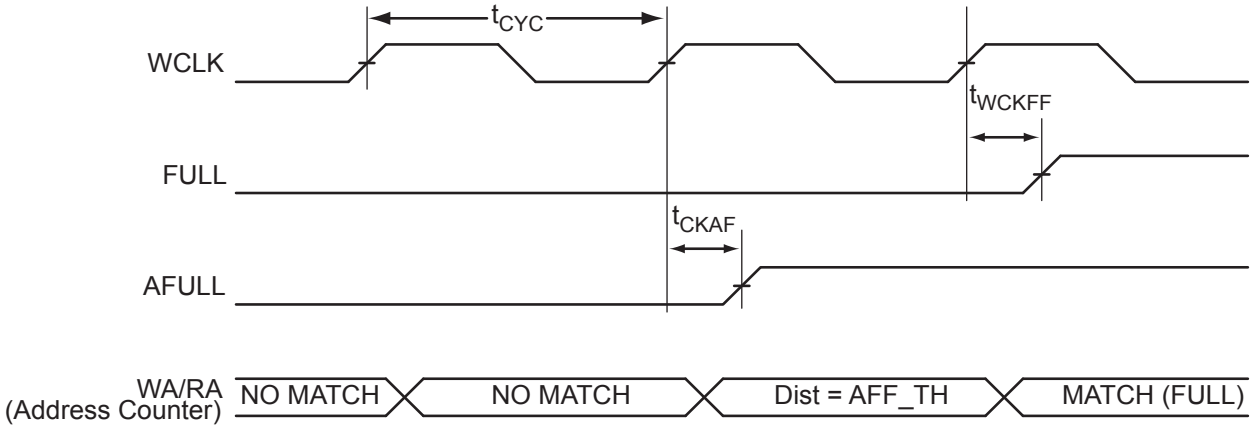


Figure 2-40 • **FIFO FULL Flag and AFULL Flag Assertion**

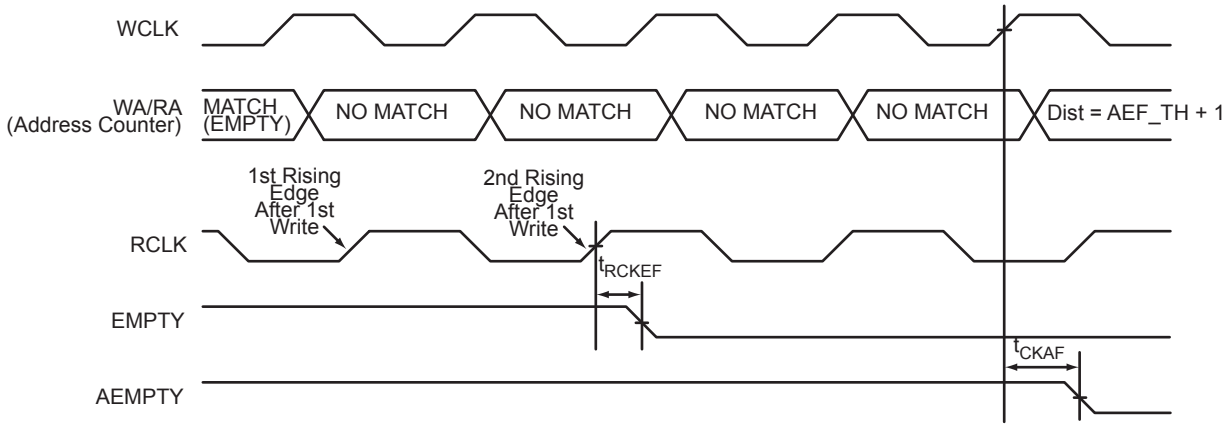


Figure 2-41 • **FIFO EMPTY Flag and AEMPTY Flag Deassertion**

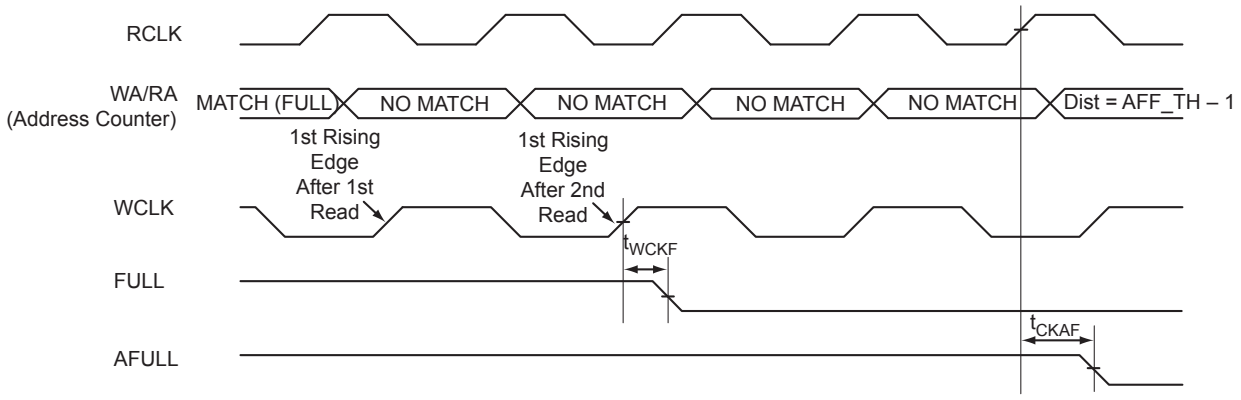


Figure 2-42 • **FIFO FULL Flag and AFULL Flag Deassertion**

Programmable Analog Specifications

Current Monitor

Unless otherwise noted, current monitor performance is specified at 25°C with nominal power supply voltages, with the output measured using the internal voltage reference with the internal ADC in 12-bit mode and 91 Ksps, after digital compensation. All results are based on averaging over 16 samples.

***Table 2-93* • Current Monitor Performance Specification**

Specification	Test Conditions	Min.	Typical	Max.	Units
Input voltage range (for driving ADC over full range)		0 – 48	0 – 50	1 – 51	mV
Analog gain	From the differential voltage across the input pads to the ADC input		50		V/V
Input referred offset voltage	Input referred offset voltage	0	0.1	0.5	mV
	–40ºC to +100ºC	0	0.1	0.5	mV
Gain error	Slope of BFSL vs. 50 V/V		±0.1	±0.5	% nom.
	–40ºC to +100ºC			±0.5	% nom.
Overall Accuracy	Peak error from ideal transfer function, 25°C		±(0.1 + 0.25%)	±(0.4 + 1.5%)	mV plus % reading
Input referred noise	0 VDC input (no output averaging)	0.3	0.4	0.5	mVrms
Common-mode rejection ratio	0 V to 12 VDC common-mode voltage	–86	–87		dB
Analog settling time	To 0.1% of final value (with ADC load)				
	From CM_STB (High)	5			µs
	From ADC_START (High)	5		200	µs
Input capacitance			8		pF
Input biased current	CM[n] or TM[n] pad, –40°C to +100°C over maximum input voltage range (plus is into pad)				
	Strobe = 0; IBIAS on CM[n]		0		µA
	Strobe = 1; IBIAS on CM[n]		1		µA
	Strobe = 0; IBIAS on TM[n]		2		µA
	Strobe = 1; IBIAS on TM[n]		1		µA
Power supply rejection ratio	DC (0 – 10 KHz)	41	42		dB
Incremental operational current monitor power supply current requirements (per current monitor instance, not including ADC or VAREFx)	VCC33A		150		µA
	VCC33AP		140		µA
	VCC15A		50		µA

Note: Under no condition should the TM pad ever be greater than 10 mV above the CM pad. This restriction is applicable only if current monitor is used.

Name	Type	Description	Associated With	
			ADC/SDD	SCB
TM0	In	SCB 0 / low side of current monitor / comparator Negative input / high side of temperature monitor. See the Temperature Monitor section.	ADC0	SCB0
TM1	In	SCB 1 / low side of current monitor / comparator. Negative input / high side of temperature monitor.	ADC0	SCB1
TM2	In	SCB 2 / low side of current monitor / comparator. Negative input / high side of temperature monitor.	ADC1	SCB2
TM3	In	SCB 3 low side of current monitor / comparator. Negative input / high side of temperature monitor.	ADC1	SCB3
TM4	In	SCB 4 low side of current monitor / comparator. Negative input / high side of temperature monitor.	ADC2	SCB4
SDD0	Out	Output of SDD0 See the Sigma-Delta Digital-to-Analog Converter (DAC) section in the *SmartFusion Programmable Analog User's Guide*.	SDD0	N/A
SDD1	Out	Output of SDD1	SDD1	N/A
SDD2	Out	Output of SDD2	SDD2	N/A

Note: Unused analog inputs should be grounded. This aids in shielding and prevents an undesired coupling path.

TQ144	
Pin Number	**A2F060 Function**
1	VCCPLL0
2	VCOMPLA0
3	GNDQ
4	GFA2/IO42PDB5V0
5	GFB2/IO42NDB5V0
6	GFC2/IO41PDB5V0
7	IO41NDB5V0
8	VCC
9	GND
10	VCCFPGAIOB5
11	IO38PDB5V0
12	IO38NDB5V0
13	IO36PDB5V0
14	IO36NDB5V0
15	GND
16	GNDRCOSC
17	VCCRCOSC
18	MSS_RESET_N
19	GPIO_0/IO33RSB4V0
20	GPIO_1/IO32RSB4V0
21	GPIO_2/IO31RSB4V0
22	GPIO_3/IO30RSB4V0
23	GPIO_4/IO29RSB4V0
24	GND
25	VCCMSSIOB4
26	VCC
27	GPIO_5/IO28RSB4V0
28	GPIO_6/IO27RSB4V0
29	GPIO_7/IO26RSB4V0
30	GPIO_8/IO25RSB4V0
31	VCCESRAM
32	GNDSDD0
33	VCC33SDD0
34	VCC15A
35	PCAP
36	NCAP

TQ144	
Pin Number	**A2F060 Function**
37	VCC33AP
38	VCC33N
39	SDD0
40	GNDA
41	GNDAQ
42	GNDAQ
43	ADC0
44	ADC1
45	ADC2
46	ADC3
47	ADC4
48	ADC5
49	ADC6
50	ADC7
51	ADC8
52	ADC9
53	ADC10
54	NC
55	NC
56	NC
57	GND15ADC0
58	VCC15ADC0
59	GND33ADC0
60	VCC33ADC0
61	GND33ADC0
62	VAREF0
63	ABPS0
64	ABPS1
65	CM0
66	TM0
67	GNDTM0
68	GNDAQ
69	GNDA
70	GNDVAREF
71	VAREFOUT
72	PU_N

Pin No.	CS288		
	A2F060 Function	A2F200 Function	A2F500 Function
C21	IO17NDB0V0	GBA2/IO20PDB1V0	GBA2/IO27PDB1V0
D1	EMC_DB[14]/IO45NDB5V0	EMC_DB[14]/GAB2/IO71NDB5V0	EMC_DB[14]/GAB2/IO88NDB5V0
D3	VCCFPGAIOB5	VCCFPGAIOB5	VCCFPGAIOB5
D19	GND	GND	GND
D21	VCCFPGAIOB1	VCCFPGAIOB1	VCCFPGAIOB1
E1	EMC_DB[13]/IO44PDB5V0	EMC_DB[13]/GAC2/IO70PDB5V0	EMC_DB[13]/GAC2/IO87PDB5V0
E3	EMC_DB[12]/IO44NDB5V0	EMC_DB[12]/IO70NDB5V0	EMC_DB[12]/IO87NDB5V0
E5	GNDQ	GNDQ	GNDQ
E6	EMC_BYTEN[0]/IO02NDB0V0	EMC_BYTEN[0]/GAC0/IO02NDB0V0	EMC_BYTEN[0]/GAC0/IO07NDB0V0
E7	EMC_BYTEN[1]/IO02PDB0V0	EMC_BYTEN[1]/GAC1/IO02PDB0V0	EMC_BYTEN[1]/GAC1/IO07PDB0V0
E8	EMC_OEN1_N/IO03PDB0V0	EMC_OEN1_N/IO03PDB0V0	EMC_OEN1_N/IO08PDB0V0
E9	EMC_AB[3]/IO05PDB0V0	EMC_AB[3]/IO05PDB0V0	EMC_AB[3]/IO09PDB0V0
E10	EMC_AB[10]/IO09NDB0V0	EMC_AB[10]/IO09NDB0V0	EMC_AB[10]/IO11NDB0V0
E11	EMC_AB[7]/IO07PDB0V0	EMC_AB[7]/IO07PDB0V0	EMC_AB[7]/IO12PDB0V0
E12	EMC_AB[13]/IO10PDB0V0	EMC_AB[13]/IO10PDB0V0	EMC_AB[13]/IO14PDB0V0
E13	EMC_AB[16]/IO12NDB0V0	EMC_AB[16]/IO12NDB0V0	EMC_AB[16]/IO17NDB0V0
E14	EMC_AB[17]/IO12PDB0V0	EMC_AB[17]/IO12PDB0V0	EMC_AB[17]/IO17PDB0V0
E15	GCC0/IO18NPB0V0	GCB0/IO27NDB1V0	GCB0/IO34NDB1V0
E16	GCA1/IO20PPB0V0	GCB1/IO27PDB1V0	GCB1/IO34PDB1V0
E17	GCC1/IO18PPB0V0	GCB2/IO24PDB1V0	GCB2/IO33PDB1V0
E19	GCB2/IO22PPB1V0	GCA0/IO28NDB1V0	GCA0/IO36NDB1V0 *
E21	IO21NDB1V0	GCA1/IO28PDB1V0	GCA1/IO36PDB1V0 *
F1	VCCFPGAIOB5	VCCFPGAIOB5	VCCFPGAIOB5
F3	GFB2/IO42NDB5V0	GFB2/IO68NDB5V0	GFB2/IO85NDB5V0
F5	GFA2/IO42PDB5V0	GFA2/IO68PDB5V0	GFA2/IO85PDB5V0
F6	EMC_DB[11]/IO43PDB5V0	EMC_DB[11]/IO69PDB5V0	EMC_DB[11]/IO86PDB5V0
F7	GND	GND	GND
F8	NC	GFC1/IO66PPB5V0	GFC1/IO83PPB5V0
F9	VCCFPGAIOB0	VCCFPGAIOB0	VCCFPGAIOB0
F10	EMC_AB[11]/IO09PDB0V0	EMC_AB[11]/IO09PDB0V0	EMC_AB[11]/IO11PDB0V0
F11	EMC_AB[6]/IO07NDB0V0	EMC_AB[6]/IO07NDB0V0	EMC_AB[6]/IO12NDB0V0

Notes:

1. *Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.*
2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*

Pin No.	CS288		
	A2F060 Function	A2F200 Function	A2F500 Function
H19	VCCFPGAIOB1	VCCFPGAIOB1	VCCFPGAIOB1
H21	NC	GDB2/IO33PDB1V0	GDB2/IO42PDB1V0
J1	EMC_DB[4]/IO38NPB5V0	EMC_DB[4]/GEA0/IO61NPB5V0	EMC_DB[4]/GEA0/IO78NPB5V0
J3	EMC_DB[8]/IO40NPB5V0	EMC_DB[8]/GEC0/IO63NPB5V0	EMC_DB[8]/GEC0/IO80NPB5V0
J5	EMC_DB[1]/IO36PDB5V0	EMC_DB[1]/GEB2/IO59PDB5V0	EMC_DB[1]/GEB2/IO76PDB5V0
J6	EMC_DB[6]/IO39NDB5V0	EMC_DB[6]/GEB0/IO62NDB5V0	EMC_DB[6]/GEB0/IO79NDB5V0
J7	VCCFPGAIOB5	VCCFPGAIOB5	VCCFPGAIOB5
J8	VCC	VCC	VCC
J9	GND	GND	GND
J10	VCC	VCC	VCC
J11	GND	GND	GND
J12	VCC	VCC	VCC
J13	GND	GND	GND
J14	VCC	VCC	VCC
J15	VPP	VPP	VPP
J16	NC	IO32NPB1V0	IO41NPB1V0
J17	NC	GNDQ	GNDQ
J19	VCCMAINXTAL	VCCMAINXTAL	VCCMAINXTAL
J21	NC	GDA2/IO33NDB1V0	GDA2/IO42NDB1V0
K1	GND	GND	GND
K3	EMC_DB[5]/IO38PPB5V0	EMC_DB[5]/GEA1/IO61PPB5V0	EMC_DB[5]/GEA1/IO78PPB5V0
K5	EMC_DB[0]/IO36NDB5V0	EMC_DB[0]/GEA2/IO59NDB5V0	EMC_DB[0]/GEA2/IO76NDB5V0
K6	EMC_DB[3]/IO37PPB5V0	EMC_DB[3]/GEC2/IO60PPB5V0	EMC_DB[3]/GEC2/IO77PPB5V0
K8	GND	GND	GND
K9	VCC	VCC	VCC
K10	GND	GND	GND
K11	VCC	VCC	VCC
K12	GND	GND	GND
K13	VCC	VCC	VCC
K14	GND	GND	GND
K16	LPXOUT	LPXOUT	LPXOUT

Notes:

1. *Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.*
2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*

PQ208

Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx.

Pin Number	FG484	
	A2F200 Function	A2F500 Function
U13	NC	GNDTM2
U14	NC	ADC11
U15	GNDVAREF	GNDVAREF
U16	VCC33SDD1	VCC33SDD1
U17	SPI_0_DO/GPIO_16	SPI_0_DO/GPIO_16
U18	UART_0_RXD/GPIO_21	UART_0_RXD/GPIO_21
U19	VCCMSSIOB2	VCCMSSIOB2
U20	I2C_1_SCL/GPIO_31	I2C_1_SCL/GPIO_31
U21	I2C_0_SCL/GPIO_23	I2C_0_SCL/GPIO_23
U22	GND	GND
V1	GPIO_0/IO47RSB4V0	GPIO_0/IO56RSB4V0
V2	GPIO_6/IO41RSB4V0	GPIO_6/IO50RSB4V0
V3	GPIO_9/IO38RSB4V0	GPIO_9/IO47RSB4V0
V4	MAC_MDIO/IO49RSB4V0	MAC_MDIO/IO58RSB4V0
V5	MAC_RXD[0]/IO54RSB4V0	MAC_RXD[0]/IO63RSB4V0
V6	GND	GND
V7	SDD0	SDD0
V8	ABPS1	ABPS1
V9	ADC2	ADC2
V10	VCC33ADC0	VCC33ADC0
V11	ADC6	ADC6
V12	ADC5	ADC5
V13	ABPS5	ABPS5
V14	NC	ADC8
V15	NC	GND33ADC2
V16	NC	NC
V17	GND	GND
V18	SPI_0_DI/GPIO_17	SPI_0_DI/GPIO_17
V19	SPI_1_DI/GPIO_25	SPI_1_DI/GPIO_25
V20	UART_1_TXD/GPIO_28	UART_1_TXD/GPIO_28
V21	I2C_0_SDA/GPIO_22	I2C_0_SDA/GPIO_22
V22	I2C_1_SDA/GPIO_30	I2C_1_SDA/GPIO_30
W1	GPIO_2/IO45RSB4V0	GPIO_2/IO54RSB4V0
W2	GPIO_7/IO40RSB4V0	GPIO_7/IO49RSB4V0

Notes:

1. *Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.*
2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*

Revision	Changes	Page
Revision 10 (January 2013)	The "SmartFusion cSoC Family Product Table" section has been updated to specify that External Memory Controller support for A2F060-TQ144 is not available (SAR 41555).	II
	The following Note was added to the "Package I/Os: MSS + FPGA I/Os" table (SAR 41027): "There are no LVTTL capable direct inputs available on A2F060 devices."	III
	The "Product Ordering Codes" section has been updated to mention "Y" as "Blank" mentioning "Device Does Not Include License to Implement IP Based on the Cryptography Research, Inc. (CRI) Patent Portfolio" (SAR 43218).	VI
	Added a note to Table 2-3 • Recommended Operating Conditions[5,6] (SAR 43428): The programming temperature range supported is $T_{ambient}$ = 0°C to 85°C.	2-3
	Statements about the state of the I/Os during programming were updated in the following sections: "I/O Power-Up and Supply Voltage Thresholds for Power-On Reset (Commercial and Industrial)" and "User I/O Naming Conventions" (SAR 43380).	2-4, 5-7
	In Table 2-4 • FPGA and Embedded Flash Programming, Storage and Operating Limits, the upper value of temperature ranges was corrected from "Min." to "Max." (SAR 41826).	2-4
	Information for A2F200M3F-CS288 was added to Table 2-6 • Package Thermal Resistance. The die size column was removed (SARs 41828, 42168). Also added details for A2F200M3F-PQG208I (SAR 35728).	2-7
	Added the following note to Table 2-65 • LVDS and Table 2-68 • LVPECL: "The above mentioned timing parameters correspond to 24mA drive strength." (SAR 43457)	2-41, 2-43
	The note in Table 2-86 • SmartFusion CCC/PLL Specification referring the reader to SmartGen was revised to refer instead to the online help associated with the core (SAR 34816).	2-63
	The SRAM collision data in Table 2-87 • RAM4K9 and Table 2-88 • RAM512X18 was updated (SAR 38583).	2-69,2-70
	The maximum input bias current for comparators 1, 3, 5, 7, and 9, in Table 2-97 • Comparator Performance Specifications, was revised from 60 to 100 nA (SAR 36008).	2-84

Revision	Changes	Page
Revision 9 (continued)	The following note was added to Table 2-86 • SmartFusion CCC/PLL Specification in regard to delay increments in programmable delay blocks (SAR 34816): "When the CCC/PLL core is generated by Microsemi core generator software, not all delay values of the specified delay increments are available. Refer to SmartGen online help for more information."	2-63
	Figure 2-36 • FIFO Read and Figure 2-37 • FIFO Write have been added (SAR 34851).	2-72
	Information regarding the MSS resetting itself after IAP of the FPGA fabric was added to the "Reprogramming the FPGA Fabric Using the Cortex-M3" section (SAR 37970).	4-8
	Instructions for unused VCC33ADCx pins were revised in "Supply Pins" (SAR 41137).	5-1
	Libero IDE was changed to Libero SoC throughout the document (SAR 40264).	N/A
Revision 8 (March 2012)	In the "Analog Front-End (AFE)" section, the resolution for the first-order sigma delta DAC was corrected from 12-bit to "8-bit, 16-bit, or 24-bit." The same correction was made in the "SmartFusion cSoC Family Product Table" (SAR 36541).	I, II
	The "SmartFusion cSoC Family Product Table" was revised to break out the features by package as well as device. The table now indicates that only one SPI is available for the PQ208 package in A2F200 and A2F500, and in the TQ144 package for A2F060 (SAR 33477). The EMC address bus size has been corrected to 26 bits (SAR 35664).	II
	The "SmartFusion cSoC Device Status" table was revised to change the CS288 package for A2F200 and A2F500 from preliminary to production status (SAR 37811).	III
	TQ144 package information for A2F060 was added to the "Package I/Os: MSS + FPGA I/Os" table, "SmartFusion cSoC Device Status" table, "Product Ordering Codes", and "Temperature Grade Offerings" table (SAR 36246).	III, VI
	Table 1 • SmartFusion cSoC Package Sizes Dimensions is new (SAR 31178).	III
	The Halogen-Free Packaging code (H) was removed from the "Product Ordering Codes" table (SAR 34017).	VI
	The "Specifying I/O States During Programming" section is new (SAR 34836).	1-3
	The reference to guidelines for global spines and VersaTile rows, given in the "Global Clock Dynamic Contribution—P_{CLOCK}" section, was corrected to the "Device Architecture" chapter in the *SmartFusion FPGA Fabric User's Guide* (SAR 34742).	2-15
	The AC Loading figures in the "Single-Ended I/O Characteristics" section were updated to match tables in the "Summary of I/O Timing Characteristics – Default I/O Software Settings" section (SAR 34891).	2-30, 2-24
	The following sentence was deleted from the "2.5 V LVCMOS" section (SAR 34799): "It uses a 5 V–tolerant input buffer and push-pull output buffer."	2-32
	In the SRAM "Timing Characteristics" tables, reference was made to a new application note, *Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs*, which covers these cases in detail (SAR 34874).	2-69
	The note for Table 2-93 • Current Monitor Performance Specification was modified to include the statement that the restriction on the TM pad being no greater than 10 mV above the CM pad.is applicable only if current monitor is used (SAR 26373).	2-78
	The unit "FR" in Table 2-96 • ABPS Performance Specifications and Table 2-98 • Analog Sigma-Delta DAC, used to designate full-scale error, was changed to "FS" and clarified with a table note (SAR 35342).	2-82, 2-85

Revision	Changes	Page
Revision 3 (continued)	Two notes were added to the "Supply Pins" table (SAR 27109): 1. *The following supplies should be connected together while following proper noise filtering practices: VCC33A, VCC33ADCx, VCC33AP, VCC33SDDx, VCCMAINXTAL, and VCCLPXTAL.* 2. *The following 1.5 V supplies should be connected together while following proper noise filtering practices: VCC, VCC15A, and VCC15ADCx.*	5-1
	The descriptions for the "VCC33N", "NCAP", and "PCAP" pins were revised to include information on what to do if analog SCB features and SDDs are not used (SAR 26744).	5-2, 5-9, 5-9
	Information was added to the "User Pins" table regarding tristating of used and unused GPIO pins. The IO portion of the table was revised to state that unused I/O pins are disabled by Libero IDE software and include a weak pull-up resistor (SAR 26890). Information was added regarding behavior of used I/O pins during power-up.	5-6
	The type for "EMC_RW_N" was changed from In/out to Out (SAR 25113).	5-12
	A note was added to the "Analog Front-End (AFE)" table stating that unused analog inputs should be grounded (SAR 26744).	5-14
	The "TQ144" section is new, with pin tables for A2F200 and A2F500 (SAR 27044).	5-18
	The "FG256" pin table was replaced and now includes "Handling When Unused" information (SAR 27709).	5-42
Revision 2 (May 2010)	Embedded nonvolatile flash memory (eNVM) was changed from "64 to 512 Kbytes" to "128 to 512 Kbytes" in the "Microcontroller Subsystem (MSS)" section and "SmartFusion cSoC Family Product Table" (SAR 26005).	I, II
	The main oscillator range of values was changed to "32 KHz to 20 MHz" in the "Microcontroller Subsystem (MSS)" section and the "SmartFusion cSoC Family Product Table" (SAR 24906).	I, II
	The value for t_{PD} was changed from 50 ns to 15 ns for the high-speed voltage comparators listed in the "Analog Front-End (AFE)" section (SAR 26005).	I
	The number of PLLs for A2F200 was changed from 2 to 1 in the "SmartFusion cSoC Family Product Table" (SAR 25093).	II
	Values for direct analog input, total analog input, and total I/Os were updated for the FG256 package, A2F060, in the "Package I/Os: MSS + FPGA I/Os" table. The Max. column was removed from the table (SAR 26005).	III
	The Speed Grade section of the "Product Ordering Codes" table was revised (SAR 25257).	VI
Revision 1 (March 2010)	The "Product Ordering Codes" table was revised to add "blank" as an option for lead-free packaging and application (junction temperature range).	VI
	Table 2-3 • Recommended Operating Conditions[5,6] was revised. Ta (ambient temperature) was replaced with T_J (junction temperature).	2-3
	PDC5 was deleted from Table 2-15 • Different Components Contributing to the Static Power Consumption in SmartFusion cSoCs.	2-13
	The formulas in the footnotes for Table 2-29 • I/O Weak Pull-Up/Pull-Down Resistances were revised.	2-27
	The values for input biased current were revised in Table 2-93 • Current Monitor Performance Specification.	2-78
Revision 0 (March 2010)	The "Analog Front-End (AFE)" section was updated to change the throughput for 10-bit mode from 600 Ksps to 550 Ksps.	I