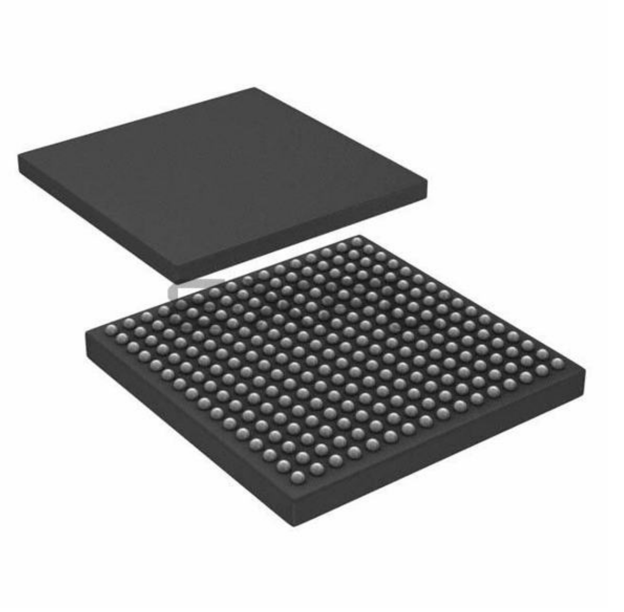
Microsemi Corporation - A2F060M3E-1FG256 Datasheet



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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details	
Product Status	Obsolete
Architecture	MCU, FPGA
Core Processor	ARM® Cortex®-M3
Flash Size	128KB
RAM Size	16KB
Peripherals	DMA, POR, WDT
Connectivity	EBI/EMI, I²C, SPI, UART/USART
Speed	100MHz
Primary Attributes	ProASIC®3 FPGA, 60K Gates, 1536D-Flip-Flops
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/a2f060m3e-1fg256

Table 2-11 • **Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings Applicable to MSS I/O Banks**

	VCCMSSIOBx (V)	Static Power PDC7 (mW)	Dynamic Power PAC9 (µW/MHz)
Single-Ended			
3.3 V LVTTL / 3.3 V LVCMOS	3.3	–	17.21
3.3 V LVCMOS / 3.3 V LVCMOS – Schmitt trigger	3.3	–	20.00
2.5 V LVCMOS	2.5	–	5.55
2.5 V LVCMOS – Schmitt trigger	2.5	–	7.03
1.8 V LVCMOS	1.8	–	2.61
1.8 V LVCMOS – Schmitt trigger	1.8	–	2.72
1.5 V LVCMOS (JESD8-11)	1.5	–	1.98
1.5 V LVCMOS (JESD8-11) – Schmitt trigger	1.5	–	1.93

Table 2-12 • **Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings* Applicable to FPGA I/O Banks, I/O Assigned to EMC I/O Pins**

	C_{LOAD} (pF)	VCCFPGAIOBx (V)	Static Power PDC8 (mW)	Dynamic Power PAC10 (µW/MHz)
Single-Ended				
3.3 V LVTTL / 3.3 V LVCMOS	35	3.3	–	475.66
2.5 V LVCMOS	35	2.5	–	270.50
1.8 V LVCMOS	35	1.8	–	152.17
1.5 V LVCMOS (JESD8-11)	35	1.5	–	104.44
3.3 V PCI	10	3.3	–	202.69
3.3 V PCI-X	10	3.3	–	202.69
Differential				
LVDS	–	2.5	7.74	88.26
LVPECL	–	3.3	19.54	164.99

*Note: *Dynamic power consumption is given for standard load and software default drive strength and output slew.*

Table 2-13 • **Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings Applicable to MSS I/O Banks**

	C_{LOAD} (pF)	VCCMSSIOBx (V)	Static Power PDC8 (mW)[2]	Dynamic Power PAC10 (µW/MHz)[3]
Single-Ended				
3.3 V LVTTL / 3.3 V LVCMOS	10	3.3	–	155.65
2.5 V LVCMOS	10	2.5	–	88.23
1.8 V LVCMOS	10	1.8	–	45.03
1.5 V LVCMOS (JESD8-11)	10	1.5	–	31.01

Standby Mode and Time Keeping Mode

P_{NET} = 0 W

I/O Input Buffer Dynamic Contribution—P_{INPUTS}

SoC Mode

$P_{INPUTS} = N_{INPUTS} * (\alpha_2 / 2) * P_{AC9} * F_{CLK}$

Where:

N_{INPUTS} is the number of I/O input buffers used in the design.

α_2 is the I/O buffer toggle rate—guidelines are provided in Table 2-17 on page 2-18.

F_{CLK} is the global clock signal frequency.

Standby Mode and Time Keeping Mode

P_{INPUTS} = 0 W

I/O Output Buffer Dynamic Contribution—$P_{OUTPUTS}$

SoC Mode

$P_{OUTPUTS} = N_{OUTPUTS} * (\alpha_2 / 2) * \beta_1 * P_{AC10} * F_{CLK}$

Where:

$N_{OUTPUTS}$ is the number of I/O output buffers used in the design.

α_2 is the I/O buffer toggle rate—guidelines are provided in Table 2-17 on page 2-18.

β_1 is the I/O buffer enable rate—guidelines are provided in Table 2-18 on page 2-18.

F_{CLK} is the global clock signal frequency.

Standby Mode and Time Keeping Mode

$P_{OUTPUTS}$ = 0 W

FPGA Fabric SRAM Dynamic Contribution—P_{MEMORY}

SoC Mode

$P_{MEMORY} = (N_{BLOCKS} * P_{AC11} * \beta_2 * F_{READ\text{-}CLOCK}) + (N_{BLOCKS} * P_{AC12} * \beta_3 * F_{WRITE\text{-}CLOCK})$

Where:

N_{BLOCKS} is the number of RAM blocks used in the design.

$F_{READ\text{-}CLOCK}$ is the memory read clock frequency.

β_2 is the RAM enable rate for read operations—guidelines are provided in Table 2-18 on page 2-18.

β_3 the RAM enable rate for write operations—guidelines are provided in Table 2-18 on page 2-18.

$F_{WRITE\text{-}CLOCK}$ is the memory write clock frequency.

Standby Mode and Time Keeping Mode

P_{MEMORY} = 0 W

PLL/CCC Dynamic Contribution—P_{PLL}

SoC Mode

$P_{PLL} = P_{AC13} * F_{CLKOUT}$

F_{CLKIN} is the input clock frequency.

F_{CLKOUT} is the output clock frequency.[1]

Standby Mode and Time Keeping Mode

---

[1] *The PLL dynamic contribution depends on the input clock frequency, the number of output clock signals generated by the PLL, and the frequency of each output clock. If a PLL is used to generate more than one output clock, include each output clock in the formula output clock by adding its corresponding contribution ($P_{AC14} * F_{CLKOUT}$ product) to the total PLL contribution.*

Timing Characteristics

Table 2-56 • 1.5 V LVCMOS High Slew
Worst Commercial-Case Conditions: T_J = 85°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCxxxxIOBx = 1.425 V
Applicable to FPGA I/O Banks, I/O Assigned to EMC I/O Pins

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 m	Std.	0.60	7.79	0.04	1.34	0.39	6.43	7.79	3.19	2.59	8.49	9.85	ns
	–1	0.50	6.49	0.03	1.12	0.32	5.36	6.49	2.66	2.16	7.08	8.21	ns
4 mA	Std.	0.60	4.95	0.04	1.34	0.39	4.61	4.96	3.53	3.19	6.67	7.02	ns
	–1	0.50	4.13	0.03	1.12	0.32	3.85	4.13	2.94	2.66	5.56	5.85	ns
6 mA	Std.	0.60	4.36	0.04	1.34	0.39	4.34	4.36	3.60	3.34	6.40	6.42	ns
	–1	0.50	3.64	0.03	1.12	0.32	3.62	3.64	3.00	2.78	5.33	5.35	ns
8 mA	Std.	0.60	3.89	0.04	1.34	0.39	3.96	3.34	3.72	3.92	6.02	5.40	ns
	–1	0.50	3.24	0.03	1.12	0.32	3.30	2.79	3.10	3.27	5.02	4.50	ns
12 mA	Std.	0.60	3.89	0.04	1.34	0.39	3.96	3.34	3.72	3.92	6.02	5.40	ns
	–1	0.50	3.24	0.03	1.12	0.32	3.30	2.79	3.10	3.27	5.02	4.50	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.*

Table 2-57 • 1.5 V LVCMOS Low Slew
Worst Commercial-Case Conditions: T_J = 85°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCxxxxIOBx = 1.4 V
Applicable to FPGA I/O Banks, I/O Assigned to EMC I/O Pins

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.60	11.96	0.04	1.34	0.39	12.18	11.70	3.20	2.47	14.24	13.76	ns
	–1	0.50	9.96	0.03	1.12	0.32	10.15	9.75	2.67	2.06	11.86	11.46	ns
4 mA	Std.	0.60	9.51	0.04	1.34	0.39	9.68	8.76	3.54	3.07	11.74	10.82	ns
	–1	0.50	7.92	0.03	1.12	0.32	8.07	7.30	2.95	2.56	9.79	9.02	ns
6 mA	Std.	0.60	8.86	0.04	1.34	0.39	9.03	8.17	3.61	3.22	11.08	10.23	ns
	–1	0.50	7.39	0.03	1.12	0.32	7.52	6.81	3.01	2.68	9.24	8.52	ns
8 mA	Std.	0.60	8.44	0.04	1.34	0.39	8.60	8.18	3.73	3.78	10.66	10.24	ns
	–1	0.50	7.04	0.03	1.12	0.32	7.17	6.82	3.11	3.15	8.88	8.53	ns
12 mA	Std.	0.60	8.44	0.04	1.34	0.39	8.60	8.18	3.73	3.78	10.66	10.24	ns
	–1	0.50	7.04	0.03	1.12	0.32	7.17	6.82	3.11	3.15	8.88	8.53	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.

Table 2-58 • 1.5 V LVCMOS High Slew
Worst Commercial-Case Conditions: T_J = 85°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCxxxxIOBx = 3.0 V
Applicable to MSS I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	0.22	3.24	0.09	1.28	1.86	0.22	3.30	3.20	2.24	2.21	ns
	–1	0.18	2.70	0.07	1.07	1.55	0.18	2.75	2.67	1.87	1.85	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.*

Main and Lower Power Crystal Oscillator

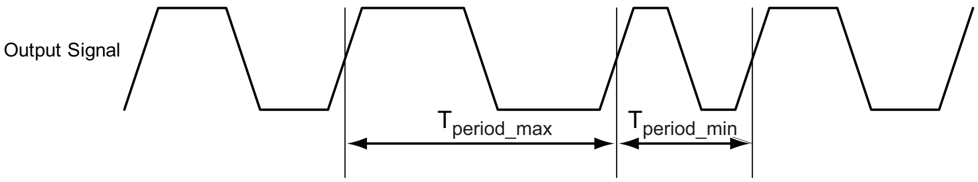
The tables below describes the electrical characteristics of the main and low power crystal oscillator.

***Table 2-84* • Electrical Characteristics of the Main Crystal Oscillator**

Parameter	Description	Condition	Min.	Typ.	Max.	Units
	Operating frequency	Using external crystal	0.032		20	MHz
		Using ceramic resonator	0.5		8	MHz
		Using RC Network	0.032		4	MHz
	Output duty cycle			50		%
	Output jitter	With 10 MHz crystal		1		ns RMS
IDYNXTAL	Operating current	RC		0.6		mA
		0.032–0.2		0.6		mA
		0.2–2.0		0.6		mA
		2.0–20.0		0.6		mA
ISTBXTAL	Standby current of crystal oscillator			10		µA
PSRRXTAL	Power supply noise tolerance			0.5		Vp-p
VIHXTAL	Input logic level High		90% of VCC			V
VILXTAL	Input logic level Low				10% of VCC	V
	Startup time	RC [Tested at 3.24Mhz]		300	550	µs
		0.032–0.2 [Tested at 32KHz]		500	3,000	µs
		0.2–2.0 [Tested at 2MHz]		8	12	µs
		2.0–20.0 [Tested at 20MHz]		160	180	µs

***Table 2-85* • Electrical Characteristics of the Low Power Oscillator**

Parameter	Description	Condition	Min.	Typ.	Max.	Units
	Operating frequency			32		KHz
	Output duty cycle			50		%
	Output jitter			30		ns RMS
IDYNXTAL	Operating current	32 KHz		10		µA
ISTBXTAL	Standby current of crystal oscillator			2		µA
PSRRXTAL	Power supply noise tolerance			0.5		Vp-p
VIHXTAL	Input logic level High		90% of VCC			V
VILXTAL	Input logic level Low				10% of VCC	V
	Startup time	Test load used: 20 pF		2.5		s
		Test load used: 30 pF		3.7	13	s



Note: Peak-to-peak jitter measurements are defined by $T_{peak\text{-}to\text{-}peak} = T_{period\_max} - T_{period\_min}$.

***Figure 2-28* • Peak-to-Peak Jitter Definition**

***Table 2-92* • JTAG 1532**
Worst Commercial-Case Conditions: T_J = 85°C, Worst-Case VCC = 1.425 V

Parameter	Description	–1	Std.	Units
t_{RSTB2Q}	Reset to Q (data out)	26.67	30.67	ns
F_{TCKMAX}	TCK Maximum Frequency	19.00	21.85	MHz
$t_{TRSTREM}$	ResetB Removal Time	0.00	0.00	ns
$t_{TRSTREC}$	ResetB Recovery Time	0.27	0.31	ns
$t_{TRSTMPW}$	ResetB Minimum Pulse	TBD	TBD	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.

Analog-to-Digital Converter (ADC)

Unless otherwise noted, ADC direct input performance is specified at 25°C with nominal power supply voltages, with the output measured using the external voltage reference with the internal ADC in 12-bit mode and 500 KHz sampling frequency, after trimming and digital compensation.

Table 2-95 **• ADC Specifications**

Specification	Test Conditions	Min.	Typ.	Max.	Units
Input voltage range (for driving ADC over its full range)			2.56		V
Gain error			±0.4	±0.7	%
	–40ºC to +100ºC		±0.4	±0.7	%
Input referred offset voltage			±1	±2	mV
	–40ºC to +100ºC		±1	±2	
Integral non-linearity (INL)	RMS deviation from BFSL				
	12-bit mode		1.71		LSB
	10-bit mode		0.60	1.00	LSB
	8-bit mode		0.2	0.33	LSB
Differential non-linearity (DNL)	12-bit mode		2.4		LSB
	10-bit mode		0.80	0.94	LSB
	8-bit mode		0.2	0.23	LSB
Signal to noise ratio		62	64		dB
Effective number of bits (ENOB) $\text{ENOB} = \frac{\text{SINAD} - 1.76\text{ dB}}{6.02\text{ dB/bit}}$ *EQ 10*	–1 dBFS input				
	12-bit mode 10 KHz	9.9	10		Bits
	12-bit mode 100 KHz	9.9	10		Bits
	10-bit mode 10 KHz	9.5	9.6		Bits
	10-bit mode 100 KHz	9.5	9.6		Bits
	8-bit mode 10 KHz	7.8	7.9		Bits
	8-bit mode 100 KHz	7.8	7.9		Bits
Full power bandwidth	At –3 dB; –1 dBFS input	300			KHz
Analog settling time	To 0.1% of final value (with 1 Kohm source impedance and with ADC load)		2		µs
Input capacitance	Switched capacitance (ADC sample capacitor)		12	15	pF
	Cs: Static capacitance (Figure 2-44 on page 2-86)				
	CM[n] input		5	7	pF
	TM[n] input		5	7	pF
	ADC[n] input		5	7	pF
Input resistance	Rin: Series resistance (Figure 2-44)		2		KΩ
	Rsh: Shunt resistance, exclusive of switched capacitance effects (Figure 2-44)	10			MΩ

Note: All 3.3 V supplies are tied together and varied from 3.0 V to 3.6 V. 1.5 V supplies are held constant.

Serial Peripheral Interface (SPI) Characteristics

This section describes the DC and switching of the SPI interface. Unless otherwise noted, all output characteristics given for a 35 pF load on the pins and all sequential timing characteristics are related to SPI_x_CLK. For timing parameter definitions, refer to Figure 2-47 on page 2-90.

***Table 2-100* • SPI Characteristics**
Commercial Case Conditions: T_J = 85ºC, VDD = 1.425 V, –1 Speed Grade

Symbol	Description and Condition	A2F060	A2F200	A2F500	Unit
sp1	SPI_x_CLK minimum period				
	SPI_x_CLK = PCLK/2	20	NA	20	ns
	SPI_x_CLK = PCLK/4	40	40	40	ns
	SPI_x_CLK = PCLK/8	80	80	80	ns
	SPI_x_CLK = PCLK/16	0.16	0.16	0.16	µs
	SPI_x_CLK = PCLK/32	0.32	0.32	0.32	µs
	SPI_x_CLK = PCLK/64	0.64	0.64	0.64	µs
	SPI_x_CLK = PCLK/128	1.28	1.28	1.28	µs
	SPI_x_CLK = PCLK/256	2.56	2.56	2.56	µs
sp2	SPI_x_CLK minimum pulse width high				
	SPI_x_CLK = PCLK/2	10	NA	10	ns
	SPI_x_CLK = PCLK/4	20	20	20	ns
	SPI_x_CLK = PCLK/8	40	40	40	ns
	SPI_x_CLK = PCLK/16	0.08	0.08	0.08	µs
	SPI_x_CLK = PCLK/32	0.16	0.16	0.16	µs
	SPI_x_CLK = PCLK/64	0.32	0.32	0.32	µs
	SPI_x_CLK = PCLK/128	0.64	0.64	0.64	µs
	SPI_x_CLK = PCLK/256	1.28	1.28	1.28	us
sp3	SPI_x_CLK minimum pulse width low				
	SPI_x_CLK = PCLK/2	10	NA	10	ns
	SPI_x_CLK = PCLK/4	20	20	20	ns
	SPI_x_CLK = PCLK/8	40	40	40	ns
	SPI_x_CLK = PCLK/16	0.08	0.08	0.08	µs
	SPI_x_CLK = PCLK/32	0.16	0.16	0.16	µs
	SPI_x_CLK = PCLK/64	0.32	0.32	0.32	µs
	SPI_x_CLK = PCLK/128	0.64	0.64	0.64	µs
	SPI_x_CLK = PCLK/256	1.28	1.28	1.28	µs
sp4	SPI_x_CLK, SPI_x_DO, SPI_x_SS rise time (10%-90%) [1]	4.7	4.7	4.7	ns
sp5	SPI_x_CLK, SPI_x_DO, SPI_x_SS fall time (10%-90%) [1]	3.4	3.4	3.4	ns

Notes:

1. *These values are provided for a load of 35 pF. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website: http://www.microsemi.com/index.php?option=com_microsemi&Itemid=489&lang=en&view=salescontact.*
2. *For allowable pclk configurations, refer to the Serial Peripheral Interface Controller section in the SmartFusion Microcontroller Subsystem User's Guide.*

3 – SmartFusion Development Tools

Designing with SmartFusion cSoCs involves three different types of design: FPGA design, embedded design and analog design. These roles can be filled by three different designers, two designers or even a single designer, depending on company structure and project complexity.

Types of Design Tools

Microsemi has developed design tools and flows to meet the needs of these three types of designers so they can work together smoothly on a single project (Figure 3-1).

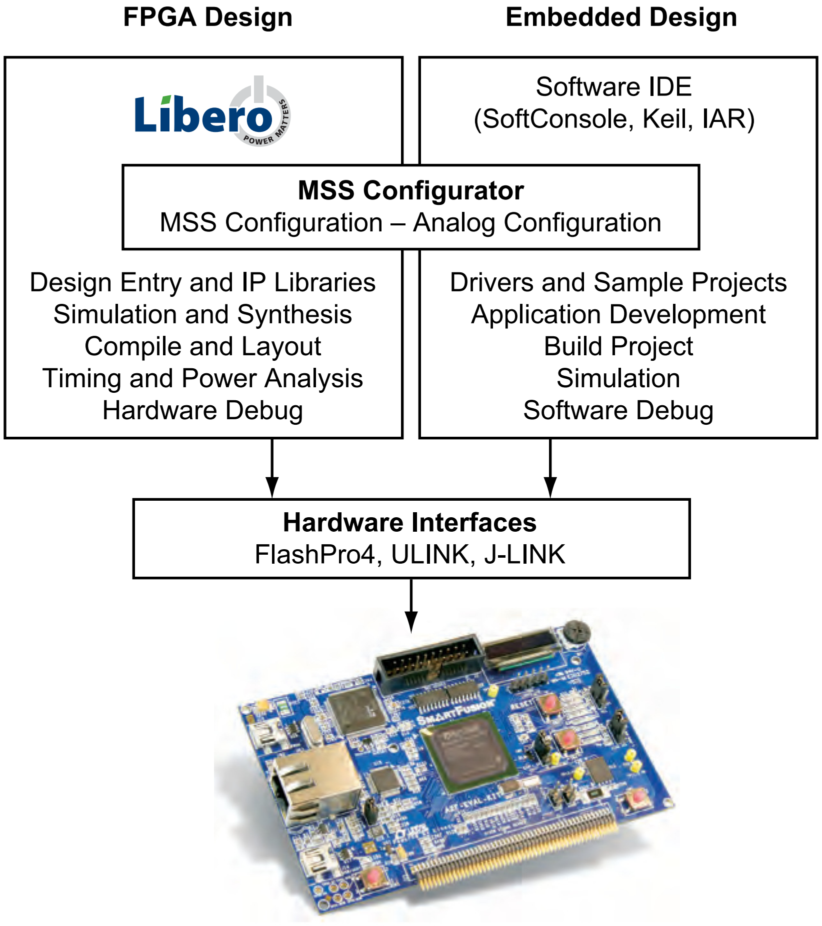


Figure 3-1 • **Three Design Roles**

FPGA Design

Libero System-on-Chip (SoC) software is Microsemi's comprehensive software toolset for designing with all Microsemi FPGAs and cSoCs. Libero SoC includes industry-leading synthesis, simulation and debug tools from Synopsys® and Mentor Graphics®, as well as innovative timing and power optimization and analysis.

User-Defined Supply Pins

Name	**Type**	**Polarity/ Bus Size**	**Description**
VAREF0	Input	1	Analog reference voltage for first ADC. The SmartFusion cSoC can be configured to generate a 2.56 V internal reference that can be used by the ADC. While using the internal reference, the reference voltage is output on the VAREFOUT pin for use as a system reference. If a different reference voltage is required, it can be supplied by an external source and applied to this pin. The valid range of values that can be supplied to the ADC is 1.0 V to 3.3 V. When VAREF0 is internally generated, a bypass capacitor must be connected from this pin to ground. The value of the bypass capacitor should be between 3.3 µF and 22 µF, which is based on the needs of the individual designs. The choice of the capacitor value has an impact on the settling time it takes the VAREF0 signal to reach the required specification of 2.56 V to initiate valid conversions by the ADC. If the lower capacitor value is chosen, the settling time required for VAREF0 to achieve 2.56 V will be shorter than when selecting the larger capacitor value. The above range of capacitor values supports the accuracy specification of the ADC, which is detailed in the datasheet. Designers choosing the smaller capacitor value will not obtain as much margin in the accuracy as that achieved with a larger capacitor value. See the Analog-to-Digital Converter (ADC) section in the *SmartFusion Programmable Analog User's Guide* for more information. The SoC Products Group recommends customers use 10 µF as the value of the bypass capacitor. Designers choosing to use an external VAREF0 need to ensure that a stable and clean VAREF0 source is supplied to the VAREF0 pin before initiating conversions by the ADC. To use the internal voltage reference, the VAREFOUT pin must be connected to the appropriate ADC VAREFx input on the PCB. For example, VAREFOUT can be connected to VAREF0 only, if ADC0 alone is used. VAREFOUT can be connected to VAREF1 only, if ADC1 alone is used. VAREFOUT can be connected to VAREF2 only, if ADC2 alone is used. VAREFOUT can be connected to VAREF0, VAREF1 and VAREF2 together, if ADC0, ADC1, and ADC2 all are used.
VAREF1	Input	1	Analog reference voltage for second ADC See "VAREF0" above for more information.
VAREF2	Input	1	Analog reference voltage for third ADC See "VAREF0" above for more.
VAREFOUT	Out	1	Internal 2.56 V voltage reference output. Can be used to provide the two ADCs with a unique voltage reference externally by connecting VAREFOUT to both VAREF0 and VAREF1. To use the internal voltage reference, you must connect the VAREFOUT pin to the appropriate ADC VAREFx input—either the VAREF0 or VAREF1 pin—on the PCB.

User I/O Naming Conventions

The naming convention used for each FPGA user I/O is Gmn/IOuxwByVz, where:

Gmn is only used for I/Os that also have CCC access—i.e., global pins. Refer to the "Global I/O Naming Conventions" section on page 5-6.

u = I/O pair number in bank, starting at 00 from the northwest I/O bank and proceeding in a clockwise direction.

x = P (positive) or N (negative) or S (single-ended) or R (regular, single-ended).

w = D (Differential Pair), P (Pair), or S (Single-Ended). D (Differential Pair) if both members of the pair are bonded out to adjacent pins or are separated only by one GND or NC pin; P (Pair) if both members of the pair are bonded out but do not meet the adjacency requirement; or S (Single-Ended) if the I/O pair is not bonded out. For Differential Pairs (D), adjacency for ball grid packages means only vertical or horizontal. Diagonal adjacency does not meet the requirements for a true differential pair.

B = Bank

y = Bank number starting at 0 from northwest I/O bank and incrementing clockwise.

V = Reference voltage

z = VREF mini bank number.

The FPGA user I/O pin functions as an input, output, tristate or bidirectional buffer. Input and output signal levels are compatible with the I/O standard selected. Unused I/O pins are disabled by Libero SoC software and include a weak pull-up resistor. During power-up, the used I/O pins are tristated with no pull-up or pull-down resistors until I/O enable (there is a delay after voltage stabilizes, and different I/O banks power up sequentially to avoid a surge of ICCI).

Unused I/Os are configured as follows:

- Output buffer is disabled (with tristate value of high impedance)
- Input buffer is disabled (with tristate value of high impedance)
- Weak pull-up is programmed

Some of these pins are also multiplexed with integrated peripherals in the MSS (Ethernet MAC and external memory controller).

All unused MSS I/Os are tristated by default (with output buffer disabled). However, you can configure it as weak pull-up or pull-down by using Libero SoC I/O attributor window. The Schmitt trigger is disabled. Essentially, I/Os have the reset values as defined in Table 19-25 IOMUX_n_CR, in the *SmartFusion Microcontroller Subsystem User's Guide*.

By default, during programming I/Os become tristated and weakly pulled up to VCCxxxxIOBx. You can modify the I/O states during programming in FlashPro. For more details, refer to "Specifying I/O States During Programming" on page 1-3. With the VCCI and VCC supplies continuously powered up, when the device transitions from programming to operating mode, the I/Os are instantly configured to the desired user configuration. For more information, see the SmartFusion FPGA User I/Os section in the *SmartFusion FPGA Fabric User's Guide*.

Special Function Pins

Name	Type	Polarity/Bus Size	Description
NC			No connect This pin is not connected to circuitry within the device. These pins can be driven to any voltage or can be left floating with no effect on the operation of the device.
DC			Do not connect. This pin should not be connected to any signals on the PCB. These pins should be left unconnected.
LPXIN	In	1	Low power 32 KHz crystal oscillator. Input from the 32 KHz oscillator. Pin for connecting a low power 32 KHz watch crystal. If not used, the LPXIN pin can be left floating. For more information, see the PLLs, Clock Conditioning Circuitry, and On-Chip Crystal Oscillators section in the *SmartFusion Microcontroller Subsystem User's Guide*.
LPXOUT	In	1	Low power 32 KHz crystal oscillator. Output to the 32 KHz oscillator. Pin for connecting a low power 32 KHz watch crystal. If not used, the LPXOUT pin can be left floating. For more information, see the PLLs, Clock Conditioning Circuitry, and On-Chip Crystal Oscillators section in the *SmartFusion Microcontroller Subsystem User's Guide*.
MAINXIN	In	1	Main crystal oscillator circuit. Input to the crystal oscillator circuit. Pin for connecting an external crystal, ceramic resonator, or RC network. When using an external crystal or ceramic oscillator, external capacitors are also recommended. Refer to documentation from the crystal oscillator manufacturer for proper capacitor value. If an external RC network or clock input is used, the RC components are connected to the MAINXIN pin, with MAINXOUT left floating. When the main crystal oscillator is not being used, MAINXIN and MAINXOUT pins can be left floating. For more information, see the PLLs, Clock Conditioning Circuitry, and On-Chip Crystal Oscillators section in the *SmartFusion Microcontroller Subsystem User's Guide*.
MAINXOUT	Out	1	Main crystal oscillator circuit. Output from the crystal oscillator circuit. Pin for connecting external crystal or ceramic resonator. When using an external crystal or ceramic oscillator, external capacitors are also recommended. Refer to documentation from the crystal oscillator manufacturer for proper capacitor value. If an external RC network or clock input is used, the RC components are connected to the MAINXIN pin, with MAINXOUT left floating. When the main crystal oscillator is not being used, MAINXIN and MAINXOUT pins can be left floating. For more information, see the PLLs, Clock Conditioning Circuitry, and On-Chip Crystal Oscillators section in the *SmartFusion Microcontroller Subsystem User's Guide*.

Table 5-1 • **Recommended Tie-Off Values for the TCK and TRST Pins**

VJTAG	Tie-Off Resistance[1, 2]
VJTAG at 3.3 V	200 Ω to 1 kΩ
VJTAG at 2.5 V	200 Ω to 1 kΩ
VJTAG at 1.8 V	500 Ω to 1 kΩ
VJTAG at 1.5 V	500 Ω to 1 kΩ

Notes:

1. *The TCK pin can be pulled up/down.*
2. *The TRST pin can only be pulled down.*
1. *Equivalent parallel resistance if more than one device is on JTAG chain.*

Pin No.	CS288		
	A2F060 Function	**A2F200 Function**	**A2F500 Function**
K17	GNDLPXTAL	GNDLPXTAL	GNDLPXTAL
K19	GNDMAINXTAL	GNDMAINXTAL	GNDMAINXTAL
K21	MAINXIN	MAINXIN	MAINXIN
L1	GNDRCOSC	GNDRCOSC	GNDRCOSC
L3	VCCFPGAIOB5	VCCFPGAIOB5	VCCFPGAIOB5
L5	EMC_DB[2]/IO37NPB5V0	EMC_DB[2]/IO60NPB5V0	EMC_DB[2]/IO77NPB5V0
L6	NC	GNDQ	GNDQ
L8	VCC	VCC	VCC
L9	GND	GND	GND
L10	VCC	VCC	VCC
L12	VCC	VCC	VCC
L13	GND	GND	GND
L14	VCC	VCC	VCC
L16	VCCLPXTAL	VCCLPXTAL	VCCLPXTAL
L17	VDDBAT	VDDBAT	VDDBAT
L19	LPXIN	LPXIN	LPXIN
L21	MAINXOUT	MAINXOUT	MAINXOUT
M1	VCCRCOSC	VCCRCOSC	VCCRCOSC
M3	MSS_RESET_N	MSS_RESET_N	MSS_RESET_N
M5	GPIO_5/IO28RSB4V0	GPIO_5/IO42RSB4V0	GPIO_5/IO51RSB4V0
M6	GND	GND	GND
M8	GND	GND	GND
M9	VCC	VCC	VCC
M10	GND	GND	GND
M11	VCC	VCC	VCC
M12	GND	GND	GND
M13	VCC	VCC	VCC
M14	GND	GND	GND
M16	TMS	TMS	TMS
M17	VJTAG	VJTAG	VJTAG
M19	TDO	TDO	TDO

Notes:

1. *Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.*
2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*

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Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx.

Pin No.	FG256		
	A2F060 Function	**A2F200 Function**	**A2F500 Function**
A1	GND	GND	GND
A2	VCCFPGAIOB0	VCCFPGAIOB0	VCCFPGAIOB0
A3	EMC_AB[0]/IO04NDB0V0	EMC_AB[0]/IO04NDB0V0	EMC_AB[0]/IO06NDB0V0
A4	EMC_AB[1]/IO04PDB0V0	EMC_AB[1]/IO04PDB0V0	EMC_AB[1]/IO06PDB0V0
A5	GND	GND	GND
A6	EMC_AB[3]/IO05PDB0V0	EMC_AB[3]/IO05PDB0V0	EMC_AB[3]/IO09PDB0V0
A7	EMC_AB[5]/IO06PDB0V0	EMC_AB[5]/IO06PDB0V0	EMC_AB[5]/IO10PDB0V0
A8	VCCFPGAIOB0	VCCFPGAIOB0	VCCFPGAIOB0
A9	GND	GND	GND
A10	EMC_AB[14]/IO11NDB0V0	EMC_AB[14]/IO11NDB0V0	EMC_AB[14]/IO15NDB0V0
A11	EMC_AB[15]/IO11PDB0V0	EMC_AB[15]/IO11PDB0V0	EMC_AB[15]/IO15PDB0V0
A12	GND	GND	GND
A13	EMC_AB[20]/IO14NDB0V0	EMC_AB[20]/IO14NDB0V0	EMC_AB[20]/IO21NDB0V0
A14	EMC_AB[24]/IO16NDB0V0	EMC_AB[24]/IO16NDB0V0	EMC_AB[24]/IO20NDB0V0
A15	VCCFPGAIOB0	VCCFPGAIOB0	VCCFPGAIOB0
A16	GND	GND	GND
B1	EMC_DB[15]/IO45PDB5V0	EMC_DB[15]/GAA2/IO71PDB5V0	EMC_DB[15]/GAA2/IO88PDB5V0
B2	GND	GND	GND
B3	EMC_BYTEN[1]/IO02PDB0V0	EMC_BYTEN[1]/GAC1/IO02PDB0V0	EMC_BYTEN[1]/GAC1/IO07PDB0V0
B4	EMC_OEN0_N/IO03NDB0V0	EMC_OEN0_N/IO03NDB0V0	EMC_OEN0_N/IO08NDB0V0
B5	EMC_OEN1_N/IO03PDB0V0	EMC_OEN1_N/IO03PDB0V0	EMC_OEN1_N/IO08PDB0V0
B6	EMC_AB[2]/IO05NDB0V0	EMC_AB[2]/IO05NDB0V0	EMC_AB[2]/IO09NDB0V0
B7	EMC_AB[4]/IO06NDB0V0	EMC_AB[4]/IO06NDB0V0	EMC_AB[4]/IO10NDB0V0
B8	EMC_AB[9]/IO08PDB0V0	EMC_AB[9]/IO08PDB0V0	EMC_AB[9]/IO13PDB0V0
B9	EMC_AB[12]/IO10NDB0V0	EMC_AB[12]/IO10NDB0V0	EMC_AB[12]/IO14NDB0V0
B10	EMC_AB[13]/IO10PDB0V0	EMC_AB[13]/IO10PDB0V0	EMC_AB[13]/IO14PDB0V0
B11	EMC_AB[16]/IO12NDB0V0	EMC_AB[16]/IO12NDB0V0	EMC_AB[16]/IO17NDB0V0
B12	EMC_AB[18]/IO13NDB0V0	EMC_AB[18]/IO13NDB0V0	EMC_AB[18]/IO18NDB0V0
B13	EMC_AB[21]/IO14PDB0V0	EMC_AB[21]/IO14PDB0V0	EMC_AB[21]/IO21PDB0V0
B14	EMC_AB[25]/IO16PDB0V0	EMC_AB[25]/IO16PDB0V0	EMC_AB[25]/IO20PDB0V0
B15	GND	GND	GND

Notes:

1. *Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.*
2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*

Pin Number	FG484	
	A2F200 Function	A2F500 Function
AA13	NC	ADC10
AA14	NC	ADC9
AA15	NC	GND15ADC2
AA16	MAINXIN	MAINXIN
AA17	MAINXOUT	MAINXOUT
AA18	LPXIN	LPXIN
AA19	LPXOUT	LPXOUT
AA20	NC	NC
AA21	NC	NC
AA22	SPI_1_CLK/GPIO_26	SPI_1_CLK/GPIO_26
AB1	GND	GND
AB2	GPIO_13/IO36RSB4V0	GPIO_13/IO45RSB4V0
AB3	GPIO_14/IO35RSB4V0	GPIO_14/IO44RSB4V0
AB4	GND	GND
AB5	PCAP	PCAP
AB6	NCAP	NCAP
AB7	ABPS3	ABPS3
AB8	ADC3	ADC3
AB9	GND15ADC0	GND15ADC0
AB10	VCC33ADC1	VCC33ADC1
AB11	VAREF1	VAREF1
AB12	TM2	TM2
AB13	CM2	CM2
AB14	ABPS4	ABPS4
AB15	GNDAQ	GNDAQ
AB16	GNDMAINXTAL	GNDMAINXTAL
AB17	GNDLPXTAL	GNDLPXTAL
AB18	VCCLPXTAL	VCCLPXTAL
AB19	VDDBAT	VDDBAT
AB20	PTBASE	PTBASE
AB21	NC	NC
AB22	GND	GND
B1	EMC_DB[15]/GAA2/IO71PDB5V0	EMC_DB[15]/GAA2/IO88PDB5V0
B2	GND	GND

Notes:

1. *Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.*
2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*

Pin Number	FG484	
	A2F200 Function	**A2F500 Function**
T1	GND	GND
T2	VCCMSSIOB4	VCCMSSIOB4
T3	GPIO_8/IO39RSB4V0	GPIO_8/IO48RSB4V0
T4	GPIO_11/IO57RSB4V0	GPIO_11/IO66RSB4V0
T5	GND	GND
T6	MAC_CLK	MAC_CLK
T7	VCCMSSIOB4	VCCMSSIOB4
T8	VCC33SDD0	VCC33SDD0
T9	VCC15A	VCC15A
T10	GNDAQ	GNDAQ
T11	GND33ADC0	GND33ADC0
T12	ADC7	ADC7
T13	NC	TM4
T14	NC	VAREF2
T15	VAREFOUT	VAREFOUT
T16	VCCMSSIOB2	VCCMSSIOB2
T17	SPI_1_DO/GPIO_24	SPI_1_DO/GPIO_24
T18	GND	GND
T19	NC	NC
T20	NC	NC
T21	VCCMSSIOB2	VCCMSSIOB2
T22	GND	GND
U1	GND	GND
U2	GPIO_5/IO42RSB4V0	GPIO_5/IO51RSB4V0
U3	GPIO_10/IO58RSB4V0	GPIO_10/IO67RSB4V0
U4	VCCMSSIOB4	VCCMSSIOB4
U5	MAC_RXD[1]/IO53RSB4V0	MAC_RXD[1]/IO62RSB4V0
U6	NC	NC
U7	VCC33AP	VCC33AP
U8	VCC33N	VCC33N
U9	CM1	CM1
U10	VAREF0	VAREF0
U11	GND33ADC1	GND33ADC1
U12	ADC4	ADC4

Notes:

1. *Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.*
2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*

Revision	Changes	Page
Revision 10 (January 2013)	The "SmartFusion cSoC Family Product Table" section has been updated to specify that External Memory Controller support for A2F060-TQ144 is not available (SAR 41555).	II
	The following Note was added to the "Package I/Os: MSS + FPGA I/Os" table (SAR 41027): "There are no LVTTL capable direct inputs available on A2F060 devices."	III
	The "Product Ordering Codes" section has been updated to mention "Y" as "Blank" mentioning "Device Does Not Include License to Implement IP Based on the Cryptography Research, Inc. (CRI) Patent Portfolio" (SAR 43218).	VI
	Added a note to Table 2-3 • Recommended Operating Conditions[5,6] (SAR 43428): The programming temperature range supported is $T_{ambient}$ = 0°C to 85°C.	2-3
	Statements about the state of the I/Os during programming were updated in the following sections: "I/O Power-Up and Supply Voltage Thresholds for Power-On Reset (Commercial and Industrial)" and "User I/O Naming Conventions" (SAR 43380).	2-4, 5-7
	In Table 2-4 • FPGA and Embedded Flash Programming, Storage and Operating Limits, the upper value of temperature ranges was corrected from "Min." to "Max." (SAR 41826).	2-4
	Information for A2F200M3F-CS288 was added to Table 2-6 • Package Thermal Resistance. The die size column was removed (SARs 41828, 42168). Also added details for A2F200M3F-PQG208I (SAR 35728).	2-7
	Added the following note to Table 2-65 • LVDS and Table 2-68 • LVPECL: "The above mentioned timing parameters correspond to 24mA drive strength." (SAR 43457)	2-41, 2-43
	The note in Table 2-86 • SmartFusion CCC/PLL Specification referring the reader to SmartGen was revised to refer instead to the online help associated with the core (SAR 34816).	2-63
	The SRAM collision data in Table 2-87 • RAM4K9 and Table 2-88 • RAM512X18 was updated (SAR 38583).	2-69,2-70
	The maximum input bias current for comparators 1, 3, 5, 7, and 9, in Table 2-97 • Comparator Performance Specifications, was revised from 60 to 100 nA (SAR 36008).	2-84

Revision	Changes	Page
	The A2F060 device was added to product information tables.	N/A
	The "Product Ordering Codes" table was updated to removed Std. speed and add speed grade 1. Pre-production was removed from the application ordering code category.	VI
	The "SmartFusion cSoC Block Diagram" was revised.	IV
	The "Datasheet Categories" section was updated, referencing the "SmartFusion cSoC Block Diagram" table, which is new.	1-4, IV
	The "VCCI" parameter was renamed to "VCCxxxxIOBx." "Advanced I/Os" were renamed to "FPGA I/Os." Generic pin names that represent multiple pins were standardized with a lower case x as a placeholder. For example, VAREFx designates VAREF0, VAREF1, and VAREF2. Modes were renamed as follows: Operating mode was renamed to SoC mode. 32KHz Active mode was renamed to Standby mode. Battery mode was renamed to Time Keeping mode. Table entries have been filled with values as data has become available.	N/A
	Table 2-1 • Absolute Maximum Ratings, Table 2-2 • Analog Maximum Ratings, and Table 2-3 • Recommended Operating Conditions[5,6] were revised extensively.	2-1 through 2-3
	Device names were updated in Table 2-6 • Package Thermal Resistance.	2-7
	Table 2-8 • Power Supplies Configuration was revised extensively.	2-10
	Table 2-11 • Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings was revised extensively.	2-11
	Removed "Example of Power Calculation."	N/A
	Table 2-14 • Different Components Contributing to Dynamic Power Consumption in SmartFusion cSoCs was revised extensively.	2-12
	Table 2-15 • Different Components Contributing to the Static Power Consumption in SmartFusion cSoCs was revised extensively.	2-13
	The "Power Calculation Methodology" section was revised.	2-14
	Table 2-83 • Electrical Characteristics of the RC Oscillator was revised extensively.	2-61
	Table 2-85 • Electrical Characteristics of the Low Power Oscillator was revised extensively.	2-62
	The parameter t_{RSTBQ} was changed to T_{C2CWRH} in Table 2-87 • RAM4K9.	2-69
	The 12-bit mode row for integral non-linearity was removed from Table 2-95 • ADC Specifications. The typical value for 10-bit mode was revised. The table note was punctuated correctly to make it clear.	2-81
	Figure 37-34 • Write Access after Write onto Same Address, Figure 37-34 • Read Access after Write onto Same Address, and Figure 37-34 • Write Access after Read onto Same Address were deleted.	N/A
	Table 2-99 • Voltage Regulator was revised extensively.	2-87
	The "Serial Peripheral Interface (SPI) Characteristics" section and "Inter-Integrated Circuit (I^2C) Characteristics" section are new.	2-89, 2-91