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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details

Product Status	Obsolete
Architecture	MCU, FPGA
Core Processor	ARM® Cortex®-M3
Flash Size	128KB
RAM Size	16KB
Peripherals	DMA, POR, WDT
Connectivity	EBI/EMI, I ² C, SPI, UART/USART
Speed	100MHz
Primary Attributes	ProASIC®3 FPGA, 60K Gates, 1536D-Flip-Flops
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/a2f060m3e-1fg256i

Datasheet Categories	6-14
Microsemi SoC Products Group Safety Critical, Life Support, and High-Reliability Applications Policy	6-14

Table 2-3 • Recommended Operating Conditions^{5,6}

Symbol	Parameter ¹		Commercial	Industrial	Units
T _J	Junction temperature		0 to +85	−40 to +100	°C
VCC ²	1.5 V DC core supply voltage		1.425 to 1.575	1.425 to 1.575	V
VJTAG	JTAG DC voltage		1.425 to 3.6	1.425 to 3.6	V
VPP	Programming voltage	Programming mode ³	3.15 to 3.45	3.15 to 3.45	V
		Operation ⁴	0 to 3.6	0 to 3.6	V
VCCPLLx	Analog power supply (PLL)		1.425 to 1.575	1.425 to 1.575	V
VCCFPGAIOBx/ VCCMSSIOBx ⁵	1.5 V DC supply voltage		1.425 to 1.575	1.425 to 1.575	V
	1.8 V DC supply voltage		1.7 to 1.9	1.7 to 1.9	V
	2.5 V DC supply voltage		2.3 to 2.7	2.3 to 2.7	V
	3.3 V DC supply voltage		3.0 to 3.6	3.0 to 3.6	V
	LVDS differential I/O		2.375 to 2.625	2.375 to 2.625	V
	LVPECL differential I/O		3.0 to 3.6	3.0 to 3.6	V
VCC33A ⁶	Analog clean 3.3 V supply to the analog circuitry		3.15 to 3.45	3.15 to 3.45	V
VCC33ADCx ⁶	Analog 3.3 V supply to ADC		3.15 to 3.45	3.15 to 3.45	V
VCC33AP ⁶	Analog clean 3.3 V supply to the charge pump		3.15 to 3.45	3.15 to 3.45	V
VCC33SDDx ⁶	Analog 3.3 V supply to sigma-delta DAC		3.15 to 3.45	3.15 to 3.45	V
VAREFx	Voltage reference for ADC		2.527 to 3.3	2.527 to 3.3	V
VCCRCOSC	Analog supply to the integrated RC oscillator		3.15 to 3.45	3.15 to 3.45	V
VDDBAT	External battery supply		2.7 to 3.63	2.7 to 3.63	V
VCCMAINXTAL ⁶	Analog supply to the main crystal oscillator		3.15 to 3.45	3.15 to 3.45	V
VCCLPXTAL ⁶	Analog supply to the low power 32 KHz crystal oscillator		3.15 to 3.45	3.15 to 3.45	V
VCCENVM	Embedded nonvolatile memory supply		1.425 to 1.575	1.425 to 1.575	V
VCCESRAM	Embedded SRAM supply		1.425 to 1.575	1.425 to 1.575	V
VCC15A ²	Analog 1.5 V supply to the analog circuitry		1.425 to 1.575	1.425 to 1.575	V
VCC15ADCx ²	Analog 1.5 V supply to the ADC		1.425 to 1.575	1.425 to 1.575	V

Notes:

1. All parameters representing voltages are measured with respect to GND unless otherwise specified.
2. The following 1.5 V supplies should be connected together while following proper noise filtering practices: VCC, VCC15A, and VCC15ADCx.
3. The Programming temperature range supported is T_{ambient} = 0°C to 85°C.
4. VPP can be left floating during operation (not programming mode).
5. The ranges given here are for power supplies only. The recommended input voltage ranges specific to each I/O standard are given in [Table 2-19 on page 2-23](#). VCCxxxIOBx should be at the same voltage within a given I/O bank.
6. The following 3.3 V supplies should be connected together while following proper noise filtering practices: VCC33A, VCC33ADCx, VCC33AP, VCC33SDDx, VCCMAINXTAL, and VCCLPXTAL.

Table 2-30 • I/O Short Currents I_{OSH}/I_{OSL}
 Applicable to FPGA I/O Banks

	Drive Strength	I_{OSL} (mA)*	I_{OSH} (mA)*
3.3 V LVTTTL / 3.3 V LVCMOS	2 mA	27	25
	4 mA	27	25
	6 mA	54	51
	8 mA	54	51
	12 mA	109	103
	16 mA	127	132
	24 mA	181	268
2.5 V LVCMOS	2 mA	18	16
	4 mA	18	16
	6 mA	37	32
	8 mA	37	32
	12 mA	74	65
	16 mA	87	83
	24 mA	124	169
1.8 V LVCMOS	2 mA	11	9
	4 mA	22	17
	6 mA	44	35
	8 mA	51	45
	12 mA	74	91
	16 mA	74	91
1.5 V LVCMOS	2 mA	16	13
	4 mA	33	25
	6 mA	39	32
	8 mA	55	66
	12 mA	55	66
3.3 V PCI/PCI-X	Per PCI/PCI-X specification	109	103

Note: * $T_J = 85^{\circ}\text{C}$.

Table 2-31 • I/O Short Currents I_{OSH}/I_{OSL}
 Applicable to MSS I/O Banks

	Drive Strength	I_{OSL} (mA)*	I_{OSH} (mA)*
3.3 V LVTTTL / 3.3 V LVCMOS	8 mA	54	51
2.5 V LVCMOS	8 mA	37	32
1.8 V LVCMOS	4 mA	22	17
1.5 V LVCMOS	2 mA	16	13

Note: * $T_J = 85^{\circ}\text{C}$

Timing Characteristics

Table 2-44 • 2.5 V LVCMOS High Slew

Worst Commercial-Case Conditions: $T_J = 85^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$,

Worst-Case $V_{CC} \times I_{O/B} = 2.3\text{ V}$

Applicable to FPGA I/O Banks, I/O Assigned to EMC I/O Pins

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.55	8.10	0.04	1.23	0.39	7.37	8.10	2.54	2.17	9.43	10.15	ns
	–1	0.46	6.75	0.03	1.03	0.32	6.14	6.75	2.12	1.81	7.85	8.46	ns
8 mA	Std.	0.55	4.85	0.04	1.23	0.39	4.76	4.85	2.90	2.83	6.82	6.91	ns
	–1	0.46	4.04	0.03	1.03	0.32	3.97	4.04	2.42	2.36	5.68	5.76	ns
12 mA	Std.	0.60	3.28	0.04	1.23	0.39	3.46	3.23	3.15	3.24	5.52	5.29	ns
	–1	0.50	2.73	0.03	1.03	0.32	2.88	2.69	2.62	2.70	4.60	4.41	ns
16 mA	Std.	0.60	3.09	0.04	1.23	0.39	3.27	2.88	3.20	3.35	5.33	4.94	ns
	–1	0.50	2.57	0.03	1.03	0.32	2.72	2.40	2.67	2.79	4.44	4.12	ns
24 mA	Std.	0.60	2.95	0.04	1.23	0.39	3.01	2.31	3.27	3.76	5.07	4.37	ns
	–1	0.50	2.46	0.03	1.03	0.32	2.51	1.93	2.73	3.13	4.22	3.64	ns

Notes:

- Software default selection highlighted in gray.
- For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-9](#) for derating values.

Table 2-45 • 2.5 V LVCMOS Low Slew

Worst Commercial-Case Conditions: $T_J = 85^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$,

Worst-Case $V_{CC} \times I_{O/B} = 2.3\text{ V}$

Applicable to FPGA I/O Banks, I/O Assigned to EMC I/O Pins

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.55	10.50	0.04	1.23	0.39	10.69	10.50	2.54	2.07	12.75	12.56	ns
	–1	0.46	8.75	0.03	1.03	0.32	8.91	8.75	2.12	1.73	10.62	10.47	ns
8 mA	Std.	0.55	7.61	0.04	1.23	0.39	7.46	7.19	2.81	2.66	9.52	9.25	ns
	–1	0.46	6.34	0.03	1.03	0.32	6.22	5.99	2.34	2.22	7.93	7.71	ns
12 mA	Std.	0.60	5.92	0.04	1.23	0.39	5.79	5.45	3.04	3.06	7.85	7.51	ns
	–1	0.50	4.93	0.03	1.03	0.32	4.83	4.54	2.53	2.55	6.54	6.26	ns
16 mA	Std.	0.60	5.53	0.04	1.23	0.39	5.40	5.09	3.09	3.16	7.46	7.14	ns
	–1	0.50	4.61	0.03	1.03	0.32	4.50	4.24	2.58	2.64	6.22	5.95	ns
24 mA	Std.	0.60	5.18	0.04	1.23	0.39	5.28	5.14	3.27	3.64	7.34	7.20	ns
	–1	0.50	4.32	0.03	1.03	0.32	4.40	4.29	2.72	3.03	6.11	6.00	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-9](#) for derating values.

Table 2-46 • 2.5 V LVCMOS High Slew

Worst Commercial-Case Conditions: $T_J = 85^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$,

Worst-Case $V_{CC} \times I_{O/B} = 3.0\text{ V}$

Applicable to MSS I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
8 mA	Std.	0.22	2.35	0.09	1.18	1.39	0.22	2.40	2.18	2.19	2.32	ns
	–1	0.18	1.96	0.07	0.99	1.16	0.18	2.00	1.82	1.82	1.93	ns

Notes:

- Software default selection highlighted in gray.
- For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-9](#) for derating values.

Differential I/O Characteristics

Physical Implementation

Configuration of the I/O modules as a differential pair is handled by SoC Products Group Designer software when the user instantiates a differential I/O macro in the design.

Differential I/Os can also be used in conjunction with the embedded Input Register (InReg), Output Register (OutReg), Enable Register (EnReg), and Double Data Rate (DDR). However, there is no support for bidirectional I/Os or tristates with the LVPECL standards.

LVDS

Low-Voltage Differential Signaling (ANSI/TIA/EIA-644) is a high-speed, differential I/O standard. It requires that one data bit be carried through two signal lines, so two pins are needed. It also requires external resistor termination.

The full implementation of the LVDS transmitter and receiver is shown in an example in [Figure 2-11](#). The building blocks of the LVDS transmitter-receiver are one transmitter macro, one receiver macro, three board resistors at the transmitter end, and one resistor at the receiver end. The values for the three driver resistors are different from those used in the LVPECL implementation because the output standard specifications are different.

Along with LVDS I/O, SmartFusion cSoCs also support bus LVDS structure and multipoint LVDS (M-LVDS) configuration (up to 40 nodes).

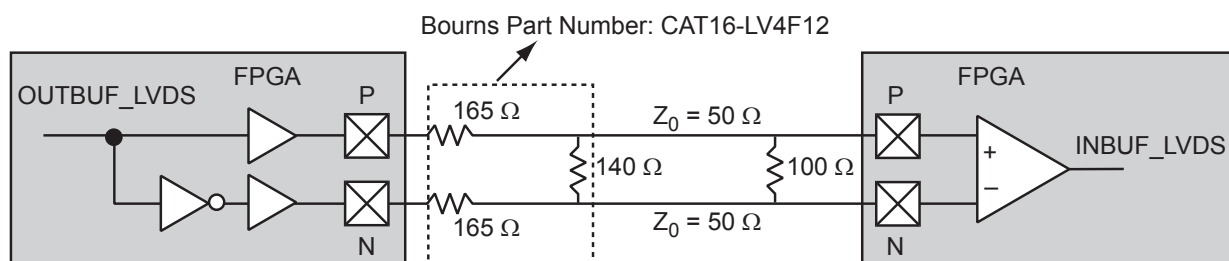


Figure 2-11 • LVDS Circuit Diagram and Board-Level Implementation

Output Enable Register

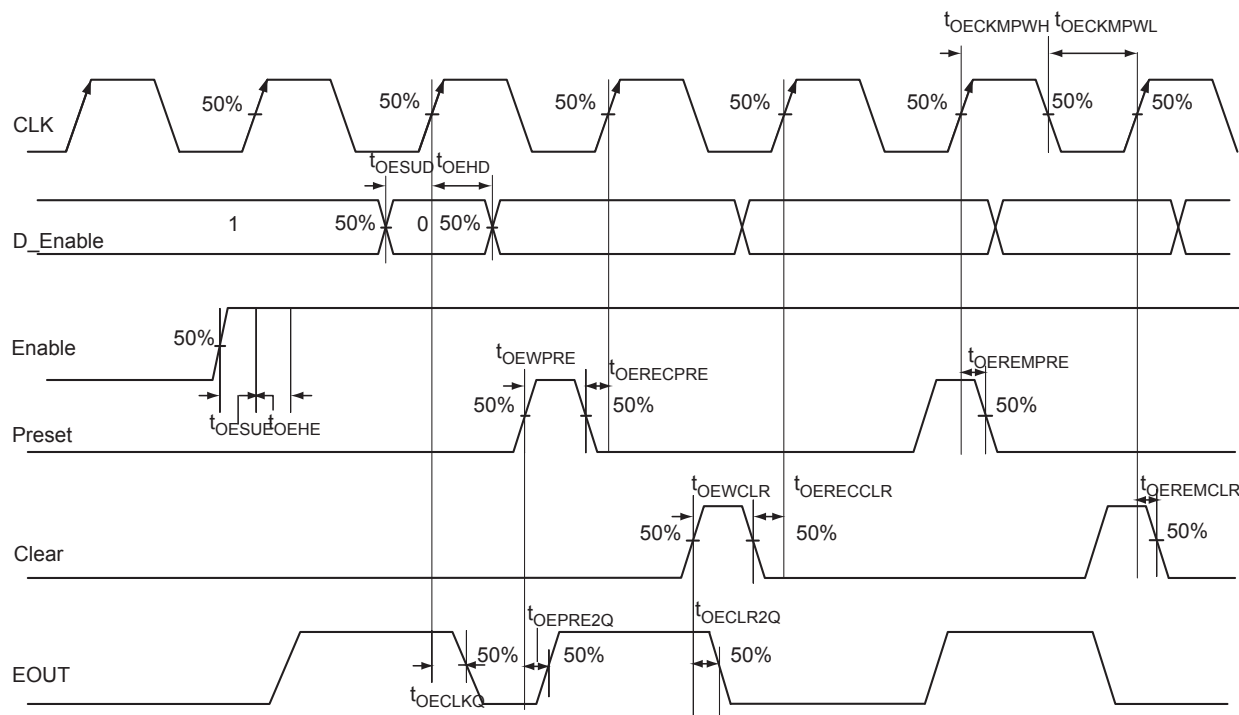


Figure 2-18 • Output Enable Register Timing Diagram

Timing Characteristics

Table 2-73 • Output Enable Register Propagation Delays

Worst Commercial-Case Conditions: $T_J = 85^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

Parameter	Description	-1	Std.	Units
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	0.45	0.54	ns
t_{OESUD}	Data Setup Time for the Output Enable Register	0.32	0.38	ns
t_{OEHD}	Data Hold Time for the Output Enable Register	0.00	0.00	ns
t_{OESUE}	Enable Setup Time for the Output Enable Register	0.44	0.53	ns
t_{OEHE}	Enable Hold Time for the Output Enable Register	0.00	0.00	ns
$t_{OECLR2Q}$	Asynchronous Clear-to-Q of the Output Enable Register	0.68	0.81	ns
$t_{OEPRE2Q}$	Asynchronous Preset-to-Q of the Output Enable Register	0.68	0.81	ns
$t_{OEREMCLR}$	Asynchronous Clear Removal Time for the Output Enable Register	0.00	0.00	ns
$t_{OERECCLR}$	Asynchronous Clear Recovery Time for the Output Enable Register	0.23	0.27	ns
$t_{OEREMPRE}$	Asynchronous Preset Removal Time for the Output Enable Register	0.00	0.00	ns
$t_{OERECPRE}$	Asynchronous Preset Recovery Time for the Output Enable Register	0.23	0.27	ns
$t_{OEWCCLR}$	Asynchronous Clear Minimum Pulse Width for the Output Enable Register	0.22	0.22	ns
$t_{OEWPRES}$	Asynchronous Preset Minimum Pulse Width for the Output Enable Register	0.22	0.22	ns
$t_{OECKMPWH}$	Clock Minimum Pulse Width High for the Output Enable Register	0.36	0.36	ns
$t_{OECKMPWL}$	Clock Minimum Pulse Width Low for the Output Enable Register	0.32	0.32	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-9](#) for derating values.

Timing Characteristics

Table 2-78 • Combinatorial Cell Propagation Delays

Worst Commercial-Case Conditions: $T_J = 85^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

Combinatorial Cell	Equation	Parameter	-1	Std.	Units
INV	$Y = !A$	t_{PD}	0.41	0.49	ns
AND2	$Y = A \cdot B$	t_{PD}	0.48	0.57	ns
NAND2	$Y = !(A \cdot B)$	t_{PD}	0.48	0.57	ns
OR2	$Y = A + B$	t_{PD}	0.49	0.59	ns
NOR2	$Y = !(A + B)$	t_{PD}	0.49	0.59	ns
XOR2	$Y = A \oplus B$	t_{PD}	0.75	0.90	ns
MAJ3	$Y = \text{MAJ}(A, B, C)$	t_{PD}	0.71	0.85	ns
XOR3	$Y = A \oplus B \oplus C$	t_{PD}	0.89	1.07	ns
MUX2	$Y = A \text{ IS } + B \text{ S}$	t_{PD}	0.51	0.62	ns
AND3	$Y = A \cdot B \cdot C$	t_{PD}	0.57	0.68	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-9](#) for derating values.

VersaTile Specifications as a Sequential Module

The SmartFusion library offers a wide variety of sequential cells, including flip-flops and latches. Each has a data input and optional enable, clear, or preset. In this section, timing characteristics are presented for a representative sample from the library. For more details, refer to the [IGLOO/e](#), [Fusion](#), [ProASIC3/E](#), and [SmartFusion Macro Library Guide](#).

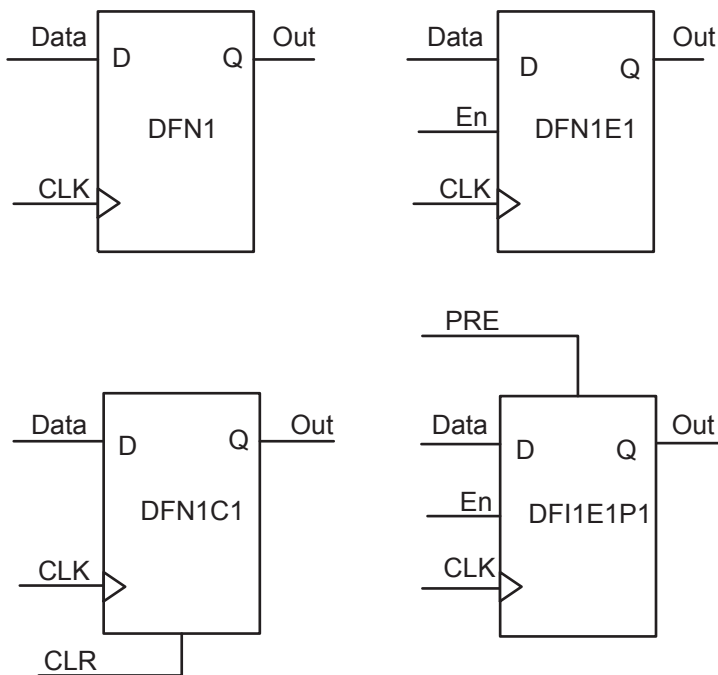


Figure 2-25 • Sample of Sequential Cells

Timing Waveforms

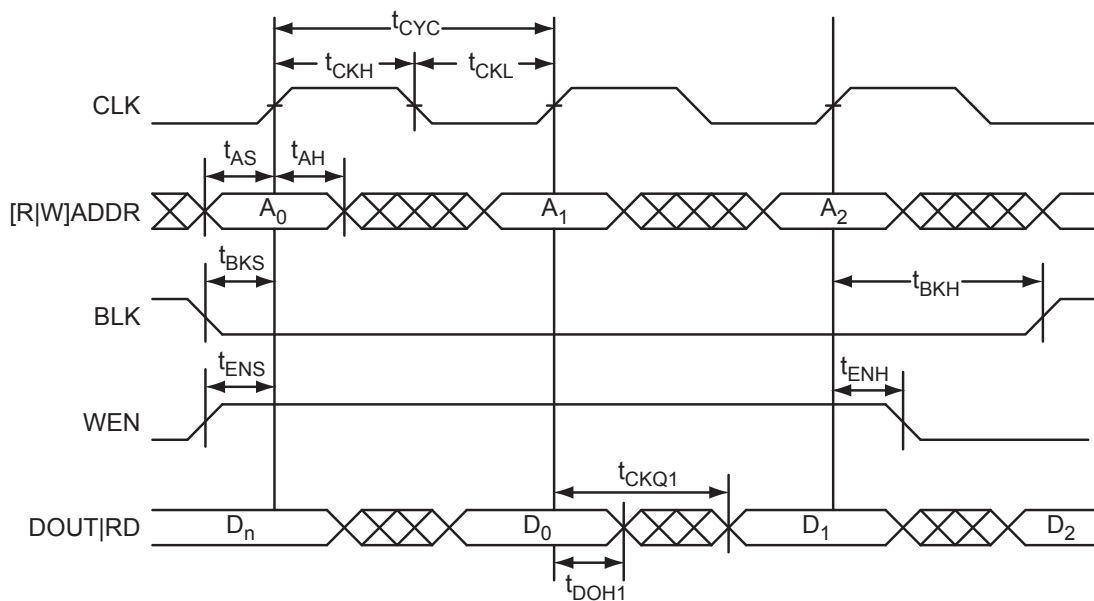


Figure 2-30 • RAM Read for Pass-Through Output. Applicable to both RAM4K9 and RAM512x18.

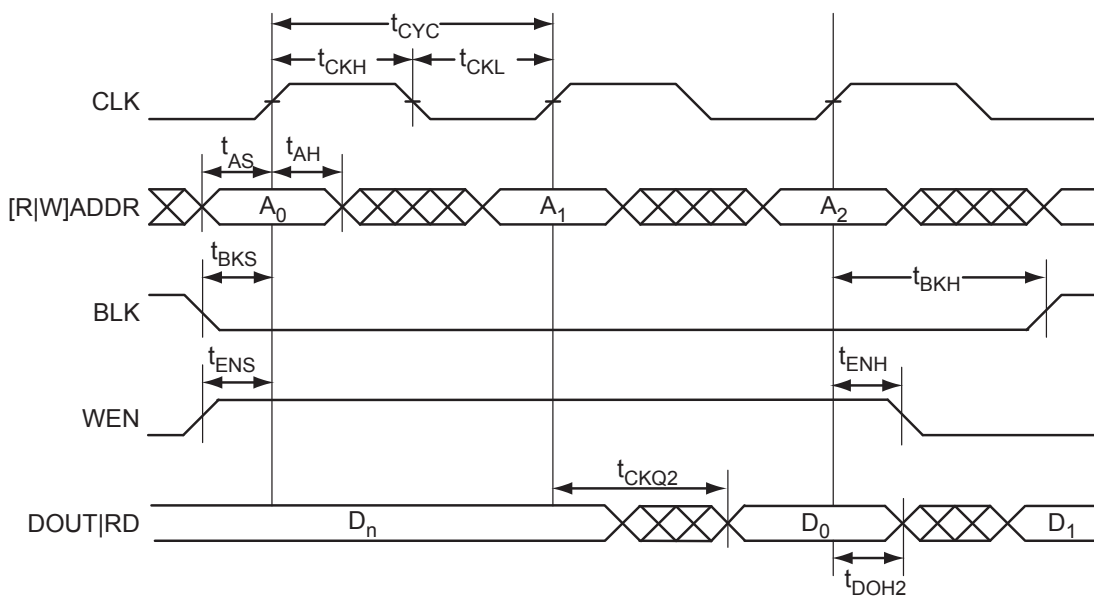


Figure 2-31 • RAM Read for Pipelined Output Applicable to both RAM4K9 and RAM512x18.

Table 2-95 • ADC Specifications (continued)

Specification	Test Conditions	Min.	Typ.	Max.	Units
Input leakage current	–40°C to +100°C		1		μA
Power supply rejection ratio	DC	44	53		dB
ADC power supply operational current requirements	VCC33ADCx			2.5	mA
	VCC15A			2	mA

Note: All 3.3 V supplies are tied together and varied from 3.0 V to 3.6 V. 1.5 V supplies are held constant.

Analog Bipolar Prescaler (ABPS)

With the ABPS set to its high range setting (GDEC = 00), a hypothetical input voltage in the range –15.36 V to +15.36 V is scaled and offset by the ABPS input amplifier to match the ADC full range of 0 V to 2.56 V using a nominal gain of –0.08333 V/V. However, due to reliability considerations, the voltage applied to the ABPS input should never be outside the range of –11.5 V to +14.4 V, restricting the usable ADC input voltage to 2.238 V to 0.080 V and the corresponding 12-bit output codes to the range of 3581 to 128 (decimal), respectively.

Unless otherwise noted, ABPS performance is specified at 25°C with nominal power supply voltages, with the output measured using the internal voltage reference with the internal ADC in 12-bit mode and 100 KHz sampling frequency, after trimming and digital compensation; and applies to all ranges.

Table 2-96 • ABPS Performance Specifications

Specification	Test Conditions	Min.	Typ.	Max.	Units
Input voltage range (for driving ADC over its full range)	GDEC[1:0] = 11		±2.56		V
	GDEC[1:0] = 10		±5.12		V
	GDEC[1:0] = 01		±10.24		V
	GDEC[1:0] = 00 (limited by maximum rating)		See note 1		V
Analog gain (from input pad to ADC input)	GDEC[1:0] = 11		–0.5		V/V
	GDEC[1:0] = 10		–0.25		V/V
	GDEC[1:0] = 01		–0.125		V/V
	GDEC[1:0] = 00		–0.0833		V/V
Gain error		–2.8	–0.4	0.7	%
	–40°C to +100°C	–2.8	–0.4	0.7	%

Note: *FS is full-scale error, defined as the difference between the actual value that triggers the transition to full-scale and the ideal analog full-scale transition value. Full-scale error equals offset error plus gain error. Refer to the Analog-to-Digital Converter chapter of the [SmartFusion Programmable Analog User's Guide](#) for more information.

Embedded Design

Microsemi offers FREE SoftConsole Eclipse based IDE, which includes the GNU C/C++ compiler and GDB debugger. Microsemi also offers evaluation versions of software from Keil and IAR, with full versions available from respective suppliers.

Analog Design

The MSS configurator provides graphical configuration for current, voltage and temperature monitors, sample sequencing setup and post-processing configuration, as well as DAC output.

The MSS configurator creates a bridge between the FPGA fabric and embedded designers so device configuration can be easily shared between multiple developers.

The MSS configurator includes the following:

- A simple configurator for the embedded designer to control the MSS peripherals and I/Os
- A method to import and view a hardware configuration from the FPGA flow into the embedded flow containing the memory map
- Automatic generation of drivers for any peripherals or soft IP used in the system configuration
- Comprehensive analog configuration for the programmable analog components
- Creation of a standard MSS block to be used in SmartDesign for connection of FPGA fabric designs and IP

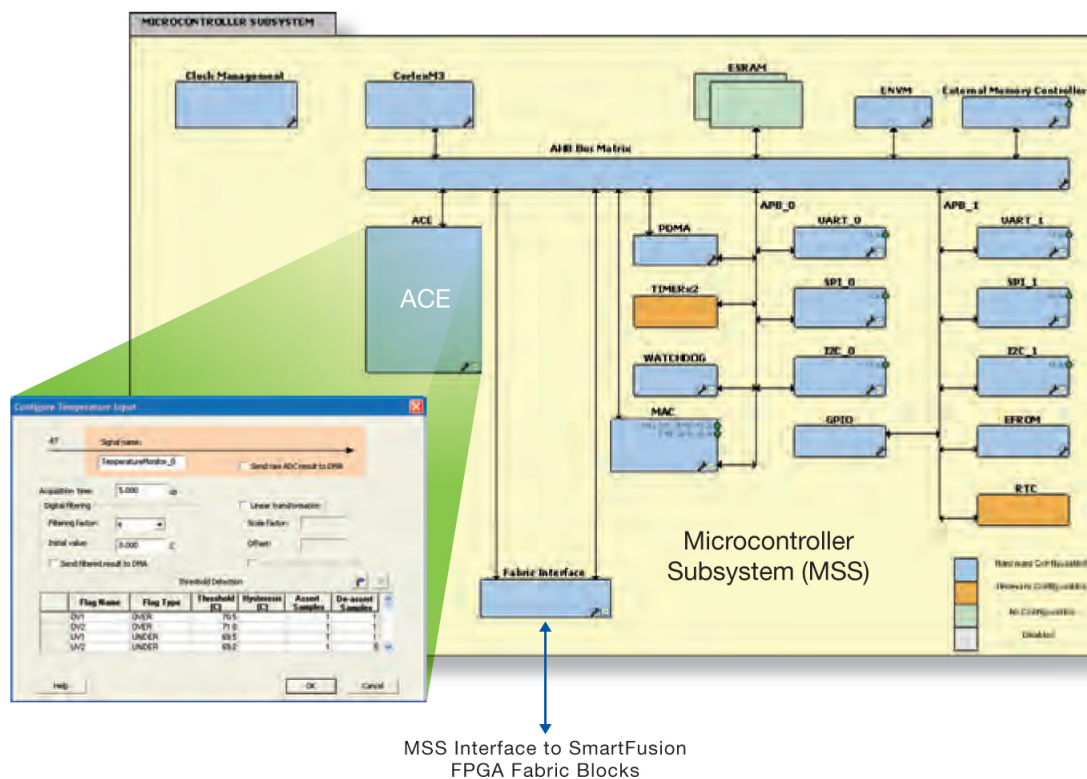


Figure 3-2 • MSS Configurator

Compile and Debug

Microsemi's SoftConsole is a free Eclipse-based IDE that enables the rapid production of C and C++ executables for Microsemi FPGA and cSoCs using Cortex-M3, Cortex-M1 and Core8051s. For SmartFusion support, SoftConsole includes the GNU C/C++ compiler and GDB debugger. Additional examples can be found on the SoftConsole page:

- [Using UART with SmartFusion: SoftConsole Standalone Flow Tutorial](#)
 - [Design Files](#)
- [Displaying POT Level with LEDs: Libero SoC and SoftConsole Flow Tutorial for SmartFusion](#)
 - [Design Files](#)

IAR Embedded Workbench® for ARM/Cortex is an integrated development environment for building and debugging embedded ARM applications using assembler, C and C++. It includes a project manager, editor, build and debugger tools with support for RTOS-aware debugging on hardware or in a simulator.

- [Designing SmartFusion cSoC with IAR Systems](#)
- [IAR Embedded Workbench IDE User Guide for ARM](#)
- [Download Evaluation or Kickstart version of IAR Embedded Workbench for ARM](#)

Keil's Microcontroller Development Kit comes in two editions: MDK-ARM and MDK Basic. Both editions feature µVision®, the ARM Compiler, MicroLib, and RTX, but the MDK Basic edition is limited to 256K so that small applications are more affordable.

- [Designing SmartFusion cSoC with Keil](#)
- [Using Keil µVision and Microsemi SmartFusion cSoC](#)
 - [Programming file for use with this tutorial](#)
- [Keil Microcontroller Development Kit for ARM Product Manuals](#)
- [Download Evaluation version of Keil MDK-ARM](#)

			
Software IDE	SoftConsole	Vision IDE	Embedded Workbench
Website	www.microsemi.com/soc	www.keil.com	www.iar.com
Free versions from SoC Products Group	Free with Libero SoC	32 K code limited	32 K code limited
Available from Vendor	N/A	Full version	Full version
Compiler	GNU GCC	RealView C/C++	IAR ARM Compiler
Debugger	GDB debug	Vision Debugger	C-SPY Debugger
Instruction Set Simulator	No	Vision Simulator	Yes
Debug Hardware	FlashPro4	ULINK2 or ULINK-ME	J-LINK or J-LINK Lite

Operating Systems

FreeRTOS™ is a portable, open source, royalty free, mini real-time kernel (a free-to-download and free-to-deploy RTOS that can be used in commercial applications without any requirement to expose your proprietary source code). FreeRTOS is scalable and designed specifically for small embedded systems. This FreeRTOS version ported by Microsemi is 6.0.1. For more information, visit the FreeRTOS website: www.freertos.org

- [SmartFusion Webserver Demo Using uIP and FreeRTOS](#)
- [SmartFusion cSoC: Running Webserver, TFTP on lwIP TCP/IP Stack Application Note](#)

Name	Type	Description	Associated With	
			ADC/SDD	SCB
TM0	In	SCB 0 / low side of current monitor / comparator Negative input / high side of temperature monitor. See the Temperature Monitor section.	ADC0	SCB0
TM1	In	SCB 1 / low side of current monitor / comparator. Negative input / high side of temperature monitor.	ADC0	SCB1
TM2	In	SCB 2 / low side of current monitor / comparator. Negative input / high side of temperature monitor.	ADC1	SCB2
TM3	In	SCB 3 low side of current monitor / comparator. Negative input / high side of temperature monitor.	ADC1	SCB3
TM4	In	SCB 4 low side of current monitor / comparator. Negative input / high side of temperature monitor.	ADC2	SCB4
SDD0	Out	Output of SDD0 See the Sigma-Delta Digital-to-Analog Converter (DAC) section in the SmartFusion Programmable Analog User's Guide .	SDD0	N/A
SDD1	Out	Output of SDD1	SDD1	N/A
SDD2	Out	Output of SDD2	SDD2	N/A

Note: Unused analog inputs should be grounded. This aids in shielding and prevents an undesired coupling path.

Analog Front-End Pin-Level Function Multiplexing

Table 5-2 describes the relationships between the various internal signals found in the analog front-end (AFE) and how they are multiplexed onto the external package pins. Note that, in general, only one function is available for those pads that have numerous functions listed. The exclusion to this rule is when a comparator is used; the ADC can still convert either input side of the comparator.

Table 5-2 • Relationships Between Signals in the Analog Front-End

Pin	ADC Channel	Dir.-In Option	Prescaler	Current Mon.	Temp. Mon.	Compar.	LVTTTL	SDD MUX	SDD
ABPS0	ADC0_CH1		ABPS0_IN						
ABPS1	ADC0_CH2		ABPS1_IN						
ABPS2	ADC0_CH5		ABPS2_IN						
ABPS3	ADC0_CH6		ABPS3_IN						
ABPS4	ADC1_CH1		ABPS4_IN						
ABPS5	ADC1_CH2		ABPS5_IN						
ABPS6	ADC1_CH5		ABPS6_IN						
ABPS7	ADC1_CH6		ABPS7_IN						
ABPS8	ADC2_CH1		ABPS8_IN						
ABPS9	ADC2_CH2		ABPS9_IN						
ADC0	ADC0_CH9	Yes				CMP1_P	LVTTTL0_IN		
ADC1	ADC0_CH10	Yes				CMP1_N	LVTTTL1_IN	SDDM0_OUT	
ADC2	ADC0_CH11	Yes				CMP3_P	LVTTTL2_IN		
ADC3	ADC0_CH12	Yes				CMP3_N	LVTTTL3_IN	SDDM1_OUT	
ADC4	ADC1_CH9	Yes				CMP5_P	LVTTTL4_IN		
ADC5	ADC1_CH10	Yes				CMP5_N	LVTTTL5_IN	SDDM2_OUT	
ADC6	ADC1_CH11	Yes				CMP7_P	LVTTTL6_IN		
ADC7	ADC1_CH12	Yes				CMP7_N	LVTTTL7_IN	SDDM3_OUT	
ADC8	ADC2_CH9	Yes				CMP9_P	LVTTTL8_IN		
ADC9	ADC2_CH10	Yes				CMP9_N	LVTTTL9_IN	SDDM4_OUT	
ADC10	ADC2_CH11	Yes					LVTTTL10_IN		
ADC11	ADC2_CH12	Yes					LVTTTL11_IN		
CM0	ADC0_CH3	Yes		CM0_H		CMP0_P			
CM1	ADC0_CH7	Yes		CM1_H		CMP2_P			
CM2	ADC1_CH3	Yes		CM2_H		CMP4_P			
CM3	ADC1_CH7	Yes		CM3_H		CMP6_P			
CM4	ADC2_CH3	Yes		CM4_H		CMP8_P			
SDD0	ADC0_CH15								SDD0_OUT
SDD1	ADC1_CH15								SDD1_OUT

Notes:

1. ABPSx_IN: Input to active bipolar prescaler channel x.
2. CMx_H/L: Current monitor channel x, high/low side.
3. TMx_IO: Temperature monitor channel x.
4. CMPx_P/N: Comparator channel x, positive/negative input.
5. LVTTTLx_IN: LVTTTL I/O channel x.
6. SDDMx_OUT: Output from sigma-delta DAC MUX channel x.
7. SDDx_OUT: Direct output from sigma-delta DAC channel x.

Pin No.	CS288		
	A2F060 Function	A2F200 Function	A2F500 Function
F12	EMC_AB[12]/IO10NDB0V0	EMC_AB[12]/IO10NDB0V0	EMC_AB[12]/IO14NDB0V0
F13	GND	GND	GND
F14	GCB1/IO19PPB0V0	GCC1/IO26PPB1V0	GCC1/IO35PPB1V0
F15	GNDQ	GNDQ	GNDQ
F16	VCCFPGAIOB1	VCCFPGAIOB1	VCCFPGAIOB1
F17	GCB0/IO19NPB0V0	IO24NDB1V0	IO33NDB1V0
F19	IO23NDB1V0	GDB1/IO30PDB1V0	GDB1/IO39PDB1V0
F21	GCA2/IO21PDB1V0	GDB0/IO30NDB1V0	GDB0/IO39NDB1V0
G1	IO41NDB5V0	IO67NDB5V0	IO84NDB5V0
G3	GFC2/IO41PDB5V0	GFC2/IO67PDB5V0	GFC2/IO84PDB5V0
G5	NC	GFB1/IO65PDB5V0	GFB1/IO82PDB5V0
G6	EMC_DB[10]/IO43NDB5V0	EMC_DB[10]/IO69NDB5V0	EMC_DB[10]/IO86NDB5V0
G9	NC	GFC0/IO66NPB5V0	GFC0/IO83NPB5V0
G13	GCA0/IO20NPB0V0	GCC0/IO26NPB1V0	GCC0/IO35NPB1V0
G16	NC	GDA0/IO31NDB1V0	GDA0/IO40NDB1V0
G17	IO22NPB1V0	GDC1/IO29PDB1V0	GDC1/IO38PDB1V0
G19	GCC2/IO23PDB1V0	GDC0/IO29NDB1V0	GDC0/IO38NDB1V0
G21	GND	GND	GND
H1	EMC_DB[9]/IO40PPB5V0	EMC_DB[9]/GEC1/IO63PPB5V0	EMC_DB[9]/GEC1/IO80PPB5V0
H3	GND	GND	GND
H5	NC	GFB0/IO65NDB5V0	GFB0/IO82NDB5V0
H6	EMC_DB[7]/IO39PDB5V0	EMC_DB[7]/GEB1/IO62PDB5V0	EMC_DB[7]/GEB1/IO79PDB5V0
H8	GND	GND	GND
H9	VCC	VCC	VCC
H10	GND	GND	GND
H11	VCC	VCC	VCC
H12	GND	GND	GND
H13	VCC	VCC	VCC
H14	GND	GND	GND
H16	NC	GDA1/IO31PDB1V0	GDA1/IO40PDB1V0
H17	NC	GDC2/IO32PPB1V0	GDC2/IO41PPB1V0

Notes:

1. Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.
2. *: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the [SmartFusion Microcontroller Subsystem User's Guide](#) for more details.

Pin No.	CS288		
	A2F060 Function	A2F200 Function	A2F500 Function
P19	VCCMSSIOB2	VCCMSSIOB2	VCCMSSIOB2
P21	GND	GND	GND
R1	GPIO_2/IO31RSB4V0	MAC_MDIO/IO49RSB4V0	MAC_MDIO/IO58RSB4V0
R3	GPIO_1/IO32RSB4V0	MAC_TXEN/IO52RSB4V0	MAC_TXEN/IO61RSB4V0
R5	GPIO_3/IO30RSB4V0	MAC_TXD[0]/IO56RSB4V0	MAC_TXD[0]/IO65RSB4V0
R6	GPIO_10/IO35RSB4V0	MAC_CRSDV/IO51RSB4V0	MAC_CRSDV/IO60RSB4V0
R9	GNDA	GNDA	GNDA
R13	GNDA	GNDA	GNDA
R16	UART_1_RXD/GPIO_29	UART_1_RXD/GPIO_29	UART_1_RXD/GPIO_29
R17	UART_1_TXD/GPIO_28	UART_1_TXD/GPIO_28	UART_1_TXD/GPIO_28
R19	I2C_0_SDA/GPIO_22	I2C_0_SDA/GPIO_22	I2C_0_SDA/GPIO_22
R21	I2C_1_SDA/GPIO_30	I2C_1_SDA/GPIO_30	I2C_1_SDA/GPIO_30
T1	GND	GND	GND
T3	NC	MAC_TXD[1]/IO55RSB4V0	MAC_TXD[1]/IO64RSB4V0
T5	NC	MAC_RXD[1]/IO53RSB4V0	MAC_RXD[1]/IO62RSB4V0
T6	GPIO_11/IO34RSB4V0	MAC_RXER/IO50RSB4V0	MAC_RXER/IO59RSB4V0
T7	NC	CM1	CM1
T8	NC	ADC1	ADC1
T9	NC	GND33ADC0	GND33ADC0
T10	NC	VCC15ADC0	VCC15ADC0
T11	GND33ADC0	GND33ADC1	GND33ADC1
T12	VAREF0	VAREF1	VAREF1
T13	ADC7	ADC4	ADC4
T14	TM0	TM3	TM3
T15	SPI_1_SS/GPIO_27	SPI_1_SS/GPIO_27	SPI_1_SS/GPIO_27
T16	VCCMSSIOB2	VCCMSSIOB2	VCCMSSIOB2
T17	UART_0_RXD/GPIO_21	UART_0_RXD/GPIO_21	UART_0_RXD/GPIO_21
T19	UART_0_TXD/GPIO_20	UART_0_TXD/GPIO_20	UART_0_TXD/GPIO_20
T21	I2C_1_SCL/GPIO_31	I2C_1_SCL/GPIO_31	I2C_1_SCL/GPIO_31
U1	NC	MAC_RXD[0]/IO54RSB4V0	MAC_RXD[0]/IO63RSB4V0
U3	VCCMSSIOB4	VCCMSSIOB4	VCCMSSIOB4

Notes:

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2. *: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the [SmartFusion Microcontroller Subsystem User's Guide](#) for more details.

Pin No.	FG256		
	A2F060 Function	A2F200 Function	A2F500 Function
B16	GNDQ	GNDQ	GNDQ
C1	EMC_DB[14]/IO45NDB0V0	EMC_DB[14]/GAB2/IO71NDB5V0	EMC_DB[14]/GAB2/IO88NDB5V0
C2	VCCPLL0	VCCPLL	VCCPLL0
C3	EMC_BYTEN[0]/IO02NDB0V0	EMC_BYTEN[0]/GAC0/IO02NDB0V0	EMC_BYTEN[0]/GAC0/IO07NDB0V0
C4	VCCFPGAIOB0	VCCFPGAIOB0	VCCFPGAIOB0
C5	EMC_CS0_N/IO01NDB0V0	EMC_CS0_N/GAB0/IO01NDB0V0	EMC_CS0_N/GAB0/IO05NDB0V0
C6	EMC_CS1_N/IO01PDB0V0	EMC_CS1_N/GAB1/IO01PDB0V0	EMC_CS1_N/GAB1/IO05PDB0V0
C7	GND	GND	GND
C8	EMC_AB[8]/IO08NDB0V0	EMC_AB[8]/IO08NDB0V0	EMC_AB[8]/IO13NDB0V0
C9	EMC_AB[11]/IO09PDB0V0	EMC_AB[11]/IO09PDB0V0	EMC_AB[11]/IO11PDB0V0
C10	VCCFPGAIOB0	VCCFPGAIOB0	VCCFPGAIOB0
C11	EMC_AB[17]/IO12PDB0V0	EMC_AB[17]/IO12PDB0V0	EMC_AB[17]/IO17PDB0V0
C12	EMC_AB[19]/IO13PDB0V0	EMC_AB[19]/IO13PDB0V0	EMC_AB[19]/IO18PDB0V0
C13	GND	GND	GND
C14	GCC0/IO18NPB0V0	GBA2/IO20PPB1V0	GBA2/IO27PPB1V0
C15	GCB0/IO19NDB0V0	GCA2/IO23PDB1V0	GCA2/IO28PDB1V0 *
C16	GCB1/IO19PDB0V0	IO23NDB1V0	IO28NDB1V0
D1	VCCFPGAIOB5	VCCFPGAIOB5	VCCFPGAIOB5
D2	VCOMPLA0	VCOMPLA	VCOMPLA0
D3	GND	GND	GND
D4	GNDQ	GNDQ	GNDQ
D5	EMC_CLK/IO00NDB0V0	EMC_CLK/GAA0/IO00NDB0V0	EMC_CLK/GAA0/IO02NDB0V0
D6	EMC_RW_N/IO00PDB0V0	EMC_RW_N/GAA1/IO00PDB0V0	EMC_RW_N/GAA1/IO02PDB0V0
D7	EMC_AB[6]/IO07NDB0V0	EMC_AB[6]/IO07NDB0V0	EMC_AB[6]/IO12NDB0V0
D8	EMC_AB[7]/IO07PDB0V0	EMC_AB[7]/IO07PDB0V0	EMC_AB[7]/IO12PDB0V0
D9	EMC_AB[10]/IO09NDB0V0	EMC_AB[10]/IO09NDB0V0	EMC_AB[10]/IO11NDB0V0
D10	EMC_AB[22]/IO15NDB0V0	EMC_AB[22]/IO15NDB0V0	EMC_AB[22]/IO19NDB0V0
D11	EMC_AB[23]/IO15PDB0V0	EMC_AB[23]/IO15PDB0V0	EMC_AB[23]/IO19PDB0V0
D12	GNDQ	GNDQ	GNDQ
D13	GCC1/IO18PPB0V0	GBB2/IO20NPB1V0	GBB2/IO27NPB1V0
D14	GCA0/IO20NDB0V0	GCB2/IO24PDB1V0	GCB2/IO33PDB1V0

Notes:

1. Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.
2. *: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the [SmartFusion Microcontroller Subsystem User's Guide](#) for more details.

Pin No.	FG256		
	A2F060 Function	A2F200 Function	A2F500 Function
H13	TDO	TDO	TDO
H14	TDI	TDI	TDI
H15	JTAGSEL	JTAGSEL	JTAGSEL
H16	GND	GND	GND
J1	EMC_DB[4]/IO38NPB5V0	EMC_DB[4]/GEA0/IO61NPB5V0	EMC_DB[4]/GEA0/IO78NPB5V0
J2	EMC_DB[3]/IO37PDB5V0	EMC_DB[3]/GEC2/IO60PDB5V0	EMC_DB[3]/GEC2/IO77PDB5V0
J3	EMC_DB[2]/IO37NDB5V0	EMC_DB[2]/IO60NDB5V0	EMC_DB[2]/IO77NDB5V0
J4	GNDRCOSC	GNDRCOSC	GNDRCOSC
J5	NC	GNDQ	GNDQ
J6	GND	GND	GND
J7	VCC	VCC	VCC
J8	GND	GND	GND
J9	VCC	VCC	VCC
J10	GND	GND	GND
J11	VCCMSSIOB2	VCCMSSIOB2	VCCMSSIOB2
J12	I2C_0_SCL/GPIO_23	I2C_0_SCL/GPIO_23	I2C_0_SCL/GPIO_23
J13	I2C_0_SDA/GPIO_22	I2C_0_SDA/GPIO_22	I2C_0_SDA/GPIO_22
J14	I2C_1_SCL/GPIO_31	I2C_1_SCL/GPIO_31	I2C_1_SCL/GPIO_31
J15	VCCMSSIOB2	VCCMSSIOB2	VCCMSSIOB2
J16	I2C_1_SDA/GPIO_30	I2C_1_SDA/GPIO_30	I2C_1_SDA/GPIO_30
K1	GPIO_1/IO32RSB4V0	MAC_MDIO/IO49RSB4V0	MAC_MDIO/IO58RSB4V0
K2	GPIO_0/IO33RSB4V0	MAC_MDC/IO48RSB4V0	MAC_MDC/IO57RSB4V0
K3	VCCMSSIOB4	VCCMSSIOB4	VCCMSSIOB4
K4	MSS_RESET_N	MSS_RESET_N	MSS_RESET_N
K5	VCCRCOSC	VCCRCOSC	VCCRCOSC
K6	VCCMSSIOB4	VCCMSSIOB4	VCCMSSIOB4
K7	GND	GND	GND
K8	VCC	VCC	VCC
K9	GND	GND	GND
K10	VCC	VCC	VCC
K11	GND	GND	GND

Notes:

1. Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.
2. *: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the [SmartFusion Microcontroller Subsystem User's Guide](#) for more details.

Pin Number	FG484	
	A2F200 Function	A2F500 Function
F17	NC	IO25PPB1V0
F18	VCCFPGAIOB1	VCCFPGAIOB1
F19	IO23NDB1V0	IO28NDB1V0
F20	NC	IO31PDB1V0
F21	NC	IO31NDB1V0
F22	IO22PDB1V0	IO32PDB1V0
G1	GND	GND
G2	GFB0/IO65NPB5V0	GFB0/IO82NPB5V0
G3	EMC_DB[9]/GEC1/IO63PDB5V0	EMC_DB[9]/GEC1/IO80PDB5V0
G4	GFC1/IO66PPB5V0	GFC1/IO83PPB5V0
G5	EMC_DB[11]/IO69PPB5V0	EMC_DB[11]/IO86PPB5V0
G6	GNDQ	GNDQ
G7	NC	NC
G8	GND	GND
G9	VCCFPGAIOB0	VCCFPGAIOB0
G10	GND	GND
G11	VCCFPGAIOB0	VCCFPGAIOB0
G12	GND	GND
G13	VCCFPGAIOB0	VCCFPGAIOB0
G14	GND	GND
G15	VCCFPGAIOB0	VCCFPGAIOB0
G16	GNDQ	GNDQ
G17	NC	IO26PDB1V0
G18	NC	IO26NDB1V0
G19	GCA2/IO23PDB1V0	GCA2/IO28PDB1V0 *
G20	IO24NDB1V0	IO33NDB1V0
G21	GCB2/IO24PDB1V0	GCB2/IO33PDB1V0
G22	GND	GND
H1	EMC_DB[7]/GEB1/IO62PDB5V0	EMC_DB[7]/GEB1/IO79PDB5V0
H2	VCCFPGAIOB5	VCCFPGAIOB5
H3	EMC_DB[8]/GEC0/IO63NDB5V0	EMC_DB[8]/GEC0/IO80NDB5V0
H4	GND	GND
H5	GFC0/IO66NPB5V0	GFC0/IO83NPB5V0
H6	GFA1/IO64PDB5V0	GFA1/IO81PDB5V0

Notes:

1. Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.
2. *: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the [SmartFusion Microcontroller Subsystem User's Guide](#) for more details.

Pin Number	FG484	
	A2F200 Function	A2F500 Function
M21	VPP	VPP
M22	IO32NDB1V0	IO41NDB1V0
N1	GND	GND
N2	NC	IO70PDB5V0
N3	NC	IO70NDB5V0
N4	VCCRCOSC	VCCRCOSC
N5	VCCFPGAIOB5	VCCFPGAIOB5
N6	NC	IO68NDB5V0
N7	VCCFPGAIOB5	VCCFPGAIOB5
N8	GND	GND
N9	VCC	VCC
N10	GND	GND
N11	VCC	VCC
N12	GND	GND
N13	VCC	VCC
N14	GND	GND
N15	VCC	VCC
N16	NC	GND
N17	NC	NC
N18	VCCFPGAIOB1	VCCFPGAIOB1
N19	VCCENVM	VCCENVM
N20	GNDENVM	GNDENVM
N21	NC	NC
N22	GND	GND
P1	NC	IO69NDB5V0
P2	NC	IO69PDB5V0
P3	GNDRCOSC	GNDRCOSC
P4	GND	GND
P5	NC	NC
P6	NC	NC
P7	GND	GND
P8	VCC	VCC
P9	GND	GND
P10	VCC	VCC

Notes:

1. Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.
2. *: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the [SmartFusion Microcontroller Subsystem User's Guide](#) for more details.

Revision	Changes	Page
Revision 7 (continued)	Usage instructions, such as how to handle the pin when unused, were added for the following supply pins (SAR 29769): "VCC15A" "VCC15ADC0" through "VCC15ADC2" "VCC33ADC0" through "VCC33ADC2" "VCC33AP" "VCC33ADC2" "VCCLPXTAL" "VCCMAINXTAL" "VCCMSSIOB2" "VCCPLLx" "VCCRCOSC" "VDDBAT"	5-2 through 5-3
	The "IO" description was revised to clarify the definitions of u, I/O pair, and w, differential pair (SAR 31147). Information on configuration of unused I/Os (including unused MSS I/Os, SAR 26891) was added (SAR 32643).	5-6
	Usage instructions were added for the following pins (SAR 29769): "MSS_RESET_N" "TCK" "TMS" "TRSTB" "MAC_CLK"	5-9 through 5-13
	Package names used in the "Pin Assignment Tables" section were revised to match standards given in <i>Package Mechanical Drawings</i> (SAR 27395).	5-18
	The pin assignments for A2F060 for "TQ144" and "FG256" have been revised due to the device status change from advance to preliminary (SAR 33068). The "TQ144" and "FG256" pin assignment sections previously compared functions between A2F060/A2F200 devices in one table and A2F200/A2F500 in a separate table. Functions for all three devices have now been combined into one table for each package (SAR 33072).	5-18, 5-42
	The "PQ208" pin table was revised for A2F500 to remove EMC functions, which are not available for this device/package combination (SAR 33041).	5-34
Revision 6 (March 2011)	The "PQ208" package was added to product tables and "Product Ordering Codes" for A2F200 and A2F500 (SAR 31005).	III
	The "Package I/Os: MSS + FPGA I/Os" table was revised to add the CS288 package for A2F060 and the PQ208 package for A2F200 and A2F500. A row was added for shared analog inputs (SAR 31034).	III
	The "SmartFusion cSoC Device Status" table was updated (SAR 31084).	III
	VCCESRAM was added to Table 2-1 • Absolute Maximum Ratings, Table 2-3 • Recommended Operating Conditions ^{5,6} , Table 2-8 • Power Supplies Configuration, and the "Supply Pins" table (SAR 31035).	2-1, 2-3, 2-10, 5-1
	The following note was removed from Table 2-8 • Power Supplies Configuration (SAR 30984): "Current monitors and temperature monitors should not be used when Power-Down and/or Sleep mode are required by the application."	2-10