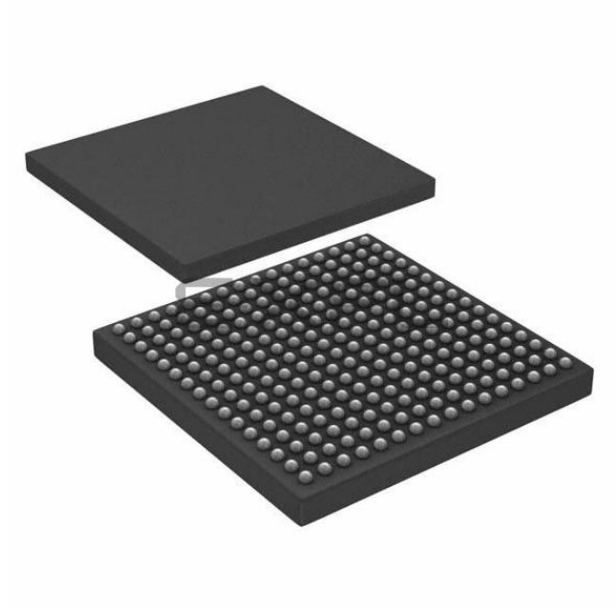

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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details	
Product Status	Obsolete
Architecture	MCU, FPGA
Core Processor	ARM® Cortex®-M3
Flash Size	128KB
RAM Size	16KB
Peripherals	DMA, POR, WDT
Connectivity	EBI/EMI, I²C, SPI, UART/USART
Speed	100MHz
Primary Attributes	ProASIC®3 FPGA, 60K Gates, 1536D-Flip-Flops
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/a2f060m3e-1fgg256

SmartFusion Family Overview

SmartFusion DC and Switching Characteristics

SmartFusion Development Tools

SmartFusion Programming

Pin Descriptions

Datasheet Information

Theta-JA

Junction-to-ambient thermal resistance (θ_{JA}) is determined under standard conditions specified by JEDEC (JESD-51), but it has little relevance in actual performance of the product. It should be used with caution but is useful for comparing the thermal performance of one package to another.

A sample calculation showing the maximum power dissipation allowed for the A2F200-FG484 package under forced convection of 1.0 m/s and 75°C ambient temperature is as follows:

$$\text{Maximum Power Allowed} = \frac{T_{J(MAX)} - T_{A(MAX)}}{\theta_{JA}}$$

EQ 4

where

θ_{JA} = 19.00°C/W (taken from Table 2-6 on page 2-7).

T_A = 75.00°C

$$\text{Maximum Power Allowed} = \frac{100.00°C - 75.00°C}{19.00°C/W} = 1.3\ W$$

EQ 5

The power consumption of a device can be calculated using the Microsemi SoC Products Group power calculator. The device's power consumption must be lower than the calculated maximum power dissipation by the package. If the power consumption is higher than the device's maximum allowable power dissipation, a heat sink can be attached on top of the case, or the airflow inside the system must be increased.

Theta-JB

Junction-to-board thermal resistance (θ_{JB}) measures the ability of the package to dissipate heat from the surface of the chip to the PCB. As defined by the JEDEC (JESD-51) standard, the thermal resistance from junction to board uses an isothermal ring cold plate zone concept. The ring cold plate is simply a means to generate an isothermal boundary condition at the perimeter. The cold plate is mounted on a JEDEC standard board with a minimum distance of 5.0 mm away from the package edge.

Theta-JC

Junction-to-case thermal resistance (θ_{JC}) measures the ability of a device to dissipate heat from the surface of the chip to the top or bottom surface of the package. It is applicable for packages used with external heat sinks. Constant temperature is applied to the surface in consideration and acts as a boundary condition. This only applies to situations where all or nearly all of the heat is dissipated through the surface in consideration.

Calculation for Heat Sink

For example, in a design implemented in an A2F200-FG484 package with 2.5 m/s airflow, the power consumption value using the power calculator is 3.00 W. The user-dependent T_a and T_j are given as follows:

T_J = 100.00°C

T_A = 70.00°C

From the datasheet:

θ_{JA} = 17.00°C/W

θ_{JC} = 8.28°C/W

$$P = \frac{T_J - T_A}{\theta_{JA}} = \frac{100°C - 70°C}{17.00\ W} = 1.76\ W$$

EQ 6

The 1.76 W power is less than the required 3.00 W. The design therefore requires a heat sink, or the airflow where the device is mounted should be increased. The design's total junction-to-air thermal resistance requirement can be estimated by EQ 7:

$$\theta_{JA(total)} = \frac{T_J - T_A}{P} = \frac{100°C - 70°C}{3.00\ W} = 10.00°C/W$$

EQ 7

Determining the heat sink's thermal performance proceeds as follows:

$$\theta_{JA(TOTAL)} = \theta_{JC} + \theta_{CS} + \theta_{SA}$$

EQ 8

where

θ_{JA} = 0.37°C/W

= Thermal resistance of the interface material between the case and the heat sink, usually provided by the thermal interface manufacturer

θ_{SA} = Thermal resistance of the heat sink in °C/W

$$\theta_{SA} = \theta_{JA(TOTAL)} - \theta_{JC} - \theta_{CS}$$

EQ 9

$$\theta_{SA} = 13.33°C/W - 8.28°C/W - 0.37°C/W = 5.01°C/W$$

A heat sink with a thermal resistance of 5.01°C/W or better should be used. Thermal resistance of heat sinks is a function of airflow. The heat sink performance can be significantly improved with increased airflow.

Carefully estimating thermal resistance is important in the long-term reliability of an FPGA. Design engineers should always correlate the power consumption of the device with the maximum allowable power dissipation of the package selected for that device.

Note: The junction-to-air and junction-to-board thermal resistances are based on JEDEC standard (JESD-51) and assumptions made in building the model. It may not be realized in actual application and therefore should be used with a degree of caution. Junction-to-case thermal resistance assumes that all power is dissipated through the case.

Temperature and Voltage Derating Factors

Table 2-7 • **Temperature and Voltage Derating Factors for Timing Delays (normalized to T_J = 85°C, worst-case VCC = 1.425 V)**

Array Voltage VCC (V)	Junction Temperature (°C)					
	–40°C	**0°C**	**25°C**	**70°C**	**85°C**	**100°C**
1.425	0.86	0.91	0.93	0.98	1.00	1.02
1.500	0.81	0.86	0.88	0.93	0.95	0.96
1.575	0.78	0.83	0.85	0.90	0.91	0.93

Power Calculation Methodology

This section describes a simplified method to estimate power consumption of an application. For more accurate and detailed power estimations, use the SmartPower tool in the Libero SoC software.

The power calculation methodology described below uses the following variables:

- The number of PLLs/CCCs as well as the number and the frequency of each output clock generated
- The number of combinatorial and sequential cells used in the design
- The internal clock frequencies
- The number and the standard of I/O pins used in the design
- The number of RAM blocks used in the design
- The number of eNVM blocks used in the design
- The analog block used in the design, including the temperature monitor, current monitor, ABPS, sigma-delta DAC, comparator, low power crystal oscillator, RC oscillator and the main crystal oscillator
- Toggle rates of I/O pins as well as VersaTiles—guidelines are provided in Table 2-17 on page 2-18.
- Enable rates of output buffers—guidelines are provided for typical applications in Table 2-18 on page 2-18.
- Read rate and write rate to the memory—guidelines are provided for typical applications in Table 2-18 on page 2-18.
- Read rate to the eNVM blocks

The calculation should be repeated for each clock domain defined in the design.

Methodology

Total Power Consumption—P_{TOTAL}

SoC Mode, Standby Mode, and Time Keeping Mode.

$P_{TOTAL} = P_{STAT} + P_{DYN}$

P_{STAT} is the total static power consumption.

P_{DYN} is the total dynamic power consumption.

Total Static Power Consumption—P_{STAT}

SoC Mode

$P_{STAT} = P_{DC1} + (N_{INPUTS} * P_{DC7}) + (N_{OUTPUTS} * P_{DC8}) + (N_{PLLS} * P_{DC9})$

N_{INPUTS} is the number of I/O input buffers used in the design.

$N_{OUTPUTS}$ is the number of I/O output buffers used in the design.

N_{PLLS} is the number of PLLs available in the device.

Standby Mode

$P_{STAT} = P_{DC2}$

Time Keeping Mode

$P_{STAT} = P_{DC3}$

Total Dynamic Power Consumption—P_{DYN}

SoC Mode

$P_{DYN} = P_{CLOCK} + P_{S\text{-}CELL} + P_{C\text{-}CELL} + P_{NET} + P_{INPUTS} + P_{OUTPUTS} + P_{MEMORY} + P_{PLL} + P_{eNVM} + P_{XTL\text{-}OSC} + P_{RC\text{-}OSC} + P_{AB} + P_{LPXTAL\text{-}OSC} + P_{MSS}$

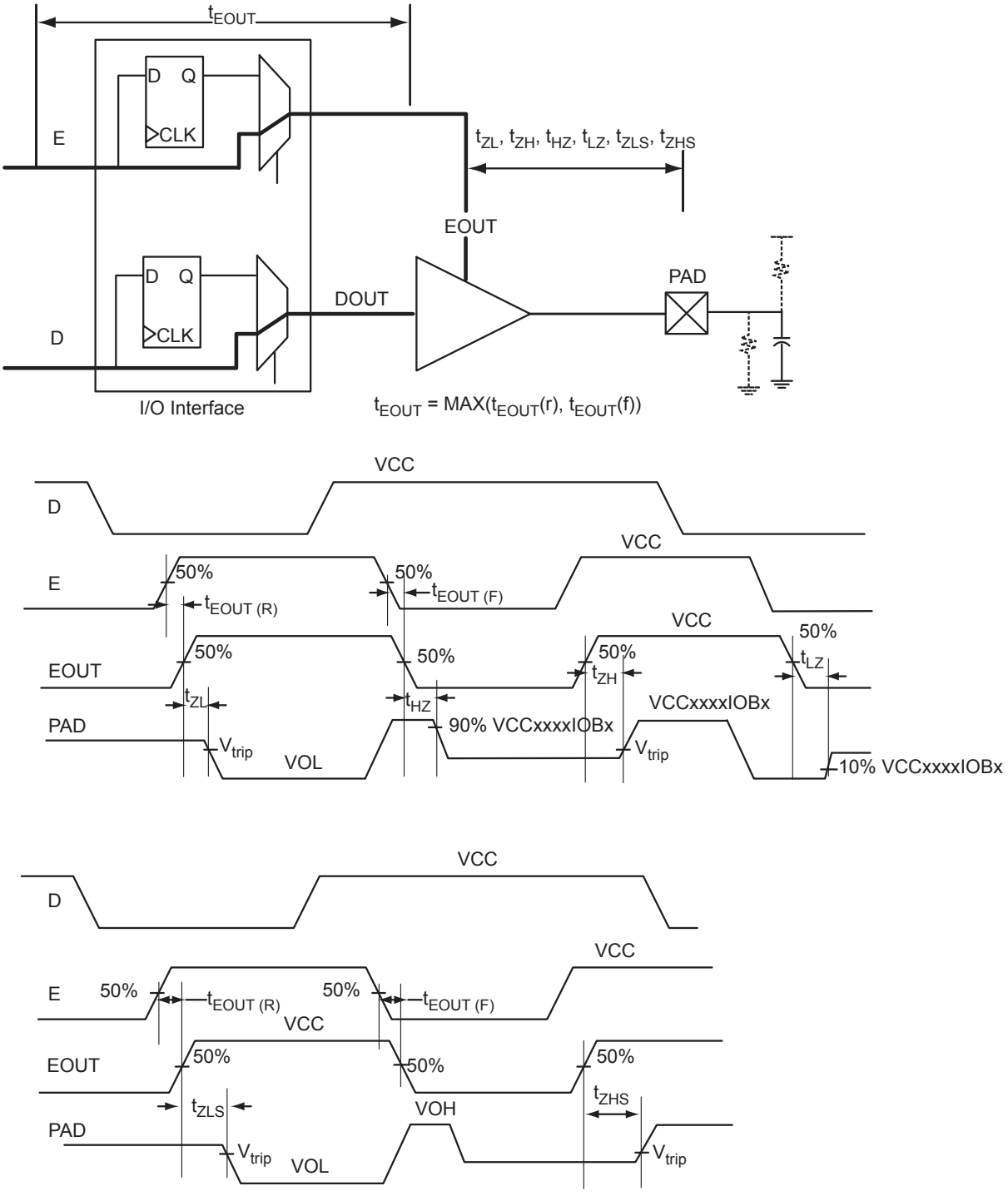


Figure 2-5 • **Tristate Output Buffer Timing Model and Delays (example)**

Table 2-63 • LVDS Minimum and Maximum DC Input and Output Levels

DC Parameter	Description	Min.	Typ.	Max.	Units
VCCFPGAIOBx	Supply voltage	2.375	2.5	2.625	V
VOL	Output low voltage	0.9	1.075	1.25	V
VOH	Output high voltage	1.25	1.425	1.6	V
I_{OL}[1]	Output lower current	0.65	0.91	1.16	mA
I_{OH}[1]	Output high current	0.65	0.91	1.16	mA
VI	Input voltage	0		2.925	V
I_{IH}[2]	Input high leakage current			15	µA
I_{IL}[2]	Input low leakage current			15	µA
V_{ODIFF}	Differential output voltage	250	350	450	mV
V_{OCM}	Output common mode voltage	1.125	1.25	1.375	V
V_{ICM}	Input common mode voltage	0.05	1.25	2.35	V
V_{IDIFF}	Input differential voltage	100	350		mV

Notes:

1. *I_{OL}/I_{OH} defined by V_{ODIFF}/(resistor network).*
2. *Currents are measured at 85°C junction temperature.*

Table 2-64 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	V_{REF} (typ.) (V)
1.075	1.325	Cross point	–

* *Measuring point = V_{trip}. See Table 2-22 on page 2-24 for a complete table of trip points.*

Timing Characteristics

Table 2-65 • LVDS
Worst Commercial-Case Conditions: T_J = 85°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCFPGAIOBx = 2.3 V
Applicable to FPGA I/O Banks, I/O Assigned to EMC I/O Pins

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	Units
Std.	0.60	1.83	0.04	1.87	ns
–1	0.50	1.53	0.03	1.55	ns

Notes:

1. *For the derating values at specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.*
2. *The above mentioned timing parameters correspond to 24mA drive strength.*

B-LVDS/M-LVDS

Bus LVDS (B-LVDS) and Multipoint LVDS (M-LVDS) specifications extend the existing LVDS standard to high-performance multipoint bus applications. Multidrop and multipoint bus configurations may contain any combination of drivers, receivers, and transceivers. SoC Products Group LVDS drivers provide the higher drive current required by B-LVDS and M-LVDS to accommodate the loading. The drivers require series terminations for better signal quality and to control voltage swing. Termination is also required at both ends of the bus since the driver can be located anywhere on the bus. These configurations can be implemented using the TRIBUF_LVDS and BIBUF_LVDS macros along with appropriate terminations. Multipoint designs using SoC Products Group LVDS macros can achieve up to 200 MHz with a maximum of 20 loads. A sample application is given in Figure 2-12. The input and output buffer delays are available in the LVDS section in Table 2-65.

Example: For a bus consisting of 20 equidistant loads, the following terminations provide the required differential voltage, in worst-case commercial operating conditions, at the farthest receiver: R_S = 60 Ω and R_T = 70 Ω, given Z_0 = 50 Ω (2") and Z_{stub} = 50 Ω (~1.5").

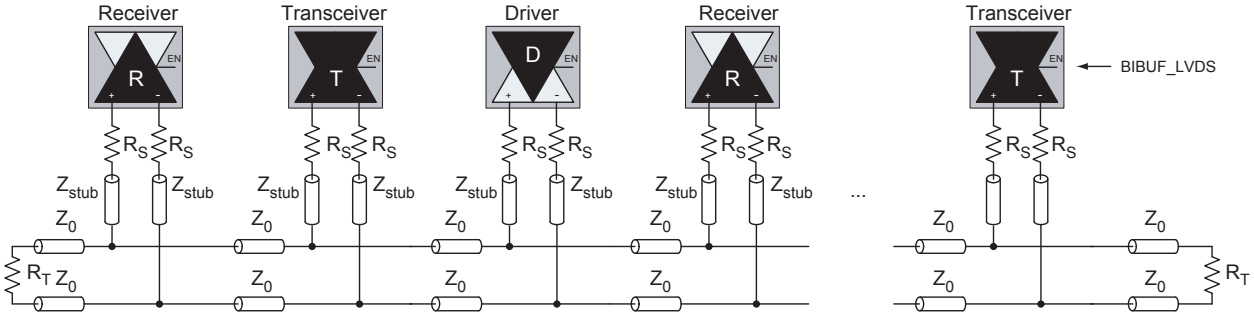


Figure 2-12 • **B-LVDS/M-LVDS Multipoint Application Using LVDS I/O Buffers**

LVPECL

Low-Voltage Positive Emitter-Coupled Logic (LVPECL) is another differential I/O standard. It requires that one data bit be carried through two signal lines. Like LVDS, two pins are needed. It also requires external resistor termination.

The full implementation of the LVDS transmitter and receiver is shown in an example in Figure 2-13. The building blocks of the LVPECL transmitter-receiver are one transmitter macro, one receiver macro, three board resistors at the transmitter end, and one resistor at the receiver end. The values for the three driver resistors are different from those used in the LVDS implementation because the output standard specifications are different.

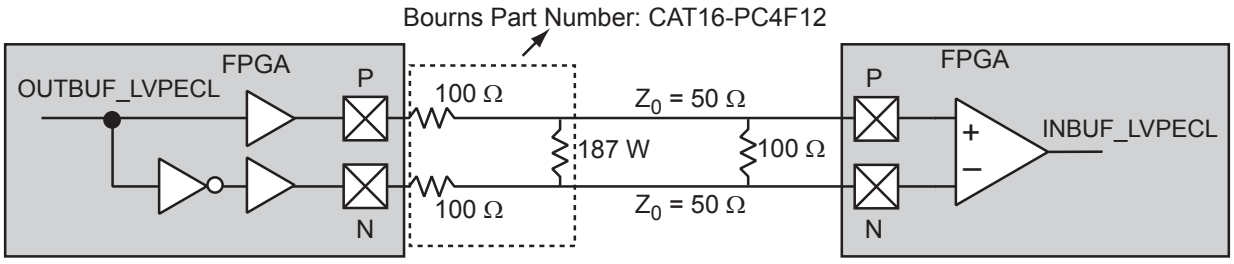


Figure 2-13 • **LVPECL Circuit Diagram and Board-Level Implementation**

DDR Module Specifications

Input DDR Module

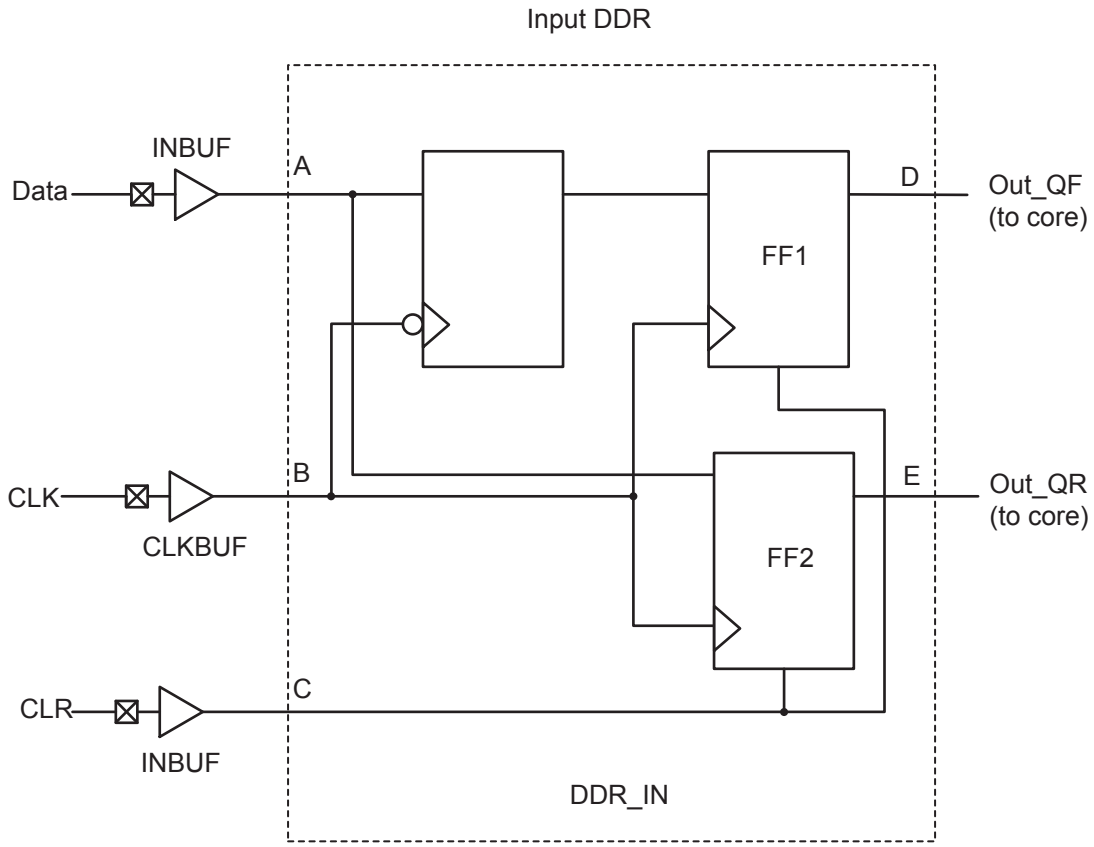


Figure 2-19 • **Input DDR Timing Model**

Table 2-74 • **Parameter Definitions**

Parameter Name	Parameter Definition	Measuring Nodes (from, to)
$t_{DDRICLKQ1}$	Clock-to-Out Out_QR	B, D
$t_{DDRICLKQ2}$	Clock-to-Out Out_QF	B, E
$t_{DDRISUD}$	Data Setup Time of DDR input	A, B
t_{DDRIHD}	Data Hold Time of DDR input	A, B
$t_{DDRICLR2Q1}$	Clear-to-Out Out_QR	C, D
$t_{DDRICLR2Q2}$	Clear-to-Out Out_QF	C, E
$t_{DDRIREMCLR}$	Clear Removal	C, B
$t_{DDRIRECCLR}$	Clear Recovery	C, B

FIFO

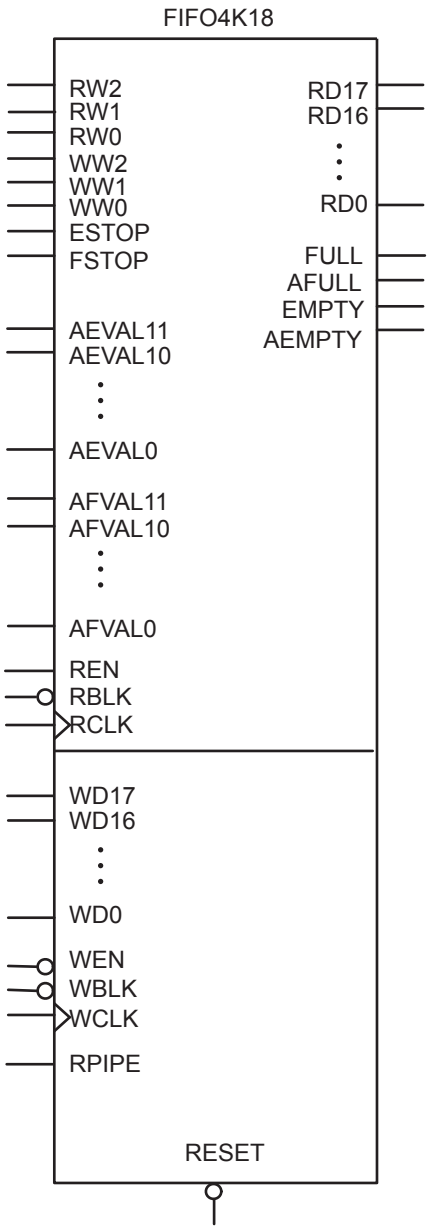


Figure 2-35 • **FIFO Model**

Temperature Monitor

Unless otherwise noted, temperature monitor performance is specified with a 2N3904 diode-connected bipolar transistor from National Semiconductor or Infineon Technologies, nominal power supply voltages, with the output measured using the internal voltage reference with the internal ADC in 12-bit mode and 62.5 Ksps. After digital compensation. Unless otherwise noted, the specifications pertain to conditions where the SmartFusion cSoC and the sensing diode are at the same temperature.

Table 2-94 • **Temperature Monitor Performance Specifications**

Specification	Test Conditions	Min.	Typical	Max.	Units
Input diode temperature range		–55		150	°C
		233.2		378.15	K
Temperature sensitivity			2.5		mV/K
Intercept	Extrapolated to 0K		0		V
Input referred temperature offset error	At 25°C (298.15K)		±1	1.5	°C
Gain error	Slope of BFSL vs. 2.5 mV/K		±1	2.5	% nom.
Overall accuracy	Peak error from ideal transfer function		±2	±3	°C
Input referred noise	At 25°C (298.15K) – no output averaging		4		°C rms
Output current	Idle mode		100		µA
	Final measurement phases		10		µA
Analog settling time	Measured to 0.1% of final value, (with ADC load)				
	From TM_STB (High)	5			µs
	From ADC_START (High)	5		105	µs
AT parasitic capacitance				500	pF
Power supply rejection ratio	DC (0–10 KHz)	1.2	0.7		°C/V
Input referred temperature sensitivity error	Variation due to device temperature (–40°C to +100°C). External temperature sensor held constant.		0.005	0.008	°C/°C
Temperature monitor (TM) operational power supply current requirements (per temperature monitor instance, not including ADC or VAREFx)	VCC33A		200		µA
	VCC33AP		150		µA
	VCC15A		50		µA

Note: All results are based on averaging over 64 samples.

Analog-to-Digital Converter (ADC)

Unless otherwise noted, ADC direct input performance is specified at 25°C with nominal power supply voltages, with the output measured using the external voltage reference with the internal ADC in 12-bit mode and 500 KHz sampling frequency, after trimming and digital compensation.

***Table 2-95* • ADC Specifications**

Specification	Test Conditions	Min.	Typ.	Max.	Units
Input voltage range (for driving ADC over its full range)			2.56		V
Gain error			±0.4	±0.7	%
	–40ºC to +100ºC		±0.4	±0.7	%
Input referred offset voltage			±1	±2	mV
	–40ºC to +100ºC		±1	±2	
Integral non-linearity (INL)	RMS deviation from BFSL				
	12-bit mode		1.71		LSB
	10-bit mode		0.60	1.00	LSB
	8-bit mode		0.2	0.33	LSB
Differential non-linearity (DNL)	12-bit mode		2.4		LSB
	10-bit mode		0.80	0.94	LSB
	8-bit mode		0.2	0.23	LSB
Signal to noise ratio		62	64		dB
Effective number of bits (ENOB) $ENOB = \frac{SINAD - 1.76\ dB}{6.02\ dB/bit}$ *EQ 10*	–1 dBFS input				
	12-bit mode 10 KHz	9.9	10		Bits
	12-bit mode 100 KHz	9.9	10		Bits
	10-bit mode 10 KHz	9.5	9.6		Bits
	10-bit mode 100 KHz	9.5	9.6		Bits
	8-bit mode 10 KHz	7.8	7.9		Bits
	8-bit mode 100 KHz	7.8	7.9		Bits
Full power bandwidth	At –3 dB; –1 dBFS input	300			KHz
Analog settling time	To 0.1% of final value (with 1 Kohm source impedance and with ADC load)		2		µs
Input capacitance	Switched capacitance (ADC sample capacitor)		12	15	pF
	Cs: Static capacitance (Figure 2-44 on page 2-86)				
	CM[n] input		5	7	pF
	TM[n] input		5	7	pF
	ADC[n] input		5	7	pF
Input resistance	Rin: Series resistance (Figure 2-44)		2		KΩ
	Rsh: Shunt resistance, exclusive of switched capacitance effects (Figure 2-44)	10			MΩ

Note: All 3.3 V supplies are tied together and varied from 3.0 V to 3.6 V. 1.5 V supplies are held constant.

Voltage Regulator

Table 2-99 • **Voltage Regulator**

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
V_{OUT}	Output voltage	T_J = 25°C		1.425	1.5	1.575	V
V_{OS}	Output offset voltage	T_J = 25°C			11		mV
ICC33A	Operation current	T_J = 25°C	I_{LOAD} = 1 mA		3.4		mA
			I_{LOAD} = 100 mA		11		mA
			I_{LOAD} = 0.5 A		21		mA
ΔV_{OUT}	Load regulation	T_J = 25°C	I_{LOAD} = 1 mA to 0.5 A		5.8		mV
ΔV_{OUT}	Line regulation	T_J = 25°C	VCC33A = 2.97 V to 3.63 V I_{LOAD} = 1 mA		5.3		mV/V
			VCC33A = 2.97 V to 3.63 V I_{LOAD}= 100 mA		5.3		mV/V
			VCC33A = 2.97 V to 3.63 V I_{LOAD} = 500mA		5.3		mV/V
	Dropout voltage[1]	T_J = 25°C	I_{LOAD} = 1 mA		0.63		V
			I_{LOAD} = 100 mA		0.84		V
			I_{LOAD} = 0.5 A		1.35		V
I_{PTBASE}	PTBase current	T_J = 25°C	I_{LOAD} = 1 mA		48		µA
			I_{LOAD} = 100 mA		736		µA
			I_{LOAD} = 0.5 A		12		mA
	Startup time[2]	T_J = 25°C			200		µs

Notes:

1. *Dropout voltage is defined as the minimum VCC33A voltage. The parameter is specified with respect to the output voltage. The specification represents the minimum input-to-output differential voltage required to maintain regulation.*
2. *Assumes 10 µF.*

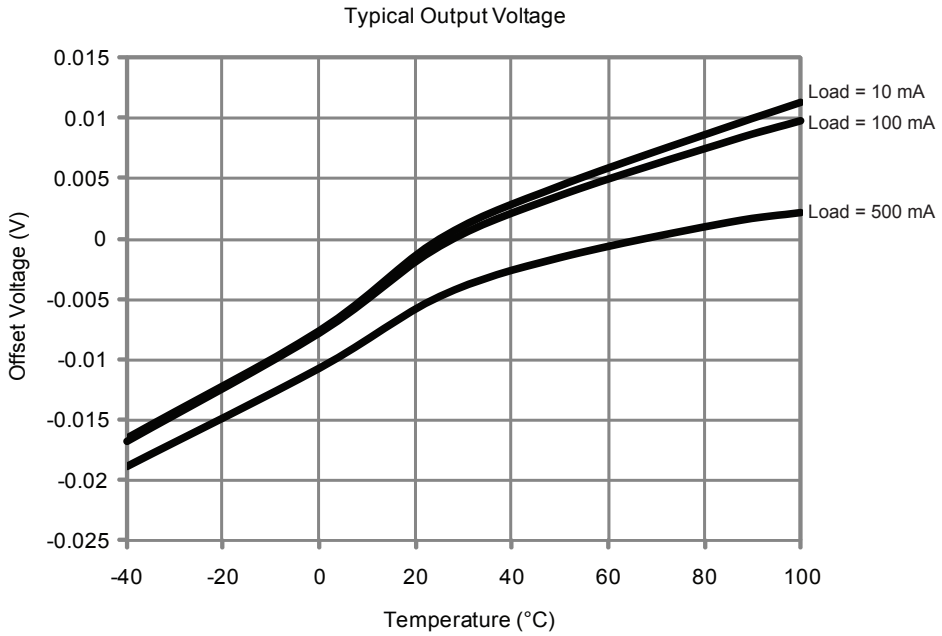


Figure 2-45 • **Typical Output Voltage**

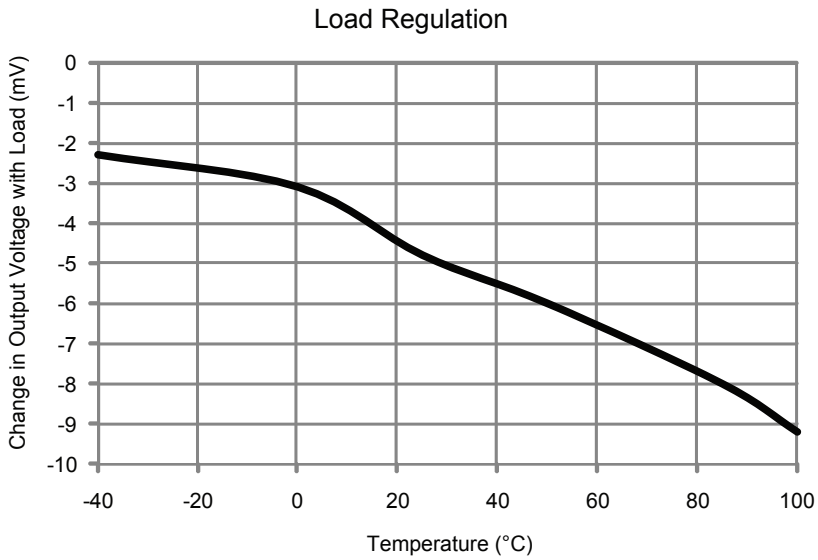


Figure 2-46 • **Load Regulation**

Serial Peripheral Interface (SPI) Characteristics

This section describes the DC and switching of the SPI interface. Unless otherwise noted, all output characteristics given for a 35 pF load on the pins and all sequential timing characteristics are related to SPI_x_CLK. For timing parameter definitions, refer to Figure 2-47 on page 2-90.

***Table 2-100* • SPI Characteristics**
Commercial Case Conditions: T_J = 85ºC, VDD = 1.425 V, –1 Speed Grade

Symbol	Description and Condition	A2F060	A2F200	A2F500	Unit
sp1	SPI_x_CLK minimum period				
	SPI_x_CLK = PCLK/2	20	NA	20	ns
	SPI_x_CLK = PCLK/4	40	40	40	ns
	SPI_x_CLK = PCLK/8	80	80	80	ns
	SPI_x_CLK = PCLK/16	0.16	0.16	0.16	µs
	SPI_x_CLK = PCLK/32	0.32	0.32	0.32	µs
	SPI_x_CLK = PCLK/64	0.64	0.64	0.64	µs
	SPI_x_CLK = PCLK/128	1.28	1.28	1.28	µs
	SPI_x_CLK = PCLK/256	2.56	2.56	2.56	µs
sp2	SPI_x_CLK minimum pulse width high				
	SPI_x_CLK = PCLK/2	10	NA	10	ns
	SPI_x_CLK = PCLK/4	20	20	20	ns
	SPI_x_CLK = PCLK/8	40	40	40	ns
	SPI_x_CLK = PCLK/16	0.08	0.08	0.08	µs
	SPI_x_CLK = PCLK/32	0.16	0.16	0.16	µs
	SPI_x_CLK = PCLK/64	0.32	0.32	0.32	µs
	SPI_x_CLK = PCLK/128	0.64	0.64	0.64	µs
	SPI_x_CLK = PCLK/256	1.28	1.28	1.28	us
sp3	SPI_x_CLK minimum pulse width low				
	SPI_x_CLK = PCLK/2	10	NA	10	ns
	SPI_x_CLK = PCLK/4	20	20	20	ns
	SPI_x_CLK = PCLK/8	40	40	40	ns
	SPI_x_CLK = PCLK/16	0.08	0.08	0.08	µs
	SPI_x_CLK = PCLK/32	0.16	0.16	0.16	µs
	SPI_x_CLK = PCLK/64	0.32	0.32	0.32	µs
	SPI_x_CLK = PCLK/128	0.64	0.64	0.64	µs
	SPI_x_CLK = PCLK/256	1.28	1.28	1.28	µs
sp4	SPI_x_CLK, SPI_x_DO, SPI_x_SS rise time (10%-90%) [1]	4.7	4.7	4.7	ns
sp5	SPI_x_CLK, SPI_x_DO, SPI_x_SS fall time (10%-90%) [1]	3.4	3.4	3.4	ns

Notes:

1. *These values are provided for a load of 35 pF. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website: http://www.microsemi.com/index.php?option=com_microsemi&Itemid=489&lang=en&view=salescontact.*
2. *For allowable pclk configurations, refer to the Serial Peripheral Interface Controller section in the SmartFusion Microcontroller Subsystem User's Guide.*

Table 2-100 • SPI Characteristics
Commercial Case Conditions: T_J = 85ºC, VDD = 1.425 V, –1 Speed Grade (continued)

Symbol	Description and Condition	A2F060	A2F200	A2F500	Unit
sp6	Data from master (SPI_x_DO) setup time [2]	1	1	1	pclk cycles
sp7	Data from master (SPI_x_DO) hold time [2]	1	1	1	pclk cycles
sp8	SPI_x_DI setup time [2]	1	1	1	pclk cycles
sp9	SPI_x_DI hold time [2]	1	1	1	pclk cycles

Notes:

1. *These values are provided for a load of 35 pF. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website: http://www.microsemi.com/index.php?option=com_microsemi&Itemid=489&lang=en&view=salescontact.*
2. *For allowable pclk configurations, refer to the Serial Peripheral Interface Controller section in the SmartFusion Microcontroller Subsystem User's Guide.*

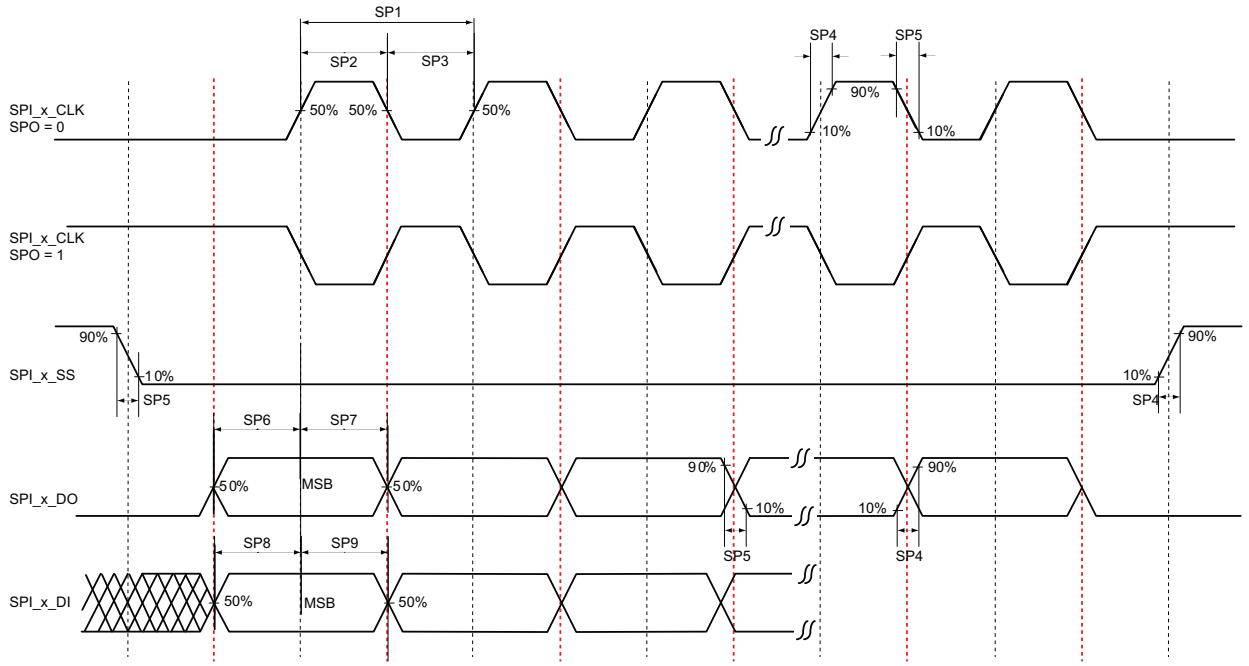
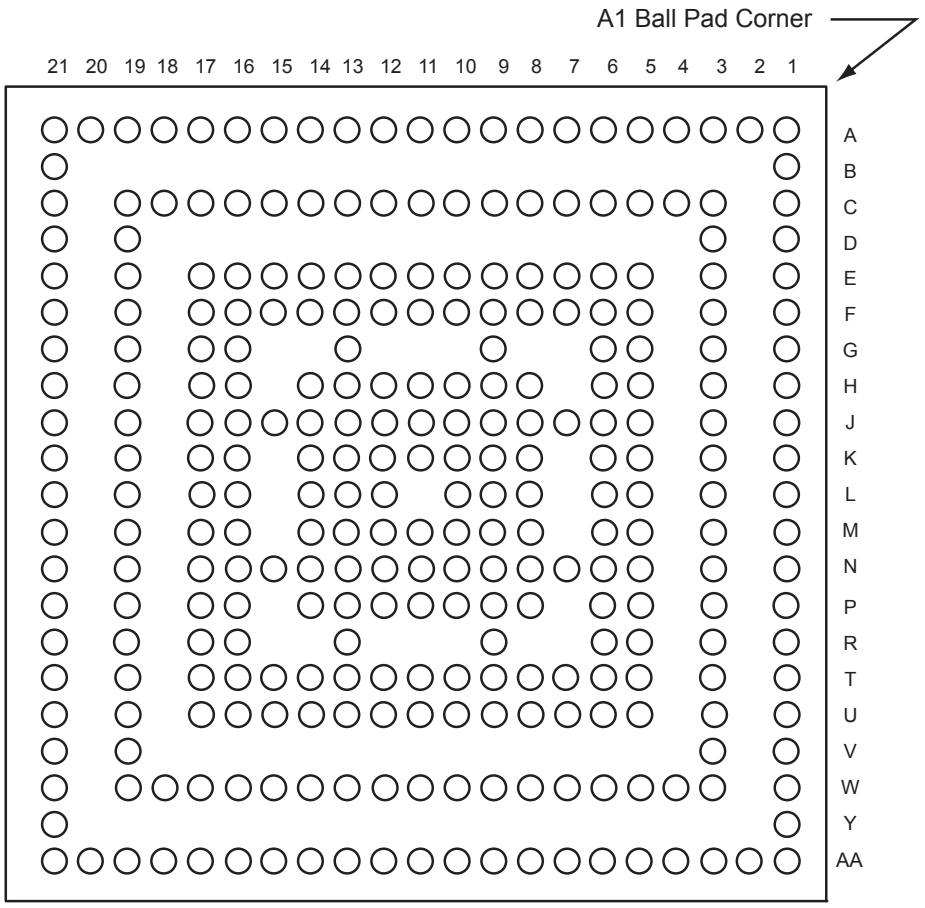


Figure 2-47 • SPI Timing for a Single Frame Transfer in Motorola Mode (SPH = 1)

CS288



Note: Bottom view

Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx.

Pin Number	PQ208	
	A2F200	A2F500
94	ABPS5	ABPS5
95	ABPS4	ABPS4
96	GNDAQ	GNDAQ
97	GNDA	GNDA
98	NC	NC
99	GNDVAREF	GNDVAREF
100	VAREFOUT	VAREFOUT
101	PU_N	PU_N
102	VCC33A	VCC33A
103	PTEM	PTEM
104	PTBASE	PTBASE
105	SPI_0_DO/GPIO_16	SPI_0_DO/GPIO_16
106	SPI_0_DI/GPIO_17	SPI_0_DI/GPIO_17
107	SPI_0_CLK/GPIO_18	SPI_0_CLK/GPIO_18
108	SPI_0_SS/GPIO_19	SPI_0_SS/GPIO_19
109	UART_0_RXD/GPIO_21	UART_0_RXD/GPIO_21
110	UART_0_TXD/GPIO_20	UART_0_TXD/GPIO_20
111	UART_1_RXD/GPIO_29	UART_1_RXD/GPIO_29
112	UART_1_TXD/GPIO_28	UART_1_TXD/GPIO_28
113	VCC	VCC
114	VCCMSSIOB2	VCCMSSIOB2
115	GND	GND
116	I2C_1_SDA/GPIO_30	I2C_1_SDA/GPIO_30
117	I2C_1_SCL/GPIO_31	I2C_1_SCL/GPIO_31
118	I2C_0_SDA/GPIO_22	I2C_0_SDA/GPIO_22
119	I2C_0_SCL/GPIO_23	I2C_0_SCL/GPIO_23
120	GNDENVM	GNDENVM
121	VCCENVM	VCCENVM
122	JTAGSEL	JTAGSEL
123	TCK	TCK
124	TDI	TDI

Notes:

1. *Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.*
2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*

Pin Number	PQ208	
	A2F200	A2F500
187	VCCFPGAIOB0	VCCFPGAIOB0
188	GND	GND
189	VCC	VCC
190	EMC_AB[5]/IO06PDB0V0	IO08PDB0V0
191	EMC_AB[4]/IO06NDB0V0	IO08NDB0V0
192	EMC_AB[3]/IO05PDB0V0	GAC1/IO07PDB0V0
193	EMC_AB[2]/IO05NDB0V0	GAC0/IO07NDB0V0
194	EMC_AB[1]/IO04PDB0V0	IO04PDB0V0
195	EMC_AB[0]/IO04NDB0V0	IO04NDB0V0
196	EMC_OEN1_N/IO03PDB0V0	IO03PDB0V0
197	EMC_OEN0_N/IO03NDB0V0	IO03NDB0V0
198	EMC_BYTEN[1]/GAC1/IO02PDB0V0	GAA1/IO02PDB0V0
199	EMC_BYTEN[0]/GAC0/IO02NDB0V0	GAA0/IO02NDB0V0
200	VCCFPGAIOB0	VCCFPGAIOB0
201	GND	GND
202	VCC	VCC
203	EMC_CS1_N/GAB1/IO01PDB0V0	IO01PDB0V0
204	EMC_CS0_N/GAB0/IO01NDB0V0	IO01NDB0V0
205	EMC_RW_N/GAA1/IO00PDB0V0	IO00PDB0V0
206	EMC_CLK/GAA0/IO00NDB0V0	IO00NDB0V0
207	VCCFPGAIOB0	VCCFPGAIOB0
208	GNDQ	GNDQ

Notes:

1. *Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.*
2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*

Pin Number	FG484	
	A2F200 Function	A2F500 Function
J19	GCA0/IO28NDB1V0	GCA0/IO36NDB1V0 *
J20	GCA1/IO28PDB1V0	GCA1/IO36PDB1V0 *
J21	GCC1/IO26PPB1V0	GCC1/IO35PPB1V0
J22	GCB1/IO27PDB1V0	GCB1/IO34PDB1V0
K1	GND	GND
K2	EMC_DB[0]/GEA2/IO59NDB5V0	EMC_DB[0]/GEA2/IO76NDB5V0
K3	EMC_DB[1]/GEB2/IO59PDB5V0	EMC_DB[1]/GEB2/IO76PDB5V0
K4	NC	IO74PPB5V0
K5	EMC_DB[2]/IO60NPB5V0	EMC_DB[2]/IO77NPB5V0
K6	NC	IO75PDB5V0
K7	GND	GND
K8	VCC	VCC
K9	GND	GND
K10	VCC	VCC
K11	GND	GND
K12	VCC	VCC
K13	GND	GND
K14	VCC	VCC
K15	GND	GND
K16	VCCFPGAIOB1	VCCFPGAIOB1
K17	NC	IO37NDB1V0
K18	GDA1/IO31PDB1V0	GDA1/IO40PDB1V0
K19	GDA0/IO31NDB1V0	GDA0/IO40NDB1V0
K20	GDC1/IO29PDB1V0	GDC1/IO38PDB1V0
K21	GDC0/IO29NDB1V0	GDC0/IO38NDB1V0
K22	GND	GND
L1	NC	IO73PDB5V0
L2	NC	IO73NDB5V0
L3	NC	IO72PPB5V0
L4	GND	GND
L5	NC	IO74NPB5V0
L6	NC	IO75NDB5V0
L7	VCCFPGAIOB5	VCCFPGAIOB5
L8	GND	GND

Notes:

1. *Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.*
2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*

Revision	Changes	Page
Revision 6 (continued)	Dynamic power values were updated in the following tables. The table subtitles changed where FPGA I/O banks were involved to note "I/O assigned to EMC I/O pins" (SAR 30987). Table 2-10 • Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings Table 2-13 • Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings.	2-10 2-11
	The "Timing Model" was updated (SAR 30986).	2-19
	Values in the timing tables for the following sections were updated. Table subtitles were updated for FPGA I/O banks to note "I/O assigned to EMC I/O pins" (SAR 30986). "Overview of I/O Performance" section: Table 2-24, Table 2-25 "Detailed I/O DC Characteristics" section: Table 2-38, Table 2-39, Table 2-40, Table 2-44, Table 2-45, Table 2-46, Table 2-50, Table 2-51, Table 2-52, Table 2-56, Table 2-57, Table 2-58, Table 2-61, Table 2-62 "LVDS" section: Table 2-65 "LVPECL" section: Table 2-68 "Global Tree Timing Characteristics" section: Table 2-80, Table 2-81	2-23 2-26 2-40 2-42 2-59
	The "PQ208" section and pin tables are new (SAR 31005).	5-34
	Global clocks were removed from the A2F060 pin table for the "CS288" and "FG256" packages, resulting in changed function names for affected pins (SAR 31033).	5-43
Revision 5 (December 2010)	Table 2-2 • Analog Maximum Ratings was revised. The recommended CM[n] pad voltage (relative to ground) was changed from –11 to –0.3 (SAR 28219).	2-2
	Table 2-7 • Temperature and Voltage Derating Factors for Timing Delays was revised to change the values for 100ºC.	2-9
	Power-down and Sleep modes, and all associated notes, were removed from Table 2-8 • Power Supplies Configuration (SAR 29479). IDC3 and IDC4 were renamed to IDC1 and IDC2 (SAR 29478). These modes are no longer supported. A note was added to the table stating that current monitors and temperature monitors should not be used when Power-down and/or Sleep mode are required by the application.	2-10
	The "Power-Down and Sleep Mode Implementation" section was deleted (SAR 29479).	N/A
	Values for PAC9 and PAC10 for LVDS and LVPECL were revised in Table 2-10 • Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings and Table 2-12 • Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings*.	2-10, 2-11
	Values for PAC1 through PAC4, PDC1, and PDC2 were added for A2F500 in Table 2-14 • Different Components Contributing to Dynamic Power Consumption in SmartFusion cSoCs and Table 2-15 • Different Components Contributing to the Static Power Consumption in SmartFusion cSoCs	2-12, 2-13
	The equation for "Total Dynamic Power Consumption—P_{DYN}" in "SoC Mode" was revised to add P_{MSS}. The "Microcontroller Subsystem Dynamic Contribution—P_{MSS}" section is new (SAR 29462).	2-14, 2-18
	Information in Table 2-24 • Summary of I/O Timing Characteristics—Software Default Settings (applicable to FPGA I/O banks) and Table 2-25 • Summary of I/O Timing Characteristics—Software Default Settings (applicable to MSS I/O banks) was updated.	2-25