Microsemi Corporation - A2F060M3E-1TQG144 Datasheet

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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details	
Product Status	Obsolete
Architecture	MCU, FPGA
Core Processor	ARM® Cortex®-M3
Flash Size	128KB
RAM Size	16KB
Peripherals	DMA, POR, WDT
Connectivity	EBI/EMI, I²C, SPI, UART/USART
Speed	100MHz
Primary Attributes	ProASIC®3 FPGA, 60K Gates, 1536D-Flip-Flops
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	144-LQFP
Supplier Device Package	144-TQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/a2f060m3e-1tqg144

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Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

SmartFusion cSoC Family Product Table

	A2F060			A2F200				A2F500			
FPGA Fabric	TQ144	CS288	FG256	PQ208	CS288	FG256	FG484	PQ208	CS288	FG256	FG484
System Gates	60,000			200,000				500,000			
Tiles (D-flip-flops)	1,536			4,608				11,520			
RAM Blocks (4,608 bits)	8			8				24			

	A2F060			A2F200				A2F500			
Microcontroller Subsystem (MSS)	TQ144	CS288	FG256	PQ208	CS288	FG256	FG484	PQ208	CS288	FG256	FG484
Flash (Kbytes)	128			256				512			
SRAM (Kbytes)	16			64				64			
Cortex-M3 processor with MPU	Yes			Yes				Yes			
10/100 Ethernet MAC	No			Yes				Yes			
External Memory Controller (EMC)	–	26-/16-bit address/data		26-bit address,16-bit data				–	26-/16-bit address/data		
DMA	8 Ch			8 Ch				8 Ch			
I^2C	2			2				2			
SPI	1	2		1	2			1	2		
16550 UART	2			2				2			
32-Bit Timer	2			2				2			
PLL	1			1				1	2	1	2
32 KHz Low Power Oscillator	1			1				1			
100 MHz On-Chip RC Oscillator	1			1				1			
Main Oscillator (32 KHz to 20 MHz)	1			1				1			

	A2F060			A2F200				A2F500			
Programmable Analog	TQ144	CS288	FG256	PQ208	CS288	FG256	FG484	PQ208	CS288	FG256	FG484
ADCs (8-/10-/12-bit SAR)	1			2				2			3
DACs (8-/16-/24-bit sigma-delta)	1			2				2			3
Signal Conditioning Blocks (SCBs)	1			4				4			5
Comparator*	2			8				8			10
Current Monitors*	1			4				4			5
Temperature Monitors*	1			4				4			5
Bipolar High Voltage Monitors*	2			8				8			10

Note: *These functions share I/O pins and may not all be available at the same time. See the "Analog Front-End Overview" section in the http://www.microsemi.com/index.php?option=com_docman&task=doc_download&gid=130925 for details.*

This enables reduction or complete removal of expensive voltage monitor and brownout detection devices from the PCB design. Flash-based SmartFusion cSoCs simplify total system design and reduce cost and design risk, while increasing system reliability.

Immunity to Firm Errors

Firm errors occur most commonly when high-energy neutrons, generated in the atmosphere, strike a configuration cell of an SRAM FPGA. The energy of the collision can change the state of the configuration cell and thus change the logic, routing, or I/O configuration behavior in an unpredictable way.

Another source of radiation-induced firm errors is alpha particles. For alpha radiation to cause a soft or firm error, its source must be in very close proximity to the affected circuit. The alpha source must be in the package molding compound or in the die itself. While low-alpha molding compounds are being used increasingly, this helps reduce but does not entirely eliminate alpha-induced firm errors.

Firm errors are impossible to prevent in SRAM FPGAs. The consequence of this type of error can be a complete system failure. Firm errors do not occur in SmartFusion cSoCs. Once it is programmed, the flash cell configuration element of SmartFusion cSoCs cannot be altered by high energy neutrons and is therefore immune to errors from them. Recoverable (or soft) errors occur in the user data SRAMs of all FPGA devices. These can easily be mitigated by using error detection and correction (EDAC) circuitry built into the FPGA fabric.

Specifying I/O States During Programming

You can modify the I/O states during programming in FlashPro. In FlashPro, this feature is supported for PDB files generated from Designer v8.5 or greater. See the *FlashPro User's Guide* for more information.

Note: PDB files generated from Designer v8.1 to Designer v8.4 (including all service packs) have limited display of Pin Numbers only.

The I/Os are controlled by the JTAG Boundary Scan register during programming, except for the analog pins (AC, AT and AV). The Boundary Scan register of the AG pin can be used to enable/disable the gate driver in software v9.0.

1. Load a PDB from the FlashPro GUI. You must have a PDB loaded to modify the I/O states during programming.
2. From the FlashPro GUI, click PDB Configuration. A FlashPoint – Programming File Generator window appears.
3. Click the Specify I/O States During Programming button to display the Specify I/O States During Programming dialog box.
4. Sort the pins as desired by clicking any of the column headers to sort the entries by that header. Select the I/Os you wish to modify (Figure 1-1 on page 1-4).
5. Set the I/O Output State. You can set Basic I/O settings if you want to use the default I/O settings for your pins, or use Custom I/O settings to customize the settings for each pin. Basic I/O state settings:

   1 – I/O is set to drive out logic High

   0 – I/O is set to drive out logic Low

   Last Known State – I/O is set to the last value that was driven out prior to entering the programming mode, and then held at that value during programming

   Z -Tri-State: I/O is tristated

Overview of I/O Performance

Summary of I/O DC Input and Output Levels – Default I/O Software Settings

Table 2-19 • **Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial Conditions—Software Default Settings Applicable to FPGA I/O Banks**

			VIL		VIH		VOL	VOH	I_{OL}[1]	I_{OH}[1]
I/O Standard	**Drive Strgth.**	**Slew Rate**	**Min. V**	**Max. V**	**Min. V**	**Max. V**	**Max. V**	**Min. V**	**mA**	**mA**
3.3 V LVTTL / 3.3 V LVCMOS	12 mA	High	–0.3	0.8	2	3.6	0.4	2.4	12	12
2.5 V LVCMOS	12 mA	High	–0.3	0.7	1.7	3.6	0.7	1.7	12	12
1.8 V LVCMOS	12 mA	High	–0.3	0.35 * VCCxxxxIOBx	0.65* VCCxxxxIOBx	3.6	0.45	VCCxxxxIOBx – 0.45	12	12
1.5 V LVCMOS	12 mA	High	–0.3	0.35 * VCCxxxxIOBx	0.65* VCCxxxxIOBx	3.6	0.25 * VCCxxxxIOBx	0.75* VCCxxxxIOBx	12	12
3.3 V PCI	Per PCI specifications									
3.3 V PCI-X	Per PCI-X specifications									

Notes:

1. *Currents are measured at 85°C junction temperature.*
2. *Output slew rate can be extracted by the IBIS Models.*

Table 2-20 • **Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial Conditions—Software Default Settings Applicable to MSS I/O Banks**

			VIL		VIH		VOL	VOH	I_{OL}[1]	I_{OH}[1]
I/O Standard	**Drive Strgth.**	**Slew Rate**	**Min. V**	**Max. V**	**Min. V**	**Max. V**	**Max. V**	**Min. V**	**mA**	**mA**
3.3 V LVTTL / 3.3 V LVCMOS	8 mA	High	–0.3	0.8	2	3.6	0.4	2.4	8	8
2.5 V LVCMOS	8 mA	High	–0.3	0.7	1.7	3.6	0.7	1.7	8	8
1.8 V LVCMOS	4 mA	High	–0.3	0.35* VCCxxxxIOBx	0.65* VCCxxxxIOBx	3.6	0.45	VCCxxxxIOBx – 0.45	4	4
1.5 V LVCMOS	2 mA	High	–0.3	0.35* VCCxxxxIOBx	0.65* VCCxxxxIOBx	3.6	0.25* VCCxxxxIOBx	0.75* VCCxxxxIOBx	2	2

Notes:

1. *Currents are measured at 85°C junction temperature.*
2. *Output slew rate can be extracted by the IBIS Models.*

2.5 V LVCMOS

Low-Voltage CMOS for 2.5 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 2.5 V applications.

Table 2-41 • Minimum and Maximum DC Input and Output Levels Applicable to FPGA I/O Banks

2.5 V LVCMOS	VIL		VIH		VOL	VOH	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[1]	Max. mA[1]	μA[2]	μA[2]
2 mA	–0.3	0.7	1.7	2.7	0.7	1.7	2	2	18	16	15	15
4 mA	–0.3	0.7	1.7	2.7	0.7	1.7	4	4	18	16	15	15
6 mA	–0.3	0.7	1.7	2.7	0.7	1.7	6	6	37	32	15	15
8 mA	–0.3	0.7	1.7	2.7	0.7	1.7	8	8	37	32	15	15
12 mA	–0.3	0.7	1.7	2.7	0.7	1.7	12	12	74	65	15	15
16 mA	–0.3	0.7	1.7	2.7	0.7	1.7	16	16	87	83	15	15
24 mA	–0.3	0.7	1.7	2.7	0.7	1.7	24	24	124	169	15	15

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*
3. *Software default selection highlighted in gray.*

Table 2-42 • Minimum and Maximum DC Input and Output Levels Applicable to MSS I/O Banks

2.5 V LVCMOS	VIL		V_{IH}		VOL	VOH	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[1]	Max., mA[1]	μA[2]	μA[2]
8 mA	–0.3	0.7	1.7	3.6	0.7	1.7	8	8	37	32	15	15

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*
3. *Software default selection highlighted in gray.*

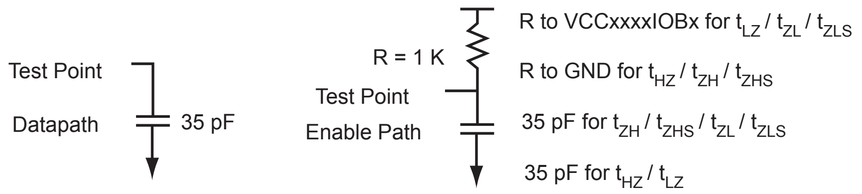

Figure 2-7 • **AC Loading**

Table 2-43 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	V_{REF} (typ.) (V)	C_{LOAD} (pF)
0	2.5	1.2	–	35

* *Measuring point = $V_{trip.}$ See Table 2-22 on page 2-24 for a complete table of trip points.*

Timing Characteristics

Table 2-44 • 2.5 V LVCMOS High Slew
Worst Commercial-Case Conditions: T_J = 85°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCxxxxIOBx = 2.3 V
Applicable to FPGA I/O Banks, I/O Assigned to EMC I/O Pins

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.55	8.10	0.04	1.23	0.39	7.37	8.10	2.54	2.17	9.43	10.15	ns
	–1	0.46	6.75	0.03	1.03	0.32	6.14	6.75	2.12	1.81	7.85	8.46	ns
8 mA	Std.	0.55	4.85	0.04	1.23	0.39	4.76	4.85	2.90	2.83	6.82	6.91	ns
	–1	0.46	4.04	0.03	1.03	0.32	3.97	4.04	2.42	2.36	5.68	5.76	ns
12 mA	Std.	0.60	3.28	0.04	1.23	0.39	3.46	3.23	3.15	3.24	5.52	5.29	ns
	–1	0.50	2.73	0.03	1.03	0.32	2.88	2.69	2.62	2.70	4.60	4.41	ns
16 mA	Std.	0.60	3.09	0.04	1.23	0.39	3.27	2.88	3.20	3.35	5.33	4.94	ns
	–1	0.50	2.57	0.03	1.03	0.32	2.72	2.40	2.67	2.79	4.44	4.12	ns
24 mA	Std.	0.60	2.95	0.04	1.23	0.39	3.01	2.31	3.27	3.76	5.07	4.37	ns
	–1	0.50	2.46	0.03	1.03	0.32	2.51	1.93	2.73	3.13	4.22	3.64	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.*

Table 2-45 • 2.5 V LVCMOS Low Slew
Worst Commercial-Case Conditions: T_J = 85°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCxxxxIOBx = 2.3 V
Applicable to FPGA I/O Banks, I/O Assigned to EMC I/O Pins

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.55	10.50	0.04	1.23	0.39	10.69	10.50	2.54	2.07	12.75	12.56	ns
	–1	0.46	8.75	0.03	1.03	0.32	8.91	8.75	2.12	1.73	10.62	10.47	ns
8 mA	Std.	0.55	7.61	0.04	1.23	0.39	7.46	7.19	2.81	2.66	9.52	9.25	ns
	–1	0.46	6.34	0.03	1.03	0.32	6.22	5.99	2.34	2.22	7.93	7.71	ns
12 mA	Std.	0.60	5.92	0.04	1.23	0.39	5.79	5.45	3.04	3.06	7.85	7.51	ns
	–1	0.50	4.93	0.03	1.03	0.32	4.83	4.54	2.53	2.55	6.54	6.26	ns
16 mA	Std.	0.60	5.53	0.04	1.23	0.39	5.40	5.09	3.09	3.16	7.46	7.14	ns
	–1	0.50	4.61	0.03	1.03	0.32	4.50	4.24	2.58	2.64	6.22	5.95	ns
24 mA	Std.	0.60	5.18	0.04	1.23	0.39	5.28	5.14	3.27	3.64	7.34	7.20	ns
	–1	0.50	4.32	0.03	1.03	0.32	4.40	4.29	2.72	3.03	6.11	6.00	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.

Table 2-46 • 2.5 V LVCMOS High Slew
Worst Commercial-Case Conditions: T_J = 85°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCxxxxIOBx = 3.0 V
Applicable to MSS I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
8 mA	Std.	0.22	2.35	0.09	1.18	1.39	0.22	2.40	2.18	2.19	2.32	ns
	–1	0.18	1.96	0.07	0.99	1.16	0.18	2.00	1.82	1.82	1.93	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.*

Input Register

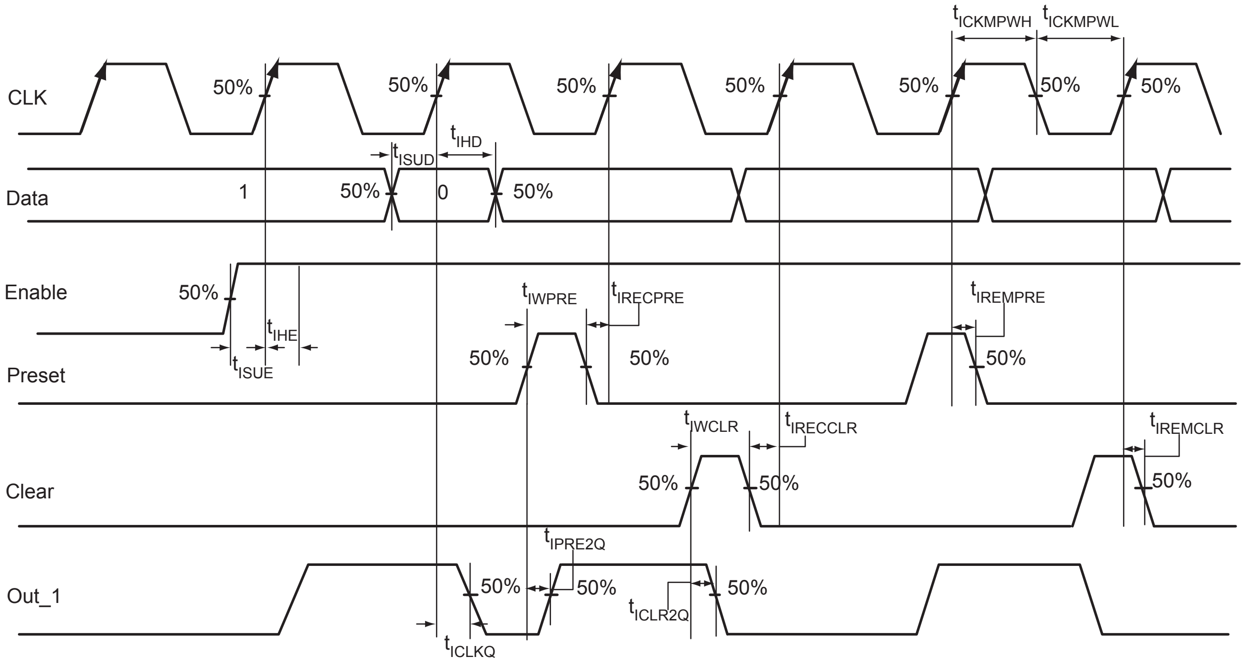

***Figure 2-16* • Input Register Timing Diagram**

Timing Characteristics

***Table 2-71* • Input Data Register Propagation Delays**
Worst Commercial-Case Conditions: T_J = 85°C, Worst-Case VCC = 1.425 V

Parameter	Description	–1	Std.	Units
t_{ICLKQ}	Clock-to-Q of the Input Data Register	0.24	0.29	ns
t_{ISUD}	Data Setup Time for the Input Data Register	0.27	0.32	ns
t_{IHD}	Data Hold Time for the Input Data Register	0.00	0.00	ns
t_{ISUE}	Enable Setup Time for the Input Data Register	0.38	0.45	ns
t_{IHE}	Enable Hold Time for the Input Data Register	0.00	0.00	ns
t_{ICLR2Q}	Asynchronous Clear-to-Q of the Input Data Register	0.46	0.55	ns
t_{IPRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	0.46	0.55	ns
$t_{IREMCLR}$	Asynchronous Clear Removal Time for the Input Data Register	0.00	0.00	ns
$t_{IRECCLR}$	Asynchronous Clear Recovery Time for the Input Data Register	0.23	0.27	ns
$t_{IREMPRE}$	Asynchronous Preset Removal Time for the Input Data Register	0.00	0.00	ns
$t_{IRECPRE}$	Asynchronous Preset Recovery Time for the Input Data Register	0.23	0.27	ns
t_{IWCLR}	Asynchronous Clear Minimum Pulse Width for the Input Data Register	0.22	0.22	ns
t_{IWPRE}	Asynchronous Preset Minimum Pulse Width for the Input Data Register	0.22	0.22	ns
$t_{ICKMPWH}$	Clock Minimum Pulse Width High for the Input Data Register	0.36	0.36	ns
$t_{ICKMPWL}$	Clock Minimum Pulse Width Low for the Input Data Register	0.32	0.32	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.

Clock Conditioning Circuits

CCC Electrical Specifications

Timing Characteristics

Table 2-86 **• SmartFusion CCC/PLL Specification**

Parameter	Minimum	Typical	Maximum	Units
Clock Conditioning Circuitry Input Frequency f_{IN_CCC}	1.5		350	MHz
Clock Conditioning Circuitry Output Frequency f_{OUT_CCC}	0.75		350[1]	MHz
Delay Increments in Programmable Delay Blocks[2,3,4]		160		ps
Number of Programmable Values in Each Programmable Delay Block			32	
Input Period Jitter			1.5	ns
Acquisition Time				
LockControl = 0			300	µs
LockControl = 1			6.0	ms
Tracking Jitter[5]				
LockControl = 0			1.6	ns
LockControl = 1			0.8	ns
Output Duty Cycle	48.5		5.15	%
Delay Range in Block: Programmable Delay 1[2,3]	0.6		5.56	ns
Delay Range in Block: Programmable Delay 2[2,3]	0.025		5.56	ns
Delay Range in Block: Fixed Delay[2,3]		2.2		ns

CCC Output Peak-to-Peak Period Jitter F_{CCC_OUT} [6,7]	Maximum Peak-to-Peak Period Jitter							
	SSO $\leq$ 2		**SSO $\leq$ 4**		**SSO $\leq$ 8**		**SSO $\leq$ 16**	
	FG/CS	**PQ**	**FG/CS**	**PQ**	**FG/CS**	**PQ**	**FG/CS**	**PQ**
0.75 MHz to 50 MHz	0.5%	1.6%	0.9%	1.6%	0.9%	1.6%	0.9%	1.8%
50 MHz to 250 MHz	1.75%	3.5%	9.3%	9.3%	9.3%	17.9%	10.0%	17.9%
250 MHz to 350 MHz	2.5%	5.2%	13.0%	13.0%	13.0%	25.0%	14.0%	25.0%

Notes:

1. *One of the CCC outputs (GLA0) is used as an MSS clock and is limited to 100 MHz (maximum) by software. Details regarding CCC/PLL are in the "PLLs, Clock Conditioning Circuitry, and On-Chip Crystal Oscillators" chapter of the SmartFusion Microcontroller Subsystem User's Guide.*
2. *This delay is a function of voltage and temperature. See Table 2-7 on page 2-9 for deratings.*
3. *T_J = 25°C, VCC = 1.5 V*
4. *When the CCC/PLL core is generated by Microsemi core generator software, not all delay values of the specified delay increments are available. Refer to the Libero SoC Online Help associated with the core for more information.*
5. *Tracking jitter is defined as the variation in clock edge position of PLL outputs with reference to the PLL input clock edge. Tracking jitter does not measure the variation in PLL output period, which is covered by the period jitter parameter.*
6. *Measurement done with LVTTL 3.3 V 12 mA I/O drive strength and High slew rate. VCC/VCCPLL = 1.425 V, VCCI = 3.3V, 20 pF output load. All I/Os are placed outside of the PLL bank.*
7. *SSOs are outputs that are synchronous to a single clock domain and have their clock-to-out within ± 200 ps of each other.*
8. *VCO output jitter is calculated as a percentage of the VCO frequency. The jitter (in ps) can be calculated by multiplying the VCO period by the % jitter. The VCO jitter (in ps) applies to CCC_OUT regardless of the output divider settings. For example, if the jitter on VCO is 300 ps, the jitter on CCC_OUT is also 300 ps.*

Programmable Analog Specifications

Current Monitor

Unless otherwise noted, current monitor performance is specified at 25°C with nominal power supply voltages, with the output measured using the internal voltage reference with the internal ADC in 12-bit mode and 91 Ksps, after digital compensation. All results are based on averaging over 16 samples.

***Table 2-93* • Current Monitor Performance Specification**

Specification	Test Conditions	Min.	Typical	Max.	Units
Input voltage range (for driving ADC over full range)		0 – 48	0 – 50	1 – 51	mV
Analog gain	From the differential voltage across the input pads to the ADC input		50		V/V
Input referred offset voltage	Input referred offset voltage	0	0.1	0.5	mV
	–40ºC to +100ºC	0	0.1	0.5	mV
Gain error	Slope of BFSL vs. 50 V/V		±0.1	±0.5	% nom.
	–40ºC to +100ºC			±0.5	% nom.
Overall Accuracy	Peak error from ideal transfer function, 25°C		±(0.1 + 0.25%)	±(0.4 + 1.5%)	mV plus % reading
Input referred noise	0 VDC input (no output averaging)	0.3	0.4	0.5	mVrms
Common-mode rejection ratio	0 V to 12 VDC common-mode voltage	–86	–87		dB
Analog settling time	To 0.1% of final value (with ADC load)				
	From CM_STB (High)	5			µs
	From ADC_START (High)	5		200	µs
Input capacitance			8		pF
Input biased current	CM[n] or TM[n] pad, –40°C to +100°C over maximum input voltage range (plus is into pad)				
	Strobe = 0; IBIAS on CM[n]		0		µA
	Strobe = 1; IBIAS on CM[n]		1		µA
	Strobe = 0; IBIAS on TM[n]		2		µA
	Strobe = 1; IBIAS on TM[n]		1		µA
Power supply rejection ratio	DC (0 – 10 KHz)	41	42		dB
Incremental operational current monitor power supply current requirements (per current monitor instance, not including ADC or VAREFx)	VCC33A		150		µA
	VCC33AP		140		µA
	VCC15A		50		µA

Note: Under no condition should the TM pad ever be greater than 10 mV above the CM pad. This restriction is applicable only if current monitor is used.

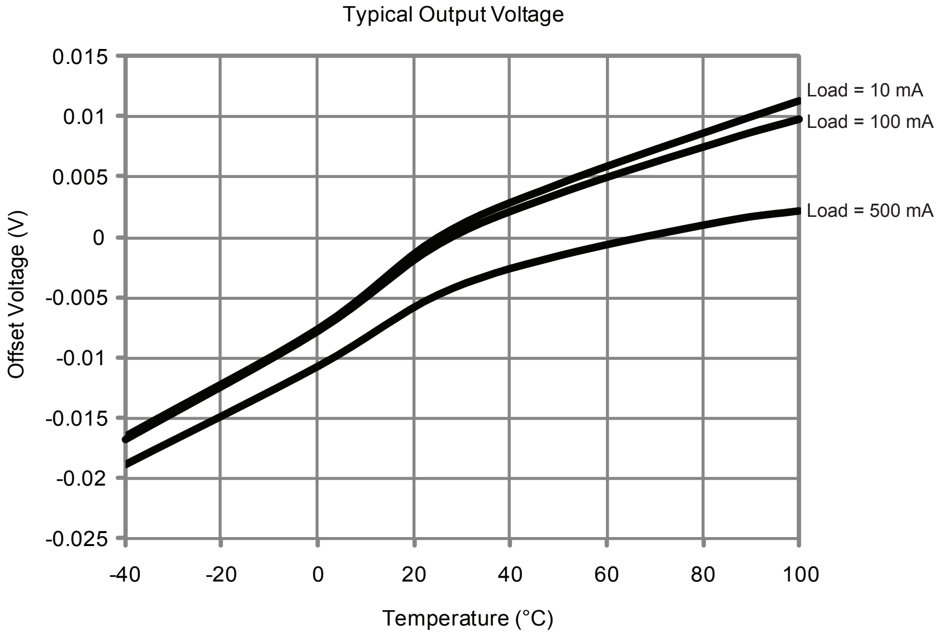

***Figure 2-45* • Typical Output Voltage**

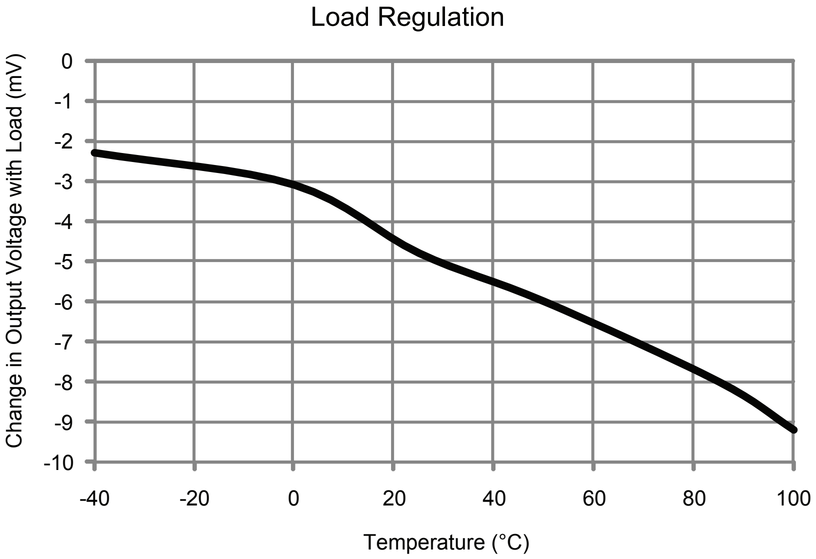

***Figure 2-46* • Load Regulation**

User-Defined Supply Pins

Name	Type	Polarity/ Bus Size	Description
VAREF0	Input	1	Analog reference voltage for first ADC. The SmartFusion cSoC can be configured to generate a 2.56 V internal reference that can be used by the ADC. While using the internal reference, the reference voltage is output on the VAREFOUT pin for use as a system reference. If a different reference voltage is required, it can be supplied by an external source and applied to this pin. The valid range of values that can be supplied to the ADC is 1.0 V to 3.3 V. When VAREF0 is internally generated, a bypass capacitor must be connected from this pin to ground. The value of the bypass capacitor should be between 3.3 µF and 22 µF, which is based on the needs of the individual designs. The choice of the capacitor value has an impact on the settling time it takes the VAREF0 signal to reach the required specification of 2.56 V to initiate valid conversions by the ADC. If the lower capacitor value is chosen, the settling time required for VAREF0 to achieve 2.56 V will be shorter than when selecting the larger capacitor value. The above range of capacitor values supports the accuracy specification of the ADC, which is detailed in the datasheet. Designers choosing the smaller capacitor value will not obtain as much margin in the accuracy as that achieved with a larger capacitor value. See the Analog-to-Digital Converter (ADC) section in the *SmartFusion Programmable Analog User's Guide* for more information. The SoC Products Group recommends customers use 10 µF as the value of the bypass capacitor. Designers choosing to use an external VAREF0 need to ensure that a stable and clean VAREF0 source is supplied to the VAREF0 pin before initiating conversions by the ADC. To use the internal voltage reference, the VAREFOUT pin must be connected to the appropriate ADC VAREFx input on the PCB. For example, VAREFOUT can be connected to VAREF0 only, if ADC0 alone is used. VAREFOUT can be connected to VAREF1 only, if ADC1 alone is used. VAREFOUT can be connected to VAREF2 only, if ADC2 alone is used. VAREFOUT can be connected to VAREF0, VAREF1 and VAREF2 together, if ADC0, ADC1, and ADC2 all are used.
VAREF1	Input	1	Analog reference voltage for second ADC See "VAREF0" above for more information.
VAREF2	Input	1	Analog reference voltage for third ADC See "VAREF0" above for more.
VAREFOUT	Out	1	Internal 2.56 V voltage reference output. Can be used to provide the two ADCs with a unique voltage reference externally by connecting VAREFOUT to both VAREF0 and VAREF1. To use the internal voltage reference, you must connect the VAREFOUT pin to the appropriate ADC VAREFx input—either the VAREF0 or VAREF1 pin—on the PCB.

Table 5-2 **• Relationships Between Signals in the Analog Front-End**

Pin	ADC Channel	Dir.-In Option	Prescaler	Current Mon.	Temp. Mon.	Compar.	LVTTL	SDD MUX	SDD
SDD2	ADC2_CH15								SDD2_OUT
TM0	ADC0_CH4	Yes		CM0_L	TM0_IO	CMP0_N			
TM1	ADC0_CH8	Yes		CM1_L	TM1_IO	CMP2_N			
TM2	ADC1_CH4	Yes		CM2_L	TM2_IO	CMP4_N			
TM3	ADC1_CH8	Yes		CM3_L	TM3_IO	CMP6_N			
TM4	ADC2_CH4	Yes		CM4_L	TM4_IO	CMP8_N			

Notes:

1. *ABPSx_IN: Input to active bipolar prescaler channel x.*
2. *CMx_H/L: Current monitor channel x, high/low side.*
3. *TMx_IO: Temperature monitor channel x.*
4. *CMPx_P/N: Comparator channel x, positive/negative input.*
5. *LVTTLx_IN: LVTTL I/O channel x.*
6. *SDDMx_OUT: Output from sigma-delta DAC MUX channel x.*
7. *SDDx_OUT: Direct output from sigma-delta DAC channel x.*

Pin Number	PQ208	
	A2F200	**A2F500**
125	TMS	TMS
126	TDO	TDO
127	TRSTB	TRSTB
128	VJTAG	VJTAG
129	VDDBAT	VDDBAT
130	VCCLPXTAL	VCCLPXTAL
131	LPXOUT	LPXOUT
132	LPXIN	LPXIN
133	GNDLPXTAL	GNDLPXTAL
134	GNDMAINXTAL	GNDMAINXTAL
135	MAINXOUT	MAINXOUT
136	MAINXIN	MAINXIN
137	VCCMAINXTAL	VCCMAINXTAL
138	GND	GND
139	VCC	VCC
140	VPP	VPP
141	VCCFPGAIOB1	VCCFPGAIOB1
142	GDA0/IO31NDB1V0	GDA0/IO40NDB1V0
143	GDA1/IO31PDB1V0	GDA1/IO40PDB1V0
144	GDC0/IO29NSB1V0	GDC0/IO38NSB1V0
145	GCA0/IO28NDB1V0	GCA0/IO36NDB1V0 *
146	GCA1/IO28PDB1V0	GCA1/IO36PDB1V0 *
147	VCCFPGAIOB1	VCCFPGAIOB1
148	GND	GND
149	VCC	VCC
150	IO25NDB1V0	IO30NDB1V0
151	GCC2/IO25PDB1V0	GBC2/IO30PDB1V0
152	IO23NDB1V0	IO28NDB1V0
153	GCA2/IO23PDB1V0	GCA2/IO28PDB1V0 *
154	GBC2/IO21PSB1V0	GBB2/IO27NDB1V0
155	GBA2/IO20PSB1V0	GBA2/IO27PDB1V0

Notes:

1. *Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.*
2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*

Pin No.	FG256		
	A2F060 Function	**A2F200 Function**	**A2F500 Function**
A1	GND	GND	GND
A2	VCCFPGAIOB0	VCCFPGAIOB0	VCCFPGAIOB0
A3	EMC_AB[0]/IO04NDB0V0	EMC_AB[0]/IO04NDB0V0	EMC_AB[0]/IO06NDB0V0
A4	EMC_AB[1]/IO04PDB0V0	EMC_AB[1]/IO04PDB0V0	EMC_AB[1]/IO06PDB0V0
A5	GND	GND	GND
A6	EMC_AB[3]/IO05PDB0V0	EMC_AB[3]/IO05PDB0V0	EMC_AB[3]/IO09PDB0V0
A7	EMC_AB[5]/IO06PDB0V0	EMC_AB[5]/IO06PDB0V0	EMC_AB[5]/IO10PDB0V0
A8	VCCFPGAIOB0	VCCFPGAIOB0	VCCFPGAIOB0
A9	GND	GND	GND
A10	EMC_AB[14]/IO11NDB0V0	EMC_AB[14]/IO11NDB0V0	EMC_AB[14]/IO15NDB0V0
A11	EMC_AB[15]/IO11PDB0V0	EMC_AB[15]/IO11PDB0V0	EMC_AB[15]/IO15PDB0V0
A12	GND	GND	GND
A13	EMC_AB[20]/IO14NDB0V0	EMC_AB[20]/IO14NDB0V0	EMC_AB[20]/IO21NDB0V0
A14	EMC_AB[24]/IO16NDB0V0	EMC_AB[24]/IO16NDB0V0	EMC_AB[24]/IO20NDB0V0
A15	VCCFPGAIOB0	VCCFPGAIOB0	VCCFPGAIOB0
A16	GND	GND	GND
B1	EMC_DB[15]/IO45PDB5V0	EMC_DB[15]/GAA2/IO71PDB5V0	EMC_DB[15]/GAA2/IO88PDB5V0
B2	GND	GND	GND
B3	EMC_BYTEN[1]/IO02PDB0V0	EMC_BYTEN[1]/GAC1/IO02PDB0V0	EMC_BYTEN[1]/GAC1/IO07PDB0V0
B4	EMC_OEN0_N/IO03NDB0V0	EMC_OEN0_N/IO03NDB0V0	EMC_OEN0_N/IO08NDB0V0
B5	EMC_OEN1_N/IO03PDB0V0	EMC_OEN1_N/IO03PDB0V0	EMC_OEN1_N/IO08PDB0V0
B6	EMC_AB[2]/IO05NDB0V0	EMC_AB[2]/IO05NDB0V0	EMC_AB[2]/IO09NDB0V0
B7	EMC_AB[4]/IO06NDB0V0	EMC_AB[4]/IO06NDB0V0	EMC_AB[4]/IO10NDB0V0
B8	EMC_AB[9]/IO08PDB0V0	EMC_AB[9]/IO08PDB0V0	EMC_AB[9]/IO13PDB0V0
B9	EMC_AB[12]/IO10NDB0V0	EMC_AB[12]/IO10NDB0V0	EMC_AB[12]/IO14NDB0V0
B10	EMC_AB[13]/IO10PDB0V0	EMC_AB[13]/IO10PDB0V0	EMC_AB[13]/IO14PDB0V0
B11	EMC_AB[16]/IO12NDB0V0	EMC_AB[16]/IO12NDB0V0	EMC_AB[16]/IO17NDB0V0
B12	EMC_AB[18]/IO13NDB0V0	EMC_AB[18]/IO13NDB0V0	EMC_AB[18]/IO18NDB0V0
B13	EMC_AB[21]/IO14PDB0V0	EMC_AB[21]/IO14PDB0V0	EMC_AB[21]/IO21PDB0V0
B14	EMC_AB[25]/IO16PDB0V0	EMC_AB[25]/IO16PDB0V0	EMC_AB[25]/IO20PDB0V0
B15	GND	GND	GND

Notes:

1. *Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.*
2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*

Pin No.	FG256		
	A2F060 Function	**A2F200 Function**	**A2F500 Function**
D15	GCA1/IO20PDB0V0	IO24NDB1V0	IO33NDB1V0
D16	VCCFPGAIOB1	VCCFPGAIOB1	VCCFPGAIOB1
E1	EMC_DB[13]/IO44PDB5V0	EMC_DB[13]/GAC2/IO70PDB5V0	EMC_DB[13]/GAC2/IO87PDB5V0
E2	EMC_DB[12]/IO44NDB5V0	EMC_DB[12]/IO70NDB5V0	EMC_DB[12]/IO87NDB5V0
E3	GFA2/IO42PDB5V0	GFA2/IO68PDB5V0	GFA2/IO85PDB5V0
E4	EMC_DB[10]/IO43NPB5V0	EMC_DB[10]/IO69NPB5V0	EMC_DB[10]/IO86NPB5V0
E5	GNDQ	GNDQ	GNDQ
E6	GND	GND	GND
E7	VCCFPGAIOB0	VCCFPGAIOB0	VCCFPGAIOB0
E8	GND	GND	GND
E9	VCCFPGAIOB0	VCCFPGAIOB0	VCCFPGAIOB0
E10	GND	GND	GND
E11	VCCFPGAIOB0	VCCFPGAIOB0	VCCFPGAIOB0
E12	GCB2/IO22PDB1V0	GCA1/IO28PDB1V0	GCA1/IO36PDB1V0 *
E13	VCCFPGAIOB1	VCCFPGAIOB1	VCCFPGAIOB1
E14	GCA2/IO21PDB1V0	GCB1/IO27PDB1V0	GCB1/IO34PDB1V0
E15	GCC2/IO23PDB1V0	GDC1/IO29PDB1V0	GDC1/IO38PDB1V0
E16	IO23NDB1V0	GDC0/IO29NDB1V0	GDC0/IO38NDB1V0
F1	EMC_DB[9]/IO40PDB5V0	EMC_DB[9]/GEC1/IO63PDB5V0	EMC_DB[9]/GEC1/IO80PDB5V0
F2	GND	GND	GND
F3	GFB2/IO42NDB5V0	GFB2/IO68NDB5V0	GFB2/IO85NDB5V0
F4	VCCFPGAIOB5	VCCFPGAIOB5	VCCFPGAIOB5
F5	EMC_DB[11]/IO43PPB5V0	EMC_DB[11]/IO69PPB5V0	EMC_DB[11]/IO86PPB5V0
F6	VCCFPGAIOB5	VCCFPGAIOB5	VCCFPGAIOB5
F7	GND	GND	GND
F8	VCC	VCC	VCC
F9	GND	GND	GND
F10	VCC	VCC	VCC
F11	GND	GND	GND
F12	IO22NDB1V0	GCA0/IO28NDB1V0	GCA0/IO36NDB1V0 *
F13	NC	GNDQ	GNDQ

Notes:

1. *Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.*
2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*

Pin No.	FG256		
	A2F060 Function	**A2F200 Function**	**A2F500 Function**
F14	IO21NDB1V0	GCB0/IO27NDB1V0	GCB0/IO34NDB1V0
F15	GND	GND	GND
F16	VCCENVM	VCCENVM	VCCENVM
G1	EMC_DB[8]/IO40NDB5V0	EMC_DB[8]/GEC0/IO63NDB5V0	EMC_DB[8]/GEC0/IO80NDB5V0
G2	EMC_DB[7]/IO39PDB5V0	EMC_DB[7]/GEB1/IO62PDB5V0	EMC_DB[7]/GEB1/IO79PDB5V0
G3	EMC_DB[6]/IO39NDB5V0	EMC_DB[6]/GEB0/IO62NDB5V0	EMC_DB[6]/GEB0/IO79NDB5V0
G4	GFC2/IO41PDB5V0	GFC2/IO67PDB5V0	GFC2/IO84PDB5V0
G5	IO41NDB5V0	IO67NDB5V0	IO84NDB5V0
G6	GND	GND	GND
G7	VCC	VCC	VCC
G8	GND	GND	GND
G9	VCC	VCC	VCC
G10	GND	GND	GND
G11	VCCFPGAIOB1	VCCFPGAIOB1	VCCFPGAIOB1
G12	VPP	VPP	VPP
G13	TRSTB	TRSTB	TRSTB
G14	TMS	TMS	TMS
G15	TCK	TCK	TCK
G16	GNDENVM	GNDENVM	GNDENVM
H1	GND	GND	GND
H2	EMC_DB[5]/IO38PPB5V0	EMC_DB[5]/GEA1/IO61PPB5V0	EMC_DB[5]/GEA1/IO78PPB5V0
H3	VCCFPGAIOB5	VCCFPGAIOB5	VCCFPGAIOB5
H4	EMC_DB[1]/IO36PDB5V0	EMC_DB[1]/GEB2/IO59PDB5V0	EMC_DB[1]/GEB2/IO76PDB5V0
H5	EMC_DB[0]/IO36NDB5V0	EMC_DB[0]/GEA2/IO59NDB5V0	EMC_DB[0]/GEA2/IO76NDB5V0
H6	VCCFPGAIOB5	VCCFPGAIOB5	VCCFPGAIOB5
H7	GND	GND	GND
H8	VCC	VCC	VCC
H9	GND	GND	GND
H10	VCC	VCC	VCC
H11	GND	GND	GND
H12	VJTAG	VJTAG	VJTAG

Notes:

1. *Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.*
2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*

Pin No.	FG256		
	A2F060 Function	**A2F200 Function**	**A2F500 Function**
H13	TDO	TDO	TDO
H14	TDI	TDI	TDI
H15	JTAGSEL	JTAGSEL	JTAGSEL
H16	GND	GND	GND
J1	EMC_DB[4]/IO38NPB5V0	EMC_DB[4]/GEA0/IO61NPB5V0	EMC_DB[4]/GEA0/IO78NPB5V0
J2	EMC_DB[3]/IO37PDB5V0	EMC_DB[3]/GEC2/IO60PDB5V0	EMC_DB[3]/GEC2/IO77PDB5V0
J3	EMC_DB[2]/IO37NDB5V0	EMC_DB[2]/IO60NDB5V0	EMC_DB[2]/IO77NDB5V0
J4	GNDRCOSC	GNDRCOSC	GNDRCOSC
J5	NC	GNDQ	GNDQ
J6	GND	GND	GND
J7	VCC	VCC	VCC
J8	GND	GND	GND
J9	VCC	VCC	VCC
J10	GND	GND	GND
J11	VCCMSSIOB2	VCCMSSIOB2	VCCMSSIOB2
J12	I2C_0_SCL/GPIO_23	I2C_0_SCL/GPIO_23	I2C_0_SCL/GPIO_23
J13	I2C_0_SDA/GPIO_22	I2C_0_SDA/GPIO_22	I2C_0_SDA/GPIO_22
J14	I2C_1_SCL/GPIO_31	I2C_1_SCL/GPIO_31	I2C_1_SCL/GPIO_31
J15	VCCMSSIOB2	VCCMSSIOB2	VCCMSSIOB2
J16	I2C_1_SDA/GPIO_30	I2C_1_SDA/GPIO_30	I2C_1_SDA/GPIO_30
K1	GPIO_1/IO32RSB4V0	MAC_MDIO/IO49RSB4V0	MAC_MDIO/IO58RSB4V0
K2	GPIO_0/IO33RSB4V0	MAC_MDC/IO48RSB4V0	MAC_MDC/IO57RSB4V0
K3	VCCMSSIOB4	VCCMSSIOB4	VCCMSSIOB4
K4	MSS_RESET_N	MSS_RESET_N	MSS_RESET_N
K5	VCCRCOSC	VCCRCOSC	VCCRCOSC
K6	VCCMSSIOB4	VCCMSSIOB4	VCCMSSIOB4
K7	GND	GND	GND
K8	VCC	VCC	VCC
K9	GND	GND	GND
K10	VCC	VCC	VCC
K11	GND	GND	GND

Notes:

1. *Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.*
2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*

Pin Number	FG484	
	A2F200 Function	**A2F500 Function**
F17	NC	IO25PPB1V0
F18	VCCFPGAIOB1	VCCFPGAIOB1
F19	IO23NDB1V0	IO28NDB1V0
F20	NC	IO31PDB1V0
F21	NC	IO31NDB1V0
F22	IO22PDB1V0	IO32PDB1V0
G1	GND	GND
G2	GFB0/IO65NPB5V0	GFB0/IO82NPB5V0
G3	EMC_DB[9]/GEC1/IO63PDB5V0	EMC_DB[9]/GEC1/IO80PDB5V0
G4	GFC1/IO66PPB5V0	GFC1/IO83PPB5V0
G5	EMC_DB[11]/IO69PPB5V0	EMC_DB[11]/IO86PPB5V0
G6	GNDQ	GNDQ
G7	NC	NC
G8	GND	GND
G9	VCCFPGAIOB0	VCCFPGAIOB0
G10	GND	GND
G11	VCCFPGAIOB0	VCCFPGAIOB0
G12	GND	GND
G13	VCCFPGAIOB0	VCCFPGAIOB0
G14	GND	GND
G15	VCCFPGAIOB0	VCCFPGAIOB0
G16	GNDQ	GNDQ
G17	NC	IO26PDB1V0
G18	NC	IO26NDB1V0
G19	GCA2/IO23PDB1V0	GCA2/IO28PDB1V0 *
G20	IO24NDB1V0	IO33NDB1V0
G21	GCB2/IO24PDB1V0	GCB2/IO33PDB1V0
G22	GND	GND
H1	EMC_DB[7]/GEB1/IO62PDB5V0	EMC_DB[7]/GEB1/IO79PDB5V0
H2	VCCFPGAIOB5	VCCFPGAIOB5
H3	EMC_DB[8]/GEC0/IO63NDB5V0	EMC_DB[8]/GEC0/IO80NDB5V0
H4	GND	GND
H5	GFC0/IO66NPB5V0	GFC0/IO83NPB5V0
H6	GFA1/IO64PDB5V0	GFA1/IO81PDB5V0

Notes:

1. *Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.*
2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*

Pin Number	FG484	
	A2F200 Function	**A2F500 Function**
T1	GND	GND
T2	VCCMSSIOB4	VCCMSSIOB4
T3	GPIO_8/IO39RSB4V0	GPIO_8/IO48RSB4V0
T4	GPIO_11/IO57RSB4V0	GPIO_11/IO66RSB4V0
T5	GND	GND
T6	MAC_CLK	MAC_CLK
T7	VCCMSSIOB4	VCCMSSIOB4
T8	VCC33SDD0	VCC33SDD0
T9	VCC15A	VCC15A
T10	GNDAQ	GNDAQ
T11	GND33ADC0	GND33ADC0
T12	ADC7	ADC7
T13	NC	TM4
T14	NC	VAREF2
T15	VAREFOUT	VAREFOUT
T16	VCCMSSIOB2	VCCMSSIOB2
T17	SPI_1_DO/GPIO_24	SPI_1_DO/GPIO_24
T18	GND	GND
T19	NC	NC
T20	NC	NC
T21	VCCMSSIOB2	VCCMSSIOB2
T22	GND	GND
U1	GND	GND
U2	GPIO_5/IO42RSB4V0	GPIO_5/IO51RSB4V0
U3	GPIO_10/IO58RSB4V0	GPIO_10/IO67RSB4V0
U4	VCCMSSIOB4	VCCMSSIOB4
U5	MAC_RXD[1]/IO53RSB4V0	MAC_RXD[1]/IO62RSB4V0
U6	NC	NC
U7	VCC33AP	VCC33AP
U8	VCC33N	VCC33N
U9	CM1	CM1
U10	VAREF0	VAREF0
U11	GND33ADC1	GND33ADC1
U12	ADC4	ADC4

Notes:

1. *Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.*
2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*

Pin Number	FG484	
	A2F200 Function	**A2F500 Function**
U13	NC	GNDTM2
U14	NC	ADC11
U15	GNDVAREF	GNDVAREF
U16	VCC33SDD1	VCC33SDD1
U17	SPI_0_DO/GPIO_16	SPI_0_DO/GPIO_16
U18	UART_0_RXD/GPIO_21	UART_0_RXD/GPIO_21
U19	VCCMSSIOB2	VCCMSSIOB2
U20	I2C_1_SCL/GPIO_31	I2C_1_SCL/GPIO_31
U21	I2C_0_SCL/GPIO_23	I2C_0_SCL/GPIO_23
U22	GND	GND
V1	GPIO_0/IO47RSB4V0	GPIO_0/IO56RSB4V0
V2	GPIO_6/IO41RSB4V0	GPIO_6/IO50RSB4V0
V3	GPIO_9/IO38RSB4V0	GPIO_9/IO47RSB4V0
V4	MAC_MDIO/IO49RSB4V0	MAC_MDIO/IO58RSB4V0
V5	MAC_RXD[0]/IO54RSB4V0	MAC_RXD[0]/IO63RSB4V0
V6	GND	GND
V7	SDD0	SDD0
V8	ABPS1	ABPS1
V9	ADC2	ADC2
V10	VCC33ADC0	VCC33ADC0
V11	ADC6	ADC6
V12	ADC5	ADC5
V13	ABPS5	ABPS5
V14	NC	ADC8
V15	NC	GND33ADC2
V16	NC	NC
V17	GND	GND
V18	SPI_0_DI/GPIO_17	SPI_0_DI/GPIO_17
V19	SPI_1_DI/GPIO_25	SPI_1_DI/GPIO_25
V20	UART_1_TXD/GPIO_28	UART_1_TXD/GPIO_28
V21	I2C_0_SDA/GPIO_22	I2C_0_SDA/GPIO_22
V22	I2C_1_SDA/GPIO_30	I2C_1_SDA/GPIO_30
W1	GPIO_2/IO45RSB4V0	GPIO_2/IO54RSB4V0
W2	GPIO_7/IO40RSB4V0	GPIO_7/IO49RSB4V0

Notes:

1. *Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.*
2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*

Revision	Changes	Page
Revision 5 (continued)	Available values for the Std. speed were added to the timing tables from Table 2-38 • 3.3 V LVTTL / 3.3 V LVCMOS High Slew to Table 2-92 • JTAG 1532 (SAR 29331). One or more values changed for the –1 speed in tables covering 3.3 V LVCMOS, 2.5 V LVCMOS, 1.8 V LVCMOS, 1.5 V LVCMOS, Combinatorial Cell Propagation Delays, and A2F200 Global Resources.	2-31 to 2-76
	Table 2-80 • A2F500 Global Resource is new.	2-60
	Table 2-90 • eNVM Block Timing, Worst Commercial Case Conditions: T_J = 85°C, VCC = 1.425 V was revised (SAR 27585).	2-76
	The programmable analog specifications tables were revised with updated information.	2-78 to 2-87
	Table 4-1 • Supported JTAG Programming Hardware was revised by adding a note to indicate "planned support" for several of the items in the table.	4-7
	The note on JTAGSEL in the "In-System Programming" section was revised to state that SoftConsole selects the appropriate TAP controller using the CTXSELECT JTAG command. When using SoftConsole, the state of JTAGSEL is a "don't care" (SAR 29261).	4-7
	The "CS288" and "FG256" pin tables for A2F060 are new, comparing the A2F060 function with the A2F200 function (SAR 29353).	5-24
	The "Handling When Unused" column was removed from the "FG256" pin table for A2F200 and A2F500 (SAR 29691).	5-42
Revision 4 (September 2010)	Table 2-8 • Power Supplies Configuration was revised. VCCRCOSC was moved to a column of its own with new values. VCCENVM was added to the table. Standby mode for VJTAG and VPP was changed from 0 V to N/A. "Disable" was changed to "Off" in the eNVM column. The column for RCOSC was deleted.	2-10
	The "Power-Down and Sleep Mode Implementation" section was revised to include VCCROSC.	2-11
Revision 3 (September 2010)	The "I/Os and Operating Voltage" section was revised to list "single 3.3 V power supply with on-chip 1.5 V regulator" and "external 1.5 V is allowed" (SAR 27663).	I
	The CS288 package was added to the "Package I/Os: MSS + FPGA I/Os" table (SAR 27101), "Product Ordering Codes" table, and "Temperature Grade Offerings" table (SAR 27044). The number of direct analog inputs for the FG256 package in A2F060 was changed from 8 to 6.	III, VI, VI
	Two notes were added to the "SmartFusion cSoC Family Product Table" indicating limitations for features of the A2F500 device: *Two PLLs are available in CS288 and FG484 (one PLL in FG256).* *[ADCs, DACs, SCBs, comparators, current monitors, and bipolar high voltage monitors are] Available on FG484 only. FG256 and CS288 packages offer the same programmable analog capabilities as A2F200.* Table cells were merged in rows containing the same values for easier reading (SAR 24748).	II
	The security feature option was added to the "Product Ordering Codes" table.	VI