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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details	
Product Status	Obsolete
Architecture	MCU, FPGA
Core Processor	ARM® Cortex®-M3
Flash Size	128KB
RAM Size	16KB
Peripherals	DMA, POR, WDT
Connectivity	EBI/EMI, I²C, SPI, UART/USART
Speed	100MHz
Primary Attributes	ProASIC®3 FPGA, 60K Gates, 1536D-Flip-Flops
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	144-LQFP
Supplier Device Package	144-TQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/a2f060m3e-1tqg144i

Table 2-4 • FPGA and Embedded Flash Programming, Storage and Operating Limits

Product Grade	Storage Temperature	Element	Grade Programming Cycles	Retention
Commercial	Min. T_J = 0°C Max. T_J = 85°C	FPGA/FlashROM	500	20 years
		Embedded Flash	< 1,000	20 years
			< 10,000	10 years
			< 15,000	5 years
Industrial	Min. T_J = –40°C Max. T_J = 100°C	FPGA/FlashROM	500	20 years
		Embedded Flash	< 1,000	20 years
			< 10,000	10 years
			< 15,000	5 years

Table 2-5 • Overshoot and Undershoot Limits [1]

VCCxxxxIOBx	Average VCCxxxxIOBx–GND Overshoot or Undershoot Duration as a Percentage of Clock Cycle[2]	Maximum Overshoot/ Undershoot[2]
2.7 V or less	10%	1.4 V
	5%	1.49 V
3 V	10%	1.1 V
	5%	1.19 V
3.3 V	10%	0.79 V
	5%	0.88 V
3.6 V	10%	0.45 V
	5%	0.54 V

Notes:

1. *Based on reliability requirements at 85°C.*
2. *The duration is allowed at one out of six clock cycles. If the overshoot/undershoot occurs at one out of two cycles, the maximum overshoot/undershoot has to be reduced by 0.15 V.*
3. *This table does not provide PCI overshoot/undershoot limits.*

Power Supply Sequencing Requirement

SmartFusion cSoCs have an on-chip 1.5 V regulator, but usage of an external 1.5 V supply is also allowed while the on-chip regulator is disabled. In that case, the 3.3 V supplies (VCC33A, etc.) should be powered before 1.5 V (VCC, etc.) supplies. The 1.5 V supplies should be enabled only after 3.3 V supplies reach a value higher than 2.7 V.

I/O Power-Up and Supply Voltage Thresholds for Power-On Reset (Commercial and Industrial)

Sophisticated power-up management circuitry is designed into every SmartFusion cSoC. These circuits ensure easy transition from the powered-off state to the powered-up state of the device. In addition, the I/O will be in a known state through the power-up sequence. The basic principle is shown in Figure 2-1 on page 2-6.

There are five regions to consider during power-up.

SmartFusion I/Os are activated only if ALL of the following three conditions are met:

1. VCC and VCCxxxxIOBx are above the minimum specified trip points (Figure 2-1 on page 2-6).
2. VCCxxxxIOBx > VCC – 0.75 V (typical)
3. Chip is in the SoC Mode.

Table 2-11 • Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings Applicable to MSS I/O Banks

	VCCMSSIOBx (V)	Static Power PDC7 (mW)	Dynamic Power PAC9 (µW/MHz)
Single-Ended			
3.3 V LVTTL / 3.3 V LVCMOS	3.3	–	17.21
3.3 V LVCMOS / 3.3 V LVCMOS – Schmitt trigger	3.3	–	20.00
2.5 V LVCMOS	2.5	–	5.55
2.5 V LVCMOS – Schmitt trigger	2.5	–	7.03
1.8 V LVCMOS	1.8	–	2.61
1.8 V LVCMOS – Schmitt trigger	1.8	–	2.72
1.5 V LVCMOS (JESD8-11)	1.5	–	1.98
1.5 V LVCMOS (JESD8-11) – Schmitt trigger	1.5	–	1.93

Table 2-12 • Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings* Applicable to FPGA I/O Banks, I/O Assigned to EMC I/O Pins

	C_{LOAD} (pF)	VCCFPGAIOBx (V)	Static Power PDC8 (mW)	Dynamic Power PAC10 (µW/MHz)
Single-Ended				
3.3 V LVTTL / 3.3 V LVCMOS	35	3.3	–	475.66
2.5 V LVCMOS	35	2.5	–	270.50
1.8 V LVCMOS	35	1.8	–	152.17
1.5 V LVCMOS (JESD8-11)	35	1.5	–	104.44
3.3 V PCI	10	3.3	–	202.69
3.3 V PCI-X	10	3.3	–	202.69
Differential				
LVDS	–	2.5	7.74	88.26
LVPECL	–	3.3	19.54	164.99

*Note: *Dynamic power consumption is given for standard load and software default drive strength and output slew.*

Table 2-13 • Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings Applicable to MSS I/O Banks

	C_{LOAD} (pF)	VCCMSSIOBx (V)	Static Power PDC8 (mW)[2]	Dynamic Power PAC10 (µW/MHz)[3]
Single-Ended				
3.3 V LVTTL / 3.3 V LVCMOS	10	3.3	–	155.65
2.5 V LVCMOS	10	2.5	–	88.23
1.8 V LVCMOS	10	1.8	–	45.03
1.5 V LVCMOS (JESD8-11)	10	1.5	–	31.01

Table 2-63 • LVDS Minimum and Maximum DC Input and Output Levels

DC Parameter	Description	Min.	Typ.	Max.	Units
VCCFPGAIOBx	Supply voltage	2.375	2.5	2.625	V
VOL	Output low voltage	0.9	1.075	1.25	V
VOH	Output high voltage	1.25	1.425	1.6	V
I_{OL}[1]	Output lower current	0.65	0.91	1.16	mA
I_{OH}[1]	Output high current	0.65	0.91	1.16	mA
VI	Input voltage	0		2.925	V
I_{IH}[2]	Input high leakage current			15	µA
I_{IL}[2]	Input low leakage current			15	µA
V_{ODIFF}	Differential output voltage	250	350	450	mV
V_{OCM}	Output common mode voltage	1.125	1.25	1.375	V
V_{ICM}	Input common mode voltage	0.05	1.25	2.35	V
V_{IDIFF}	Input differential voltage	100	350		mV

Notes:

1. *I_{OL}/I_{OH} defined by V_{ODIFF}/(resistor network).*
2. *Currents are measured at 85°C junction temperature.*

Table 2-64 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	V_{REF} (typ.) (V)
1.075	1.325	Cross point	–

* *Measuring point = V_{trip}. See Table 2-22 on page 2-24 for a complete table of trip points.*

Timing Characteristics

Table 2-65 • LVDS
Worst Commercial-Case Conditions: T_J = 85°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCFPGAIOBx = 2.3 V
Applicable to FPGA I/O Banks, I/O Assigned to EMC I/O Pins

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	Units
Std.	0.60	1.83	0.04	1.87	ns
–1	0.50	1.53	0.03	1.55	ns

Notes:

1. *For the derating values at specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.*
2. *The above mentioned timing parameters correspond to 24mA drive strength.*

Table 2-66 • Minimum and Maximum DC Input and Output Levels

DC Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
VCCFPGAIOBx	Supply Voltage	3.0		3.3		3.6		V
VOL	Output Low Voltage	0.96	1.27	1.06	1.43	1.30	1.57	V
VOH	Output High Voltage	1.8	2.11	1.92	2.28	2.13	2.41	V
VIL, VIH	Input Low, Input High Voltages	0	3.6	0	3.6	0	3.6	V
VODIFF	Differential Output Voltage	0.625	0.97	0.625	0.97	0.625	0.97	V
VOCM	Output Common-Mode Voltage	1.762	1.98	1.762	1.98	1.762	1.98	V
VICM	Input Common-Mode Voltage	1.01	2.57	1.01	2.57	1.01	2.57	V
VIDIFF	Input Differential Voltage	300		300		300		mV

Table 2-67 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	V_{REF} (typ.) (V)
1.64	1.94	Cross point	–

* *Measuring point = V_{trip}. See Table 2-22 on page 2-24 for a complete table of trip points.*

Timing Characteristics

Table 2-68 • LVPECL
Worst Commercial-Case Conditions: T_J = 85°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCFPGAIOBx = 3.0 V
Applicable to FPGA I/O Banks, I/O Assigned to EMC I/O Pins

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	Units
Std.	0.60	1.76	0.04	1.76	ns
–1	0.50	1.46	0.03	1.46	ns

Notes:

1. *For the derating values at specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.*
2. *The above mentioned timing parameters correspond to 24mA drive strength.*

DDR Module Specifications

Input DDR Module

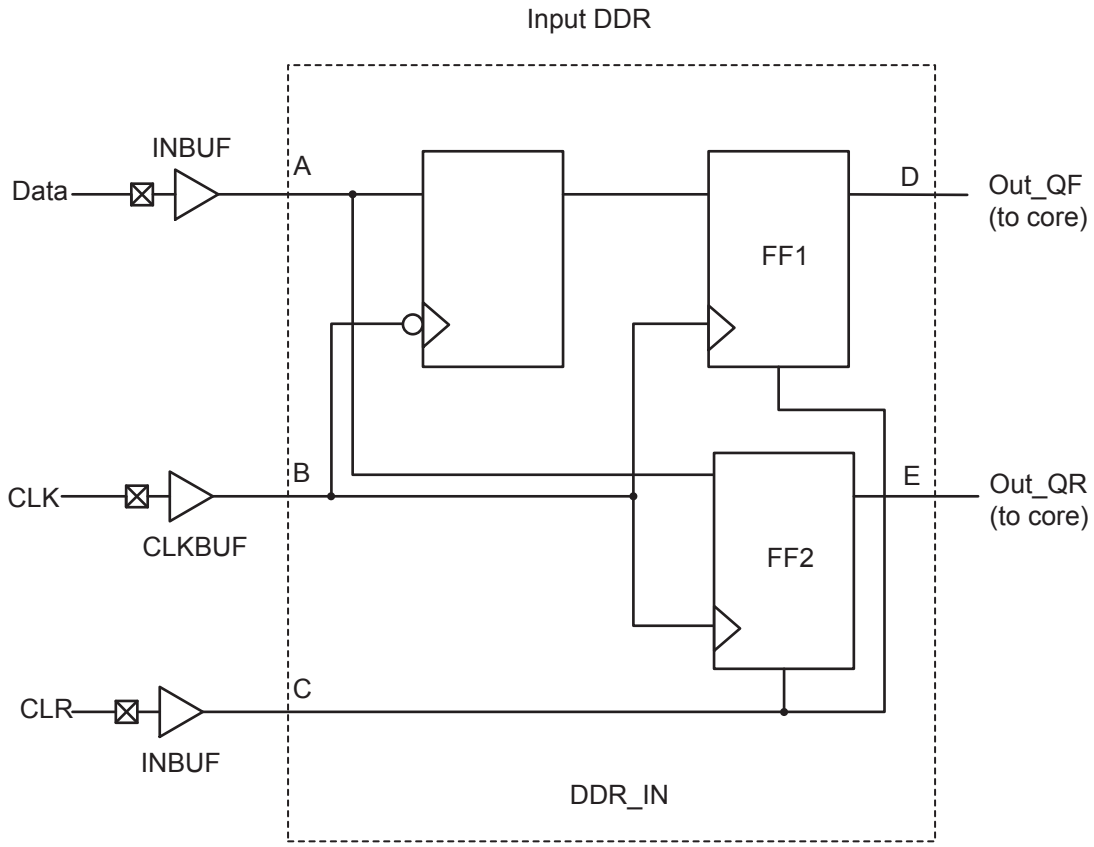


Figure 2-19 • **Input DDR Timing Model**

Table 2-74 • **Parameter Definitions**

Parameter Name	Parameter Definition	Measuring Nodes (from, to)
$t_{DDRICLKQ1}$	Clock-to-Out Out_QR	B, D
$t_{DDRICLKQ2}$	Clock-to-Out Out_QF	B, E
$t_{DDRISUD}$	Data Setup Time of DDR input	A, B
t_{DDRIHD}	Data Hold Time of DDR input	A, B
$t_{DDRICLR2Q1}$	Clear-to-Out Out_QR	C, D
$t_{DDRICLR2Q2}$	Clear-to-Out Out_QF	C, E
$t_{DDRIREMCLR}$	Clear Removal	C, B
$t_{DDRIRECCLR}$	Clear Recovery	C, B

Clock Conditioning Circuits

CCC Electrical Specifications

Timing Characteristics

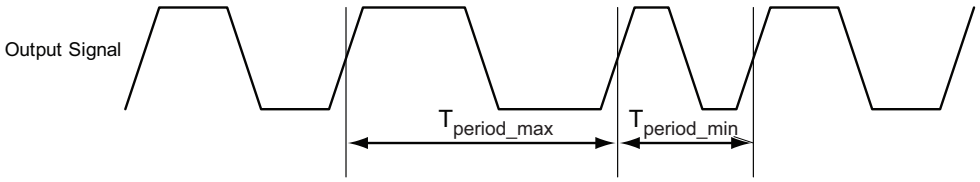
***Table 2-86* • SmartFusion CCC/PLL Specification**

Parameter	Minimum	Typical	Maximum	Units
Clock Conditioning Circuitry Input Frequency f_{IN_CCC}	1.5		350	MHz
Clock Conditioning Circuitry Output Frequency f_{OUT_CCC}	0.75		350[1]	MHz
Delay Increments in Programmable Delay Blocks[2,3,4]		160		ps
Number of Programmable Values in Each Programmable Delay Block			32	
Input Period Jitter			1.5	ns
Acquisition Time				
LockControl = 0			300	µs
LockControl = 1			6.0	ms
Tracking Jitter[5]				
LockControl = 0			1.6	ns
LockControl = 1			0.8	ns
Output Duty Cycle	48.5		5.15	%
Delay Range in Block: Programmable Delay 1[2,3]	0.6		5.56	ns
Delay Range in Block: Programmable Delay 2[2,3]	0.025		5.56	ns
Delay Range in Block: Fixed Delay[2,3]		2.2		ns
CCC Output Peak-to-Peak Period Jitter F_{CCC_OUT} [6,7]	Maximum Peak-to-Peak Period Jitter			

	SSO ≤ 2		SSO ≤ 4		SSO ≤ 8		SSO ≤ 16	
	FG/CS	PQ	FG/CS	PQ	FG/CS	PQ	FG/CS	PQ
0.75 MHz to 50 MHz	0.5%	1.6%	0.9%	1.6%	0.9%	1.6%	0.9%	1.8%
50 MHz to 250 MHz	1.75%	3.5%	9.3%	9.3%	9.3%	17.9%	10.0%	17.9%
250 MHz to 350 MHz	2.5%	5.2%	13.0%	13.0%	13.0%	25.0%	14.0%	25.0%

Notes:

1. *One of the CCC outputs (GLA0) is used as an MSS clock and is limited to 100 MHz (maximum) by software. Details regarding CCC/PLL are in the "PLLs, Clock Conditioning Circuitry, and On-Chip Crystal Oscillators" chapter of the SmartFusion Microcontroller Subsystem User's Guide.*
2. *This delay is a function of voltage and temperature. See Table 2-7 on page 2-9 for deratings.*
3. *T_J = 25°C, VCC = 1.5 V*
4. *When the CCC/PLL core is generated by Microsemi core generator software, not all delay values of the specified delay increments are available. Refer to the Libero SoC Online Help associated with the core for more information.*
5. *Tracking jitter is defined as the variation in clock edge position of PLL outputs with reference to the PLL input clock edge. Tracking jitter does not measure the variation in PLL output period, which is covered by the period jitter parameter.*
6. *Measurement done with LVTTL 3.3 V 12 mA I/O drive strength and High slew rate. VCC/VCCPLL = 1.425 V, VCCI = 3.3V, 20 pF output load. All I/Os are placed outside of the PLL bank.*
7. *SSOs are outputs that are synchronous to a single clock domain and have their clock-to-out within ± 200 ps of each other.*
8. *VCO output jitter is calculated as a percentage of the VCO frequency. The jitter (in ps) can be calculated by multiplying the VCO period by the % jitter. The VCO jitter (in ps) applies to CCC_OUT regardless of the output divider settings. For example, if the jitter on VCO is 300 ps, the jitter on CCC_OUT is also 300 ps.*



Note: Peak-to-peak jitter measurements are defined by $T_{peak\text{-}to\text{-}peak} = T_{period\_max} - T_{period\_min}$.

Figure 2-28 • **Peak-to-Peak Jitter Definition**

Temperature Monitor

Unless otherwise noted, temperature monitor performance is specified with a 2N3904 diode-connected bipolar transistor from National Semiconductor or Infineon Technologies, nominal power supply voltages, with the output measured using the internal voltage reference with the internal ADC in 12-bit mode and 62.5 Ksps. After digital compensation. Unless otherwise noted, the specifications pertain to conditions where the SmartFusion cSoC and the sensing diode are at the same temperature.

Table 2-94 • **Temperature Monitor Performance Specifications**

Specification	Test Conditions	Min.	Typical	Max.	Units
Input diode temperature range		–55		150	°C
		233.2		378.15	K
Temperature sensitivity			2.5		mV/K
Intercept	Extrapolated to 0K		0		V
Input referred temperature offset error	At 25°C (298.15K)		±1	1.5	°C
Gain error	Slope of BFSL vs. 2.5 mV/K		±1	2.5	% nom.
Overall accuracy	Peak error from ideal transfer function		±2	±3	°C
Input referred noise	At 25°C (298.15K) – no output averaging		4		°C rms
Output current	Idle mode		100		µA
	Final measurement phases		10		µA
Analog settling time	Measured to 0.1% of final value, (with ADC load)				
	From TM_STB (High)	5			µs
	From ADC_START (High)	5		105	µs
AT parasitic capacitance				500	pF
Power supply rejection ratio	DC (0–10 KHz)	1.2	0.7		°C/V
Input referred temperature sensitivity error	Variation due to device temperature (–40°C to +100°C). External temperature sensor held constant.		0.005	0.008	°C/°C
Temperature monitor (TM) operational power supply current requirements (per temperature monitor instance, not including ADC or VAREFx)	VCC33A		200		µA
	VCC33AP		150		µA
	VCC15A		50		µA

Note: All results are based on averaging over 64 samples.

Table 2-100 • SPI Characteristics
Commercial Case Conditions: T_J = 85ºC, VDD = 1.425 V, –1 Speed Grade (continued)

Symbol	Description and Condition	A2F060	A2F200	A2F500	Unit
sp6	Data from master (SPI_x_DO) setup time [2]	1	1	1	pclk cycles
sp7	Data from master (SPI_x_DO) hold time [2]	1	1	1	pclk cycles
sp8	SPI_x_DI setup time [2]	1	1	1	pclk cycles
sp9	SPI_x_DI hold time [2]	1	1	1	pclk cycles

Notes:

1. *These values are provided for a load of 35 pF. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website: http://www.microsemi.com/index.php?option=com_microsemi&Itemid=489&lang=en&view=salescontact.*
2. *For allowable pclk configurations, refer to the Serial Peripheral Interface Controller section in the SmartFusion Microcontroller Subsystem User's Guide.*

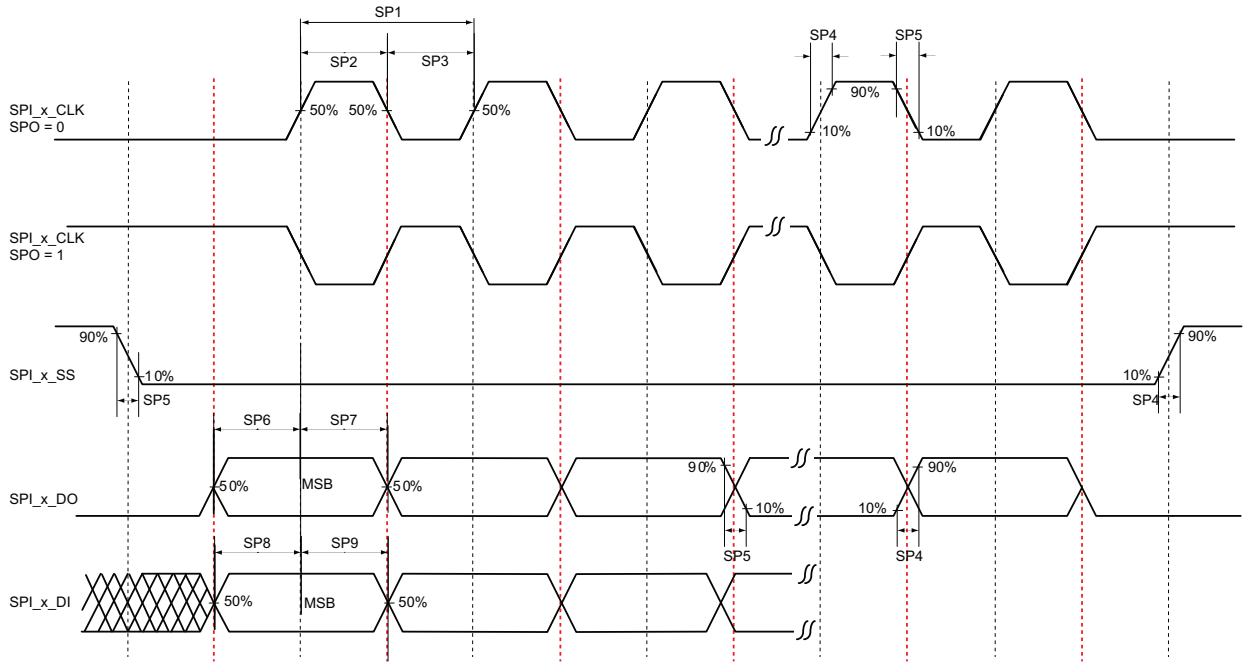


Figure 2-47 • SPI Timing for a Single Frame Transfer in Motorola Mode (SPH = 1)

Inter-Integrated Circuit (I^2C) Characteristics

This section describes the DC and switching of the I^2C interface. Unless otherwise noted, all output characteristics given are for a 100 pF load on the pins. For timing parameter definitions, refer to Figure 2-48 on page 2-92.

***Table 2-101* • I^2C Characteristics**
Commercial Case Conditions: T_J = 85ºC, V_{DD} = 1.425 V, –1 Speed Grade

Parameter	Definition	Condition	Value	Unit
V_{IL}	Minimum input low voltage	–	See Table 2-36 on page 2-30	–
	Maximum input low voltage	–	See Table 2-36	–
V_{IH}	Minimum input high voltage	–	See Table 2-36	–
	Maximum input high voltage	–	See Table 2-36	–
V_{OL}	Maximum output voltage low	I_{OL} = 8 mA	See Table 2-36	–
I_{IL}	Input current high	–	See Table 2-36	–
I_{IH}	Input current low	–	See Table 2-36	–
V_{hyst}	Hysteresis of Schmitt trigger inputs	–	See Table 2-33 on page 2-29	V
T_{FALL}	Fall time [2]	VIHmin to VILMax, C_{load} = 400 pF	15.0	ns
		VIHmin to VILMax, C_{load} = 100 pF	4.0	ns
T_{RISE}	Rise time [2]	VILMax to VIHmin, C_{load} = 400pF	19.5	ns
		VILMax to VIHmin, C_{load} = 100pF	5.2	ns
Cin	Pin capacitance	VIN = 0, f = 1.0 MHz	8.0	pF
$R_{pull-up}$	Output buffer maximum pull-down Resistance [1]	–	50	Ω
$R_{pull-down}$	Output buffer maximum pull-up Resistance [1]	–	150	Ω
D_{max}	Maximum data rate	Fast mode	400	Kbps
t_{LOW}	Low period of I2C_x_SCL [3]	–	1	pclk cycles
t_{HIGH}	High period of I2C_x_SCL [3]	–	1	pclk cycles
$t_{HD;STA}$	START hold time [3]	–	1	pclk cycles
$t_{SU;STA}$	START setup time [3]	–	1	pclk cycles
$t_{HD;DAT}$	DATA hold time [3]	–	1	pclk cycles
$t_{SU;DAT}$	DATA setup time [3]	–	1	pclk cycles

Notes:

1. *These maximum values are provided for information only. Minimum output buffer resistance values depend on VCCxxxxIOBx, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the SoC Products Group website at http://www.microsemi.com/index.php?option=com_microsemi&Itemid=489&lang=en&view=salescontact.*
2. *These values are provided for a load of 100 pF and 400 pF. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the SoC Products Group website at http://www.microsemi.com/index.php?option=com_microsemi&Itemid=489&lang=en&view=salescontact.*
3. *For allowable Pclk configurations, refer to the Inter-Integrated Circuit (I^2C) Peripherals section in the SmartFusion Microcontroller Subsystem User's Guide.*

Emcraft Systems provides porting of the open-source U-boot firmware and uClinux™ kernel to the SmartFusion cSoC, a Linux®-based cross-development framework, and other complementary components. Combined with the release of its A2F-Linux Evaluation Kit, this provides a low-cost platform for evaluation and development of Linux (uClinux) on the Cortex-M3 CPU core of the Microsemi SmartFusion cSoC.

- Emcraft Linux on Microsemi's SmartFusion cSoC

Keil offers the RTX Real-Time Kernel as a royalty-free, deterministic RTOS designed for ARM and Cortex-M devices. It allows you to create programs that simultaneously perform multiple functions and helps to create applications which are better structured and more easily maintained.

- The RTX Real-Time Kernel is included with MDK-ARM. Download the Evaluation version of Keil MDK-ARM.
- RTX source code is available as part of Keil/ARM Real-Time Library (RL-ARM), a group of tightly-coupled libraries designed to solve the real-time and communication challenges of embedded systems based on ARM-powered microcontroller devices. The RL-ARM library now supports SmartFusion cSoCs and designers with additional key features listed in the "Middleware" section on page 3-5.

Micrium supports SmartFusion cSoCs with the company's flagship µC/OS family, recognized for a variety of features and benefits, including unparalleled reliability, performance, dependability, impeccable source code and vast documentation. Micrium supports the following products for SmartFusion cSoCs and continues to work with Microsemi on additional projects.

- SmartFusion Quickstart Guide for Micrium µC/OS-III Examples
  - Design Files

µC/OS-III™, Micrium's newest RTOS, is designed to save time on your next embedded project and puts greater control of the software in your hands.

RoweBots provides an ultra tiny Linux-compatible RTOS called Unison for SmartFusion. Unison consists of a set of modular software components, which, like Linux, are either free or commercially licensed. Unison offers POSIX® and Linux compatibility with hard real-time performance, complete I/O modules and an easily understood environment for device driver programming. Seamless integration with FPGA and analog features are fast and easy.

- Unison V4-based products include a free Unison V4 Linux and POSIX-compatible kernel with serial I/O, file system, six demonstration programs, upgraded documentation and source code for Unison V4, and free (for non-commercial use) Unison V4 TCP/IP server. Commercial license upgrade is available for Unison V4 TCP/IP server with three demonstration programs, DHCP client and source code.
- Unison V5-based products include commercial Unison V5 Linux- and POSIX-compatible kernel with serial I/O, file system, extensive feature set, full documentation, source code and more than 20 demonstration programs, Unison V5 TCP/IPv4 with extended feature set, sockets interface, multiple network interfaces, PPP support, DHCP client, documentation, source code and six demonstration programs, and multiple other features.

Middleware

Microsemi has ported both uIP and lwIP for Ethernet support as well as including TFTP file service.

- SmartFusion Webserver Demo Using uIP and FreeRTOS
- SmartFusion: Running Webserver, TFTP on lwIP TCP/IP Stack Application Note

The Keil/ARM Real-Time Library (RL-ARM)[1], in addition to RTX source, includes the following:

- RL-TCPnet (TCP/IP) – The Keil RL-TCPnet library, supporting full TCP/IP and UDP protocols, is a full networking suite specifically written for small ARM and Cortex-M processor-based microcontrollers. TCPnet is now ported to and supports SmartFusion Cortex-M3. It is highly optimized, has a small code footprint, and gives excellent performance, providing a wide range of application level protocols and examples such as FTP, SNMP, SOAP and AJAX. An HTTP server example of TCPnet working in a SmartFusion design is available.

1. The CAN and USB functions within RL-ARM are not supported for SmartFusion cSoC.

- Flash File System (RL-Flash) allows your embedded applications to create, save, read, and modify files in standard storage devices such as ROM, RAM, or FlashROM, using a standard serial peripheral interface (SPI). Many ARM-based microcontrollers have a practical requirement for a standard file system. With RL-FlashFS you can implement new features in embedded applications such as data logging, storing program state during standby modes, or storing firmware upgrades.

Micrium, in addition to µC/OS-III®, offers the following support for SmartFusion cSoC:

- µC/TCP-IP™ is a compact, reliable, and high-performance stack built from the ground up by Micrium and has the quality, scalability, and reliability that translates into a rapid configuration of network options, remarkable ease-of-use, and rapid time-to-market.
- µC/Probe™ is one of the most useful tools in embedded systems design and puts you in the driver's seat, allowing you to take charge of virtually any variable, memory location, and I/O port in your embedded product, while your system is running.

References

PCB Files

A2F500 SmartFusion Development Kit PCB Files

http://www.microsemi.com/index.php?option=com_docman&task=doc_download&gid=130770

A2F200 SmartFusion Development Kit PCB Files

http://www.microsemi.com/index.php?option=com_docman&task=doc_download&gid=130773

Application Notes

SmartFusion cSoC Board Design Guidelines

http://www.microsemi.com/index.php?option=com_docman&task=doc_download&gid=129815

Special Function Pins

Name	Type	Polarity/Bus Size	Description
NC			No connect This pin is not connected to circuitry within the device. These pins can be driven to any voltage or can be left floating with no effect on the operation of the device.
DC			Do not connect. This pin should not be connected to any signals on the PCB. These pins should be left unconnected.
LPXIN	In	1	Low power 32 KHz crystal oscillator. Input from the 32 KHz oscillator. Pin for connecting a low power 32 KHz watch crystal. If not used, the LPXIN pin can be left floating. For more information, see the PLLs, Clock Conditioning Circuitry, and On-Chip Crystal Oscillators section in the *SmartFusion Microcontroller Subsystem User's Guide*.
LPXOUT	In	1	Low power 32 KHz crystal oscillator. Output to the 32 KHz oscillator. Pin for connecting a low power 32 KHz watch crystal. If not used, the LPXOUT pin can be left floating. For more information, see the PLLs, Clock Conditioning Circuitry, and On-Chip Crystal Oscillators section in the *SmartFusion Microcontroller Subsystem User's Guide*.
MAINXIN	In	1	Main crystal oscillator circuit. Input to the crystal oscillator circuit. Pin for connecting an external crystal, ceramic resonator, or RC network. When using an external crystal or ceramic oscillator, external capacitors are also recommended. Refer to documentation from the crystal oscillator manufacturer for proper capacitor value. If an external RC network or clock input is used, the RC components are connected to the MAINXIN pin, with MAINXOUT left floating. When the main crystal oscillator is not being used, MAINXIN and MAINXOUT pins can be left floating. For more information, see the PLLs, Clock Conditioning Circuitry, and On-Chip Crystal Oscillators section in the *SmartFusion Microcontroller Subsystem User's Guide*.
MAINXOUT	Out	1	Main crystal oscillator circuit. Output from the crystal oscillator circuit. Pin for connecting external crystal or ceramic resonator. When using an external crystal or ceramic oscillator, external capacitors are also recommended. Refer to documentation from the crystal oscillator manufacturer for proper capacitor value. If an external RC network or clock input is used, the RC components are connected to the MAINXIN pin, with MAINXOUT left floating. When the main crystal oscillator is not being used, MAINXIN and MAINXOUT pins can be left floating. For more information, see the PLLs, Clock Conditioning Circuitry, and On-Chip Crystal Oscillators section in the *SmartFusion Microcontroller Subsystem User's Guide*.

JTAG Pins

SmartFusion cSoCs have a separate bank for the dedicated JTAG pins. The JTAG pins can be run at any voltage from 1.5 V to 3.3 V (nominal). VCC must also be powered for the JTAG state machine to operate, even if the device is in bypass mode; VJTAG alone is insufficient. Both VJTAG and VCC to the SmartFusion cSoC part must be supplied to allow JTAG signals to transition the SmartFusion cSoC. Isolating the JTAG power supply in a separate I/O bank gives greater flexibility with supply selection and simplifies power supply and PCB design. If the JTAG interface is neither used nor planned to be used, the VJTAG pin together with the TRSTB pin could be tied to GND.

Name	Type	Polarity/ Bus Size	Description
JTAGSEL	In	1	JTAG controller selection Depending on the state of the JTAGSEL pin, an external JTAG controller will either see the FPGA fabric TAP/auxiliary TAP (High) or the Cortex-M3 JTAG debug interface (Low). The JTAGSEL pin should be connected to an external pull-up resistor such that the default configuration selects the FPGA fabric TAP.
TCK	In	1	Test clock Serial input for JTAG boundary scan, ISP, and UJTAG. The TCK pin does not have an internal pull-up/-down resistor. If JTAG is not used, it is recommended to tie off TCK to GND or V_{JTAG} through a resistor placed close to the FPGA pin. This prevents JTAG operation in case TMS enters an undesired state. Note that to operate at all V_{JTAG} voltages, 500 Ω to 1 kΩ will satisfy the requirements. Refer to Table 5-1 on page 5-11 for more information. Can be left floating when unused.
TDI	In	1	Test data Serial input for JTAG boundary scan, ISP, and UJTAG usage. There is an internal weak pull-up resistor on the TDI pin.
TDO	Out	1	Test data Serial output for JTAG boundary scan, ISP, and UJTAG usage.
TMS	In	HIGH	Test mode select The TMS pin controls the use of the IEEE1532 boundary scan pins (TCK, TDI, TDO, TRST). There is an internal weak pull-up resistor on the TMS pin. Can be left floating when unused.
TRSTB	In	HIGH	Boundary scan reset pin The TRST pin functions as an active low input to asynchronously initialize (or reset) the boundary scan circuitry. There is an internal weak pull-up resistor on the TRST pin. If JTAG is not used, an external pull-down resistor could be included to ensure the TAP is held in reset mode. The resistor values must be chosen from Table 5-1 on page 5-11 and must satisfy the parallel resistance value requirement. The values in Table 5-1 on page 5-11 correspond to the resistor recommended when a single device is used. The values correspond to the equivalent parallel resistor when multiple devices are connected via a JTAG chain. In critical applications, an upset in the JTAG circuit could allow entering an undesired JTAG state. In such cases, it is recommended that you tie off TRST to GND through a resistor placed close to the FPGA pin. The TRSTB pin also resets the serial wire JTAG – debug port (SWJ-DP) circuitry within the Cortex-M3. Can be left floating when unused.

Analog Front-End Pin-Level Function Multiplexing

Table 5-2 describes the relationships between the various internal signals found in the analog front-end (AFE) and how they are multiplexed onto the external package pins. Note that, in general, only one function is available for those pads that have numerous functions listed. The exclusion to this rule is when a comparator is used; the ADC can still convert either input side of the comparator.

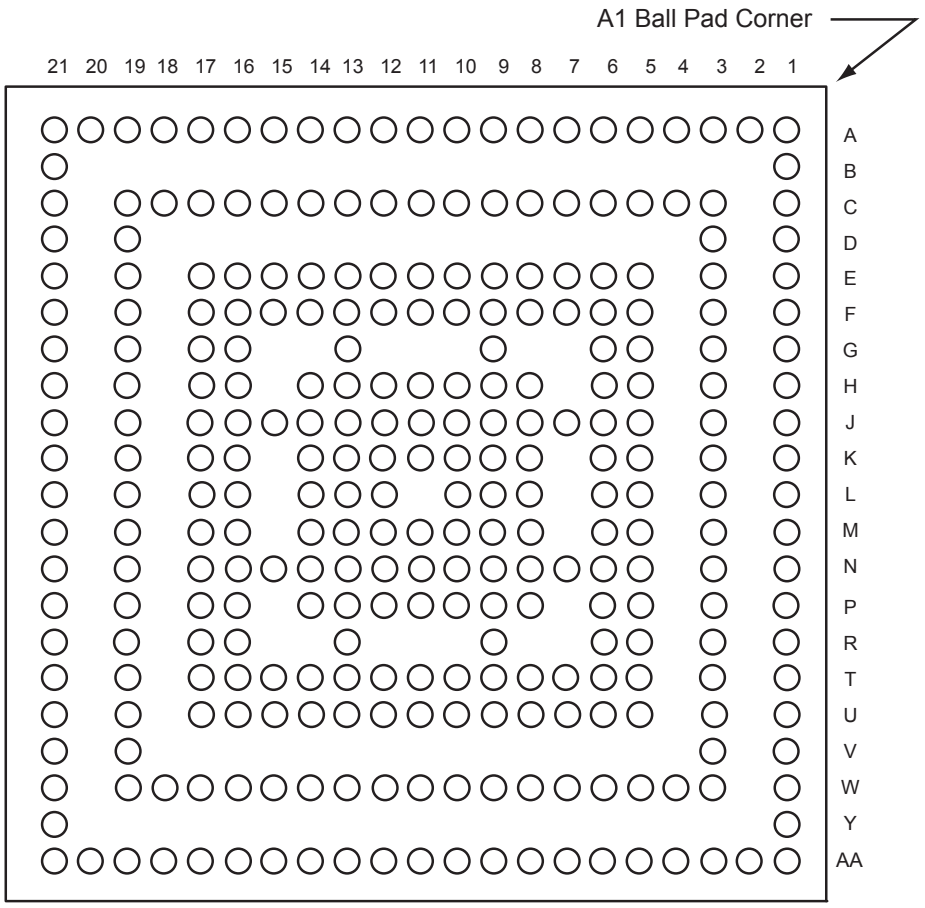
***Table 5-2* • Relationships Between Signals in the Analog Front-End**

Pin	ADC Channel	Dir.-In Option	Prescaler	Current Mon.	Temp. Mon.	Compar.	LVTTL	SDD MUX	SDD
ABPS0	ADC0_CH1		ABPS0_IN						
ABPS1	ADC0_CH2		ABPS1_IN						
ABPS2	ADC0_CH5		ABPS2_IN						
ABPS3	ADC0_CH6		ABPS3_IN						
ABPS4	ADC1_CH1		ABPS4_IN						
ABPS5	ADC1_CH2		ABPS5_IN						
ABPS6	ADC1_CH5		ABPS6_IN						
ABPS7	ADC1_CH6		ABPS7_IN						
ABPS8	ADC2_CH1		ABPS8_IN						
ABPS9	ADC2_CH2		ABPS9_IN						
ADC0	ADC0_CH9	Yes				CMP1_P	LVTTL0_IN		
ADC1	ADC0_CH10	Yes				CMP1_N	LVTTL1_IN	SDDM0_OUT	
ADC2	ADC0_CH11	Yes				CMP3_P	LVTTL2_IN		
ADC3	ADC0_CH12	Yes				CMP3_N	LVTTL3_IN	SDDM1_OUT	
ADC4	ADC1_CH9	Yes				CMP5_P	LVTTL4_IN		
ADC5	ADC1_CH10	Yes				CMP5_N	LVTTL5_IN	SDDM2_OUT	
ADC6	ADC1_CH11	Yes				CMP7_P	LVTTL6_IN		
ADC7	ADC1_CH12	Yes				CMP7_N	LVTTL7_IN	SDDM3_OUT	
ADC8	ADC2_CH9	Yes				CMP9_P	LVTTL8_IN		
ADC9	ADC2_CH10	Yes				CMP9_N	LVTTL9_IN	SDDM4_OUT	
ADC10	ADC2_CH11	Yes					LVTTL10_IN		
ADC11	ADC2_CH12	Yes					LVTTL11_IN		
CM0	ADC0_CH3	Yes		CM0_H		CMP0_P			
CM1	ADC0_CH7	Yes		CM1_H		CMP2_P			
CM2	ADC1_CH3	Yes		CM2_H		CMP4_P			
CM3	ADC1_CH7	Yes		CM3_H		CMP6_P			
CM4	ADC2_CH3	Yes		CM4_H		CMP8_P			
SDD0	ADC0_CH15								SDD0_OUT
SDD1	ADC1_CH15								SDD1_OUT

Notes:

1. *ABPSx_IN: Input to active bipolar prescaler channel x.*
2. *CMx_H/L: Current monitor channel x, high/low side.*
3. *TMx_IO: Temperature monitor channel x.*
4. *CMPx_P/N: Comparator channel x, positive/negative input.*
5. *LVTTLx_IN: LVTTL I/O channel x.*
6. *SDDMx_OUT: Output from sigma-delta DAC MUX channel x.*
7. *SDDx_OUT: Direct output from sigma-delta DAC channel x.*

CS288



Note: Bottom view

Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx.

Pin No.	CS288		
	A2F060 Function	A2F200 Function	A2F500 Function
H19	VCCFPGAIOB1	VCCFPGAIOB1	VCCFPGAIOB1
H21	NC	GDB2/IO33PDB1V0	GDB2/IO42PDB1V0
J1	EMC_DB[4]/IO38NPB5V0	EMC_DB[4]/GEA0/IO61NPB5V0	EMC_DB[4]/GEA0/IO78NPB5V0
J3	EMC_DB[8]/IO40NPB5V0	EMC_DB[8]/GEC0/IO63NPB5V0	EMC_DB[8]/GEC0/IO80NPB5V0
J5	EMC_DB[1]/IO36PDB5V0	EMC_DB[1]/GEB2/IO59PDB5V0	EMC_DB[1]/GEB2/IO76PDB5V0
J6	EMC_DB[6]/IO39NDB5V0	EMC_DB[6]/GEB0/IO62NDB5V0	EMC_DB[6]/GEB0/IO79NDB5V0
J7	VCCFPGAIOB5	VCCFPGAIOB5	VCCFPGAIOB5
J8	VCC	VCC	VCC
J9	GND	GND	GND
J10	VCC	VCC	VCC
J11	GND	GND	GND
J12	VCC	VCC	VCC
J13	GND	GND	GND
J14	VCC	VCC	VCC
J15	VPP	VPP	VPP
J16	NC	IO32NPB1V0	IO41NPB1V0
J17	NC	GNDQ	GNDQ
J19	VCCMAINXTAL	VCCMAINXTAL	VCCMAINXTAL
J21	NC	GDA2/IO33NDB1V0	GDA2/IO42NDB1V0
K1	GND	GND	GND
K3	EMC_DB[5]/IO38PPB5V0	EMC_DB[5]/GEA1/IO61PPB5V0	EMC_DB[5]/GEA1/IO78PPB5V0
K5	EMC_DB[0]/IO36NDB5V0	EMC_DB[0]/GEA2/IO59NDB5V0	EMC_DB[0]/GEA2/IO76NDB5V0
K6	EMC_DB[3]/IO37PPB5V0	EMC_DB[3]/GEC2/IO60PPB5V0	EMC_DB[3]/GEC2/IO77PPB5V0
K8	GND	GND	GND
K9	VCC	VCC	VCC
K10	GND	GND	GND
K11	VCC	VCC	VCC
K12	GND	GND	GND
K13	VCC	VCC	VCC
K14	GND	GND	GND
K16	LPXOUT	LPXOUT	LPXOUT

Notes:

1. *Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.*
2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*

Pin Number	PQ208	
	A2F200	A2F500
125	TMS	TMS
126	TDO	TDO
127	TRSTB	TRSTB
128	VJTAG	VJTAG
129	VDDBAT	VDDBAT
130	VCCLPXTAL	VCCLPXTAL
131	LPXOUT	LPXOUT
132	LPXIN	LPXIN
133	GNDLPXTAL	GNDLPXTAL
134	GNDMAINXTAL	GNDMAINXTAL
135	MAINXOUT	MAINXOUT
136	MAINXIN	MAINXIN
137	VCCMAINXTAL	VCCMAINXTAL
138	GND	GND
139	VCC	VCC
140	VPP	VPP
141	VCCFPGAIOB1	VCCFPGAIOB1
142	GDA0/IO31NDB1V0	GDA0/IO40NDB1V0
143	GDA1/IO31PDB1V0	GDA1/IO40PDB1V0
144	GDC0/IO29NSB1V0	GDC0/IO38NSB1V0
145	GCA0/IO28NDB1V0	GCA0/IO36NDB1V0 *
146	GCA1/IO28PDB1V0	GCA1/IO36PDB1V0 *
147	VCCFPGAIOB1	VCCFPGAIOB1
148	GND	GND
149	VCC	VCC
150	IO25NDB1V0	IO30NDB1V0
151	GCC2/IO25PDB1V0	GBC2/IO30PDB1V0
152	IO23NDB1V0	IO28NDB1V0
153	GCA2/IO23PDB1V0	GCA2/IO28PDB1V0 *
154	GBC2/IO21PSB1V0	GBB2/IO27NDB1V0
155	GBA2/IO20PSB1V0	GBA2/IO27PDB1V0

Notes:

1. *Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.*
2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*

Pin Number	FG484	
	A2F200 Function	A2F500 Function
J19	GCA0/IO28NDB1V0	GCA0/IO36NDB1V0 *
J20	GCA1/IO28PDB1V0	GCA1/IO36PDB1V0 *
J21	GCC1/IO26PPB1V0	GCC1/IO35PPB1V0
J22	GCB1/IO27PDB1V0	GCB1/IO34PDB1V0
K1	GND	GND
K2	EMC_DB[0]/GEA2/IO59NDB5V0	EMC_DB[0]/GEA2/IO76NDB5V0
K3	EMC_DB[1]/GEB2/IO59PDB5V0	EMC_DB[1]/GEB2/IO76PDB5V0
K4	NC	IO74PPB5V0
K5	EMC_DB[2]/IO60NPB5V0	EMC_DB[2]/IO77NPB5V0
K6	NC	IO75PDB5V0
K7	GND	GND
K8	VCC	VCC
K9	GND	GND
K10	VCC	VCC
K11	GND	GND
K12	VCC	VCC
K13	GND	GND
K14	VCC	VCC
K15	GND	GND
K16	VCCFPGAIOB1	VCCFPGAIOB1
K17	NC	IO37NDB1V0
K18	GDA1/IO31PDB1V0	GDA1/IO40PDB1V0
K19	GDA0/IO31NDB1V0	GDA0/IO40NDB1V0
K20	GDC1/IO29PDB1V0	GDC1/IO38PDB1V0
K21	GDC0/IO29NDB1V0	GDC0/IO38NDB1V0
K22	GND	GND
L1	NC	IO73PDB5V0
L2	NC	IO73NDB5V0
L3	NC	IO72PPB5V0
L4	GND	GND
L5	NC	IO74NPB5V0
L6	NC	IO75NDB5V0
L7	VCCFPGAIOB5	VCCFPGAIOB5
L8	GND	GND

Notes:

1. *Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.*
2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*

Revision	Changes	Page
Revision 6 (continued)	Dynamic power values were updated in the following tables. The table subtitles changed where FPGA I/O banks were involved to note "I/O assigned to EMC I/O pins" (SAR 30987). Table 2-10 • Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings Table 2-13 • Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings.	2-10 2-11
	The "Timing Model" was updated (SAR 30986).	2-19
	Values in the timing tables for the following sections were updated. Table subtitles were updated for FPGA I/O banks to note "I/O assigned to EMC I/O pins" (SAR 30986). "Overview of I/O Performance" section: Table 2-24, Table 2-25 "Detailed I/O DC Characteristics" section: Table 2-38, Table 2-39, Table 2-40, Table 2-44, Table 2-45, Table 2-46, Table 2-50, Table 2-51, Table 2-52, Table 2-56, Table 2-57, Table 2-58, Table 2-61, Table 2-62 "LVDS" section: Table 2-65 "LVPECL" section: Table 2-68 "Global Tree Timing Characteristics" section: Table 2-80, Table 2-81	2-23 2-26 2-40 2-42 2-59
	The "PQ208" section and pin tables are new (SAR 31005).	5-34
	Global clocks were removed from the A2F060 pin table for the "CS288" and "FG256" packages, resulting in changed function names for affected pins (SAR 31033).	5-43
Revision 5 (December 2010)	Table 2-2 • Analog Maximum Ratings was revised. The recommended CM[n] pad voltage (relative to ground) was changed from –11 to –0.3 (SAR 28219).	2-2
	Table 2-7 • Temperature and Voltage Derating Factors for Timing Delays was revised to change the values for 100ºC.	2-9
	Power-down and Sleep modes, and all associated notes, were removed from Table 2-8 • Power Supplies Configuration (SAR 29479). IDC3 and IDC4 were renamed to IDC1 and IDC2 (SAR 29478). These modes are no longer supported. A note was added to the table stating that current monitors and temperature monitors should not be used when Power-down and/or Sleep mode are required by the application.	2-10
	The "Power-Down and Sleep Mode Implementation" section was deleted (SAR 29479).	N/A
	Values for PAC9 and PAC10 for LVDS and LVPECL were revised in Table 2-10 • Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings and Table 2-12 • Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings*.	2-10, 2-11
	Values for PAC1 through PAC4, PDC1, and PDC2 were added for A2F500 in Table 2-14 • Different Components Contributing to Dynamic Power Consumption in SmartFusion cSoCs and Table 2-15 • Different Components Contributing to the Static Power Consumption in SmartFusion cSoCs	2-12, 2-13
	The equation for "Total Dynamic Power Consumption—P_{DYN}" in "SoC Mode" was revised to add P_{MSS}. The "Microcontroller Subsystem Dynamic Contribution—P_{MSS}" section is new (SAR 29462).	2-14, 2-18
	Information in Table 2-24 • Summary of I/O Timing Characteristics—Software Default Settings (applicable to FPGA I/O banks) and Table 2-25 • Summary of I/O Timing Characteristics—Software Default Settings (applicable to MSS I/O banks) was updated.	2-25