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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details	
Product Status	Obsolete
Architecture	MCU, FPGA
Core Processor	ARM® Cortex®-M3
Flash Size	128KB
RAM Size	16KB
Peripherals	DMA, POR, WDT
Connectivity	EBI/EMI, I²C, SPI, UART/USART
Speed	80MHz
Primary Attributes	ProASIC®3 FPGA, 60K Gates, 1536D-Flip-Flops
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	288-TFBGA, CSPBGA
Supplier Device Package	288-CSP (11x11)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/a2f060m3e-csg288

SmartFusion cSoC Family Product Table

FPGA Fabric	A2F060			A2F200				A2F500			
	TQ144	CS288	FG256	PQ208	CS288	FG256	FG484	PQ208	CS288	FG256	FG484
System Gates	60,000			200,000				500,000			
Tiles (D-flip-flops)	1,536			4,608				11,520			
RAM Blocks (4,608 bits)	8			8				24			
Microcontroller Subsystem (MSS)	**A2F060**			**A2F200**				**A2F500**			
	TQ144	CS288	FG256	PQ208	CS288	FG256	FG484	PQ208	CS288	FG256	FG484
Flash (Kbytes)	128			256				512			
SRAM (Kbytes)	16			64				64			
Cortex-M3 processor with MPU	Yes			Yes				Yes			
10/100 Ethernet MAC	No			Yes				Yes			
External Memory Controller (EMC)	–	26-/16-bit address/data		26-bit address,16-bit data				–	26-/16-bit address/data		
DMA	8 Ch			8 Ch				8 Ch			
I^2C	2			2				2			
SPI	1	2		1	2			1	2		
16550 UART	2			2				2			
32-Bit Timer	2			2				2			
PLL	1			1				1	2	1	2
32 KHz Low Power Oscillator	1			1				1			
100 MHz On-Chip RC Oscillator	1			1				1			
Main Oscillator (32 KHz to 20 MHz)	1			1				1			
Programmable Analog	**A2F060**			**A2F200**				**A2F500**			
	TQ144	CS288	FG256	PQ208	CS288	FG256	FG484	PQ208	CS288	FG256	FG484
ADCs (8-/10-/12-bit SAR)	1			2				2			3
DACs (8-/16-/24-bit sigma-delta)	1			2				2			3
Signal Conditioning Blocks (SCBs)	1			4				4			5
Comparator*	2			8				8			10
Current Monitors*	1			4				4			5
Temperature Monitors*	1			4				4			5
Bipolar High Voltage Monitors*	2			8				8			10

*Note: *These functions share I/O pins and may not all be available at the same time. See the "Analog Front-End Overview" section in the http://www.microsemi.com/index.php?option=com_docman&task=doc_download&gid=130925 for details.*

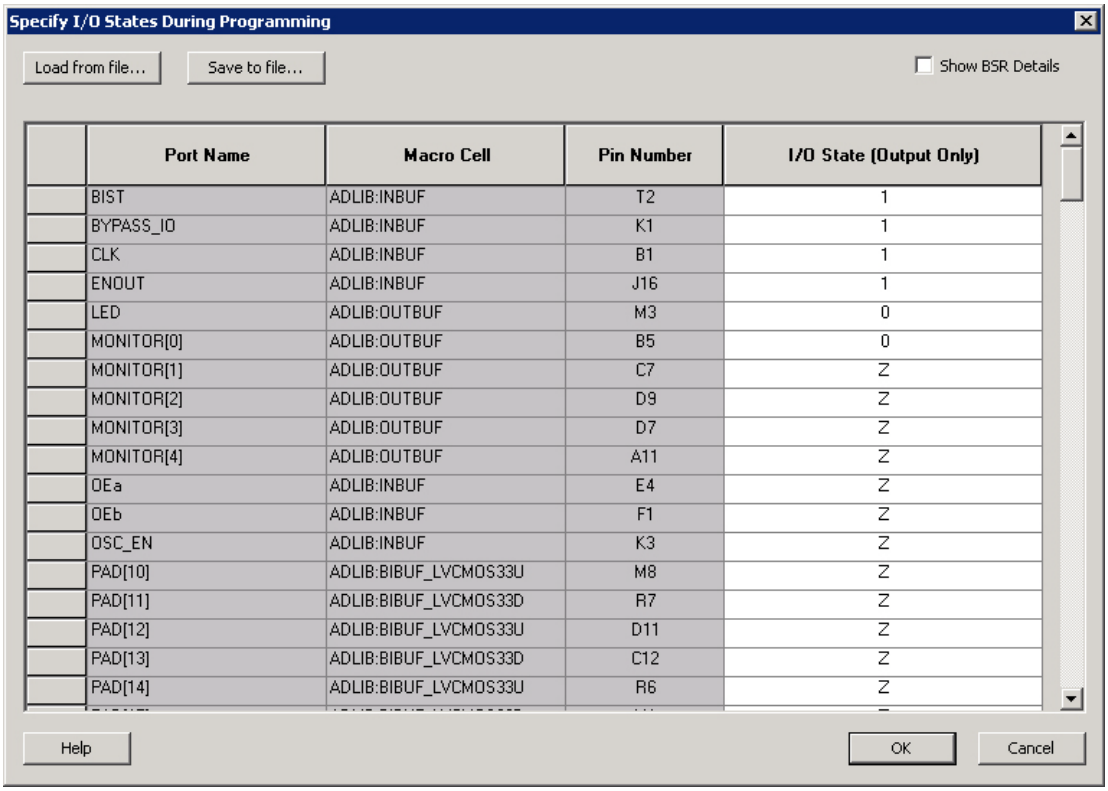


Figure 1-1 • **I/O States During Programming Window**

6. Click OK to return to the FlashPoint – Programming File Generator window.

Note: I/O States During programming are saved to the ADB and resulting programming files after completing programming file generation.

2 – SmartFusion DC and Switching Characteristics

General Specifications

Operating Conditions

Stresses beyond the operating conditions listed in Table 2-1 may cause permanent damage to the device.

Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Absolute Maximum Ratings are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the Recommended Operating Conditions specified in Table 2-3 on page 2-3 is not implied.

Table 2-1 • **Absolute Maximum Ratings**

Symbol	Parameter	Limits	Units
VCC	DC core supply voltage	–0.3 to 1.65	V
VJTAG	JTAG DC voltage	–0.3 to 3.75	V
VPP	Programming voltage	–0.3 to 3.75	V
VCCPLLx	Analog power supply (PLL)	–0.3 to 1.65	V
VCCFPGAIOBx	DC FPGA I/O buffer supply voltage	–0.3 to 3.75	V
VCCMSSIOBx	DC MSS I/O buffer supply voltage	–0.3 to 3.75	V
VI	I/O input voltage	–0.3 V to 3.6 V (when I/O hot insertion mode is enabled) –0.3 V to (VCCxxxxIOBx + 1 V) or 3.6 V, whichever voltage is lower (when I/O hot-insertion mode is disabled)	V
VCC33A	Analog clean 3.3 V supply to the analog circuitry	–0.3 to 3.75	V
VCC33ADCx	Analog 3.3 V supply to ADC	–0.3 to 3.75	V
VCC33AP	Analog clean 3.3 V supply to the charge pump	–0.3 to 3.75	V
VCC33SDDx	Analog 3.3 V supply to the sigma-delta DAC	–0.3 to 3.75	V
VAREFx	Voltage reference for ADC	1.0 to 3.75	V
VCCRCOSC	Analog supply to the integrated RC oscillator	–0.3 to 3.75	V
VDDBAT	External battery supply	–0.3 to 3.75	V
VCCMAINXTAL	Analog supply to the main crystal oscillator	–0.3 to 3.75	V
VCCLPXTAL	Analog supply to the low power 32 kHz crystal oscillator	–0.3 to 3.75	V
VCCENVM	Embedded nonvolatile memory supply	–0.3 to 1.65	V
VCCESRAM	Embedded SRAM supply	–0.3 to 1.65	V
VCC15A	Analog 1.5 V supply to the analog circuitry	–0.3 to 1.65	V
VCC15ADCx	Analog 1.5 V supply to the ADC	–0.3 to 1.65	V
T_{STG}[1]	Storage temperature	–65 to +150	°C
T_J[1]	Junction temperature	125	°C

Notes:

1. *For flash programming and retention maximum limits, refer to Table 2-4 on page 2-4. For recommended operating conditions, refer to Table 2-3 on page 2-3.*
2. *The device should be operated within the limits specified by the datasheet. During transitions, the input signal may undershoot or overshoot according to the limits shown in Table 2-5 on page 2-4.*

Table 2-14 • Different Components Contributing to Dynamic Power Consumption in SmartFusion cSoCs

Parameter	Definition	Power Supply		Device			Units
		Name	Domain	A2F060	A2F200	A2F500	
PAC24	Current Monitor Power Contribution	See Table 2-93 on page 2-78	–	1.03			mW
PAC25	ABPS Power Contribution	See Table 2-96 on page 2-82	–	0.70			mW
PAC26	Sigma-Delta DAC Power Contribution[2]	See Table 2-98 on page 2-85	–	0.58			mW
PAC27	Comparator Power Contribution	See Table 2-97 on page 2-84	–	1.02			mW
PAC28	Voltage Regulator Power Contribution[3]	See Table 2-99 on page 2-87	–	36.30			mW

Notes:

1. *For a different use of MSS peripherals and resources, refer to SmartPower.*
2. *Assumes Input = Half Scale Operation mode.*
3. *Assumes 100 mA load on 1.5 V domain.*

Table 2-15 • Different Components Contributing to the Static Power Consumption in SmartFusion cSoCs

Parameter	Definition	Power Supply		Device			Units
		Name	Domain	A2F060	A2F200	A2F200	
PDC1	Core static power contribution in SoC mode	VCC	1.5 V	11.10	23.70	37.95	mW
PDC2	Device static power contribution in Standby Mode	See Table 2-8 on page 2-10	–	11.10	23.70	37.95	mW
PDC3	Device static power contribution in Time Keeping mode	See Table 2-8 on page 2-10	3.3 V	33.00	33.00	33.00	µW
PDC7	Static contribution per input pin (standard dependent contribution)	VCCxxxxIOBx/VCC	See Table 2-10 and Table 2-11 on page 2-11.				
PDC8	Static contribution per output pin (standard dependent contribution)	VCCxxxxIOBx/VCC	See Table 2-12 and Table 2-13 on page 2-11.				
PDC9	Static contribution per PLL	VCC	1.5 V	2.55	2.55	2.55	mW

Table 2-16 • eNVM Dynamic Power Consumption

Parameter	Description	Condition	Min.	Typ.	Max.	Units
eNVM System	eNVM array operating power	Idle		795		µA
		Read operation	See Table 2-14 on page 2-12.			
		Erase		900		µA
		Write		900		µA
PNVMCTRL	eNVM controller operating power			20		µW/MHz

Table 2-63 • LVDS Minimum and Maximum DC Input and Output Levels

DC Parameter	Description	Min.	Typ.	Max.	Units
VCCFPGAIOBx	Supply voltage	2.375	2.5	2.625	V
VOL	Output low voltage	0.9	1.075	1.25	V
VOH	Output high voltage	1.25	1.425	1.6	V
I_{OL}[1]	Output lower current	0.65	0.91	1.16	mA
I_{OH}[1]	Output high current	0.65	0.91	1.16	mA
VI	Input voltage	0		2.925	V
I_{IH}[2]	Input high leakage current			15	µA
I_{IL}[2]	Input low leakage current			15	µA
V_{ODIFF}	Differential output voltage	250	350	450	mV
V_{OCM}	Output common mode voltage	1.125	1.25	1.375	V
V_{ICM}	Input common mode voltage	0.05	1.25	2.35	V
V_{IDIFF}	Input differential voltage	100	350		mV

Notes:

1. *I_{OL}/I_{OH} defined by V_{ODIFF}/(resistor network).*
2. *Currents are measured at 85°C junction temperature.*

Table 2-64 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	V_{REF} (typ.) (V)
1.075	1.325	Cross point	–

* *Measuring point = V_{trip}. See Table 2-22 on page 2-24 for a complete table of trip points.*

Timing Characteristics

Table 2-65 • LVDS
Worst Commercial-Case Conditions: T_J = 85°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCFPGAIOBx = 2.3 V
Applicable to FPGA I/O Banks, I/O Assigned to EMC I/O Pins

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	Units
Std.	0.60	1.83	0.04	1.87	ns
–1	0.50	1.53	0.03	1.55	ns

Notes:

1. *For the derating values at specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.*
2. *The above mentioned timing parameters correspond to 24mA drive strength.*

Input Register

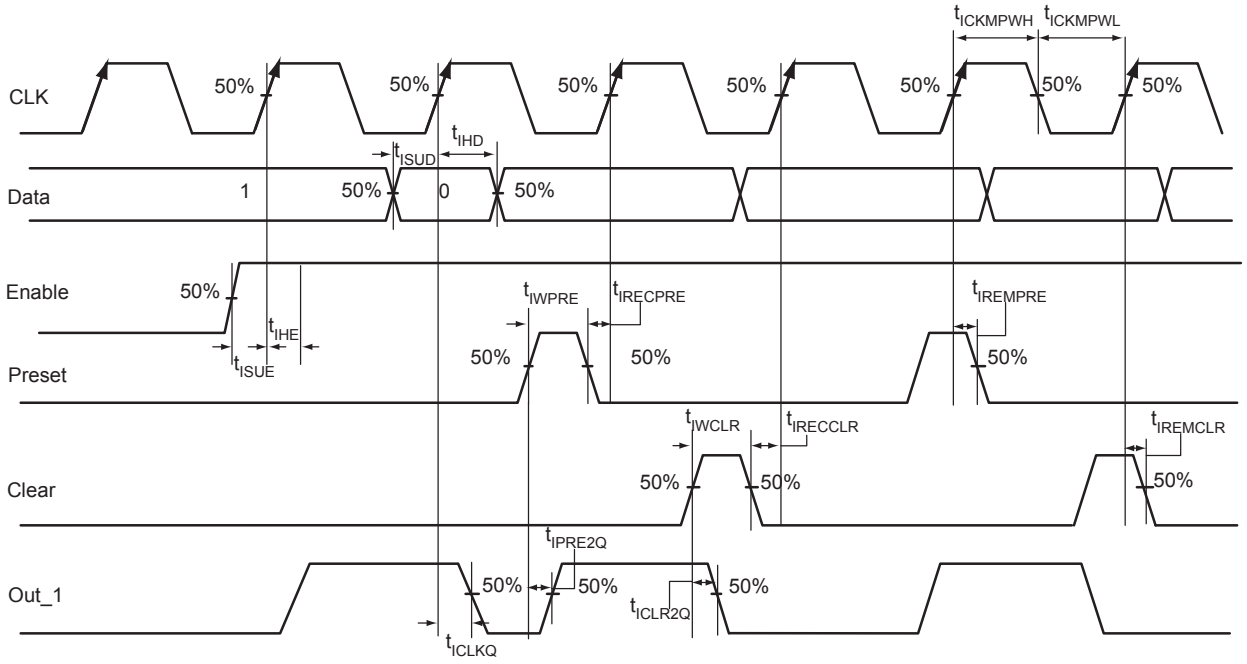


Figure 2-16 • **Input Register Timing Diagram**

Timing Characteristics

Table 2-71 • **Input Data Register Propagation Delays**
Worst Commercial-Case Conditions: T_J = 85°C, Worst-Case VCC = 1.425 V

Parameter	Description	–1	Std.	Units
t_{ICLKQ}	Clock-to-Q of the Input Data Register	0.24	0.29	ns
t_{ISUD}	Data Setup Time for the Input Data Register	0.27	0.32	ns
t_{IHD}	Data Hold Time for the Input Data Register	0.00	0.00	ns
t_{ISUE}	Enable Setup Time for the Input Data Register	0.38	0.45	ns
t_{IHE}	Enable Hold Time for the Input Data Register	0.00	0.00	ns
t_{ICLR2Q}	Asynchronous Clear-to-Q of the Input Data Register	0.46	0.55	ns
t_{IPRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	0.46	0.55	ns
$t_{IREMCLR}$	Asynchronous Clear Removal Time for the Input Data Register	0.00	0.00	ns
$t_{IRECCLR}$	Asynchronous Clear Recovery Time for the Input Data Register	0.23	0.27	ns
$t_{IREMPRE}$	Asynchronous Preset Removal Time for the Input Data Register	0.00	0.00	ns
$t_{IRECPRE}$	Asynchronous Preset Recovery Time for the Input Data Register	0.23	0.27	ns
t_{IWCLR}	Asynchronous Clear Minimum Pulse Width for the Input Data Register	0.22	0.22	ns
t_{IWPRE}	Asynchronous Preset Minimum Pulse Width for the Input Data Register	0.22	0.22	ns
$t_{ICKMPWH}$	Clock Minimum Pulse Width High for the Input Data Register	0.36	0.36	ns
$t_{ICKMPWL}$	Clock Minimum Pulse Width Low for the Input Data Register	0.32	0.32	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.

Output DDR Module

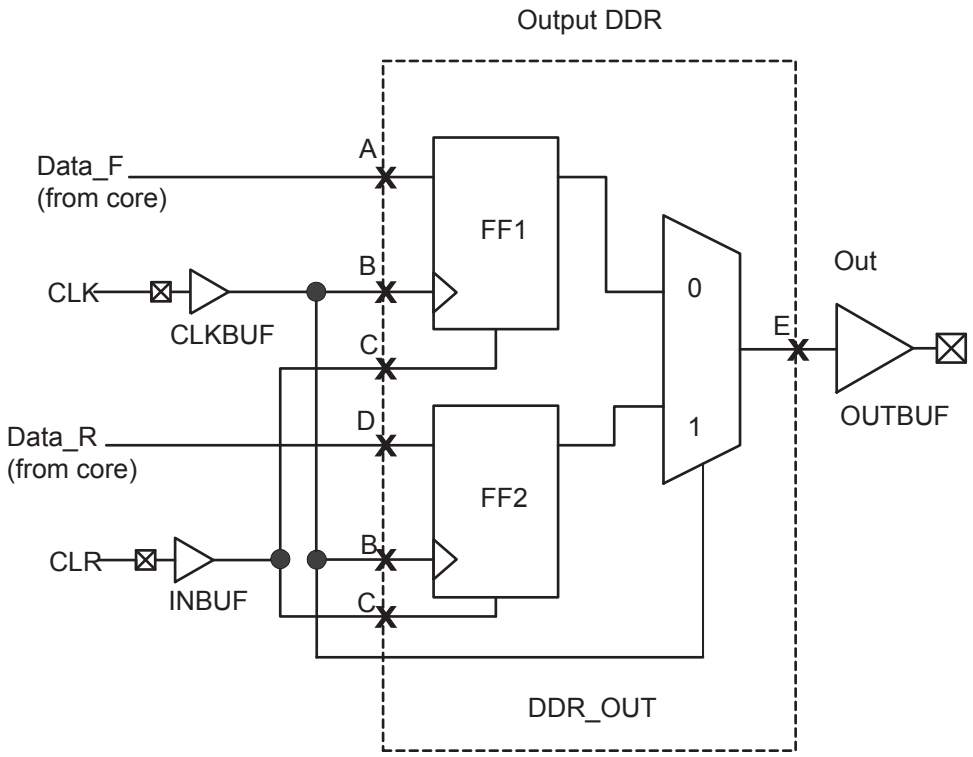


Figure 2-21 • **Output DDR Timing Model**

Table 2-76 • **Parameter Definitions**

Parameter Name	Parameter Definition	Measuring Nodes (from, to)
$t_{DDROCLKQ}$	Clock-to-Out	B, E
$t_{DDROCLR2Q}$	Asynchronous Clear-to-Out	C, E
$t_{DDROREMCLR}$	Clear Removal	C, B
$t_{DDRORECCLR}$	Clear Recovery	C, B
$t_{DDROSUD1}$	Data Setup Data_F	A, B
$t_{DDROSUD2}$	Data Setup Data_R	D, B
$t_{DDROHD1}$	Data Hold Data_F	A, B
$t_{DDROHD2}$	Data Hold Data_R	D, B

Timing Characteristics

Table 2-80 • A2F500 Global Resource
Worst Commercial-Case Conditions: T_J = 85°C, VCC = 1.425 V

Parameter	Description	–1		Std.		Units
		Min.[1]	Max.[2]	Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	1.54	1.73	1.84	2.08	ns
t_{RCKH}	Input High Delay for Global Clock	1.53	1.76	1.84	2.12	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	0.85		1.00		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	0.85		1.00		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.23		0.28	ns

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage-supply levels, refer to Table 2-7 on page 2-9 for derating values.*

Table 2-81 • A2F200 Global Resource
Worst Commercial-Case Conditions: T_J = 85°C, VCC = 1.425 V

Parameter	Description	–1		Std.		Units
		Min.[1]	Max.[2]	Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	0.74	0.99	0.88	1.19	ns
t_{RCKH}	Input High Delay for Global Clock	0.76	1.05	0.91	1.26	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	0.85		1.00		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	0.85		1.00		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.29		0.35	ns

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage-supply levels, refer to Table 2-7 on page 2-9 for derating values.*

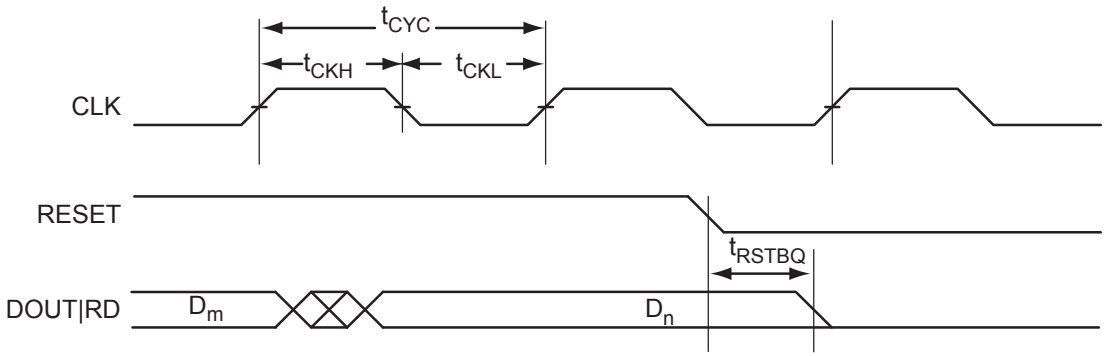


***Figure 2-34* • RAM Reset. Applicable to both RAM4K9 and RAM512x18.**

FIFO

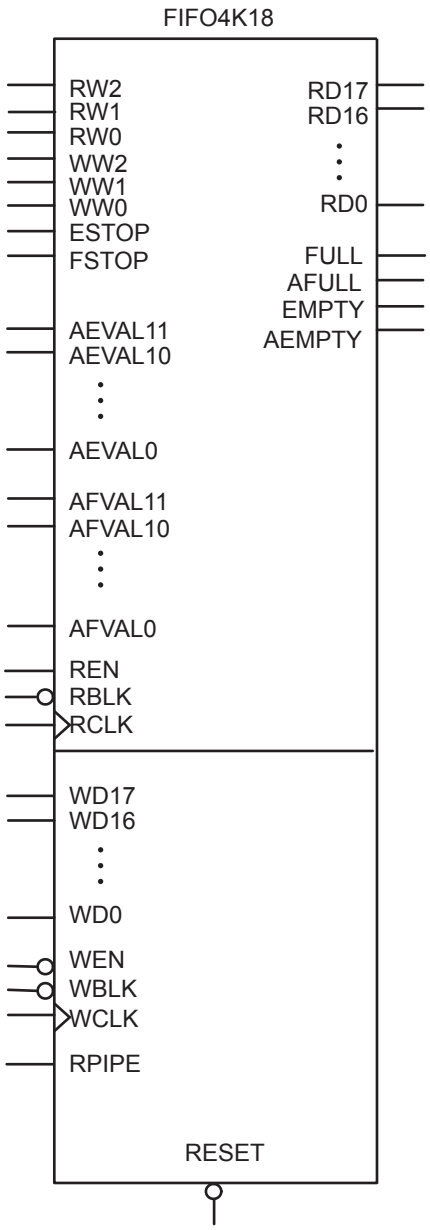


Figure 2-35 • **FIFO Model**

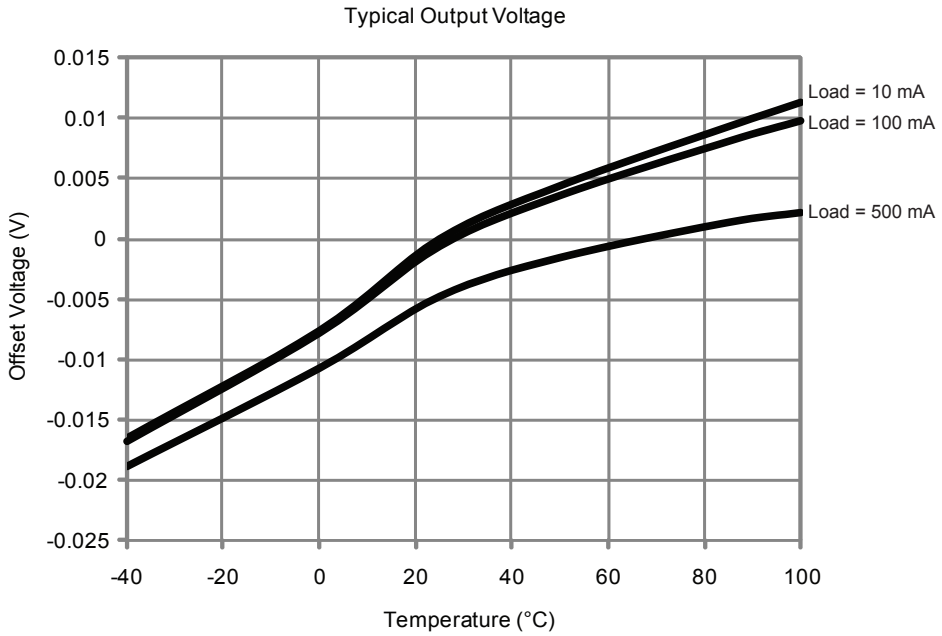


Figure 2-45 • **Typical Output Voltage**

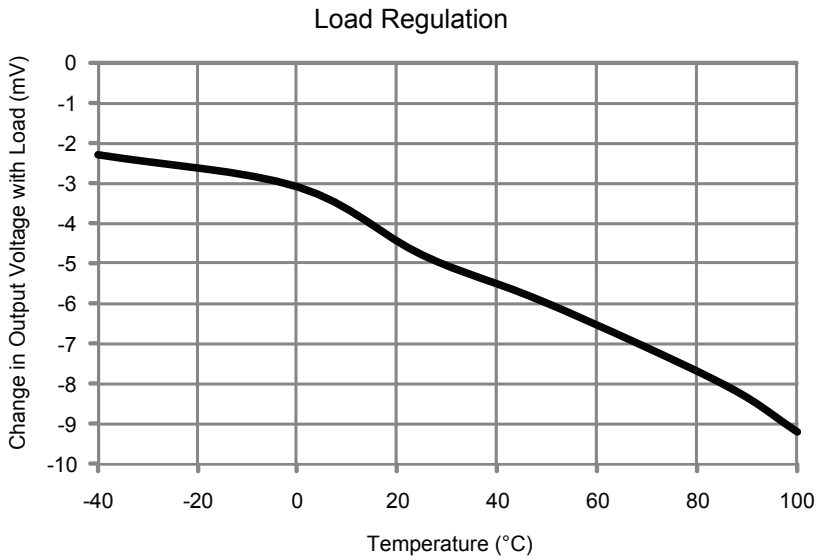


Figure 2-46 • **Load Regulation**

Table 2-100 • SPI Characteristics
Commercial Case Conditions: T_J = 85ºC, VDD = 1.425 V, –1 Speed Grade (continued)

Symbol	Description and Condition	A2F060	A2F200	A2F500	Unit
sp6	Data from master (SPI_x_DO) setup time [2]	1	1	1	pclk cycles
sp7	Data from master (SPI_x_DO) hold time [2]	1	1	1	pclk cycles
sp8	SPI_x_DI setup time [2]	1	1	1	pclk cycles
sp9	SPI_x_DI hold time [2]	1	1	1	pclk cycles

Notes:

1. *These values are provided for a load of 35 pF. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website: http://www.microsemi.com/index.php?option=com_microsemi&Itemid=489&lang=en&view=salescontact.*
2. *For allowable pclk configurations, refer to the Serial Peripheral Interface Controller section in the SmartFusion Microcontroller Subsystem User's Guide.*

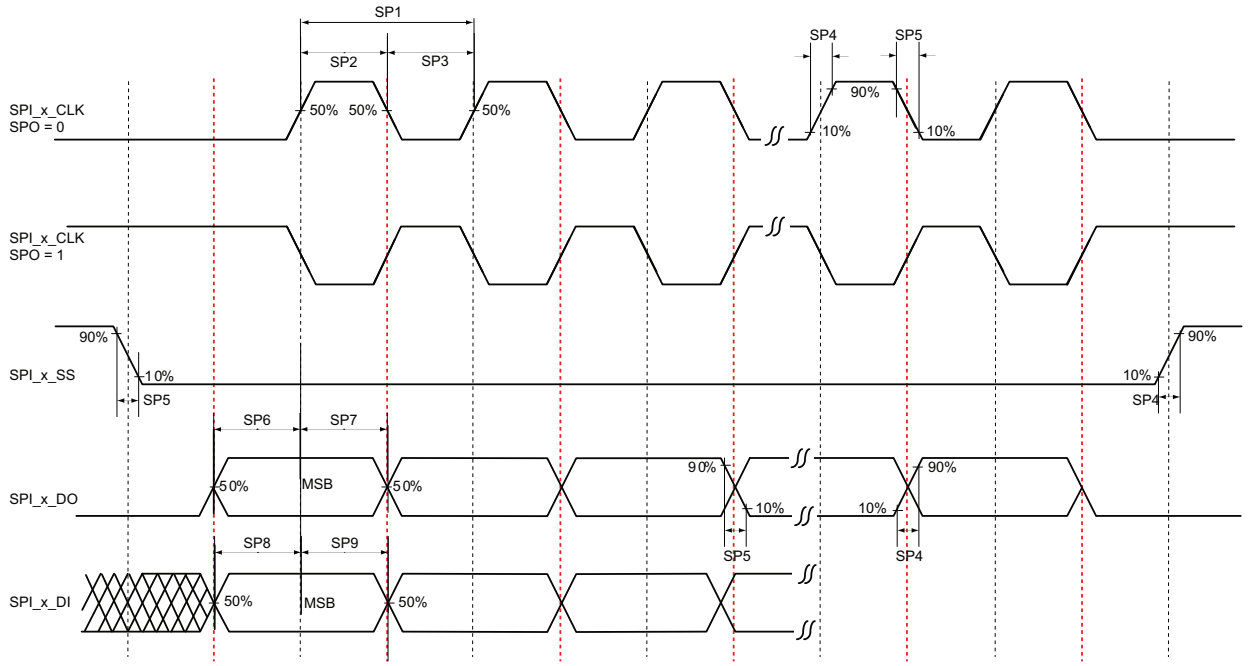


Figure 2-47 • SPI Timing for a Single Frame Transfer in Motorola Mode (SPH = 1)

Emcraft Systems provides porting of the open-source U-boot firmware and uClinux™ kernel to the SmartFusion cSoC, a Linux®-based cross-development framework, and other complementary components. Combined with the release of its A2F-Linux Evaluation Kit, this provides a low-cost platform for evaluation and development of Linux (uClinux) on the Cortex-M3 CPU core of the Microsemi SmartFusion cSoC.

- Emcraft Linux on Microsemi's SmartFusion cSoC

Keil offers the RTX Real-Time Kernel as a royalty-free, deterministic RTOS designed for ARM and Cortex-M devices. It allows you to create programs that simultaneously perform multiple functions and helps to create applications which are better structured and more easily maintained.

- The RTX Real-Time Kernel is included with MDK-ARM. Download the Evaluation version of Keil MDK-ARM.
- RTX source code is available as part of Keil/ARM Real-Time Library (RL-ARM), a group of tightly-coupled libraries designed to solve the real-time and communication challenges of embedded systems based on ARM-powered microcontroller devices. The RL-ARM library now supports SmartFusion cSoCs and designers with additional key features listed in the "Middleware" section on page 3-5.

Micrium supports SmartFusion cSoCs with the company's flagship µC/OS family, recognized for a variety of features and benefits, including unparalleled reliability, performance, dependability, impeccable source code and vast documentation. Micrium supports the following products for SmartFusion cSoCs and continues to work with Microsemi on additional projects.

- SmartFusion Quickstart Guide for Micrium µC/OS-III Examples
  - Design Files

µC/OS-III™, Micrium's newest RTOS, is designed to save time on your next embedded project and puts greater control of the software in your hands.

RoweBots provides an ultra tiny Linux-compatible RTOS called Unison for SmartFusion. Unison consists of a set of modular software components, which, like Linux, are either free or commercially licensed. Unison offers POSIX® and Linux compatibility with hard real-time performance, complete I/O modules and an easily understood environment for device driver programming. Seamless integration with FPGA and analog features are fast and easy.

- Unison V4-based products include a free Unison V4 Linux and POSIX-compatible kernel with serial I/O, file system, six demonstration programs, upgraded documentation and source code for Unison V4, and free (for non-commercial use) Unison V4 TCP/IP server. Commercial license upgrade is available for Unison V4 TCP/IP server with three demonstration programs, DHCP client and source code.
- Unison V5-based products include commercial Unison V5 Linux- and POSIX-compatible kernel with serial I/O, file system, extensive feature set, full documentation, source code and more than 20 demonstration programs, Unison V5 TCP/IPv4 with extended feature set, sockets interface, multiple network interfaces, PPP support, DHCP client, documentation, source code and six demonstration programs, and multiple other features.

Middleware

Microsemi has ported both uIP and lwIP for Ethernet support as well as including TFTP file service.

- SmartFusion Webserver Demo Using uIP and FreeRTOS
- SmartFusion: Running Webserver, TFTP on lwIP TCP/IP Stack Application Note

The Keil/ARM Real-Time Library (RL-ARM)[1], in addition to RTX source, includes the following:

- RL-TCPnet (TCP/IP) – The Keil RL-TCPnet library, supporting full TCP/IP and UDP protocols, is a full networking suite specifically written for small ARM and Cortex-M processor-based microcontrollers. TCPnet is now ported to and supports SmartFusion Cortex-M3. It is highly optimized, has a small code footprint, and gives excellent performance, providing a wide range of application level protocols and examples such as FTP, SNMP, SOAP and AJAX. An HTTP server example of TCPnet working in a SmartFusion design is available.

1. The CAN and USB functions within RL-ARM are not supported for SmartFusion cSoC.

User-Defined Supply Pins

Name	Type	Polarity/ Bus Size	Description
VAREF0	Input	1	Analog reference voltage for first ADC. The SmartFusion cSoC can be configured to generate a 2.56 V internal reference that can be used by the ADC. While using the internal reference, the reference voltage is output on the VAREFOUT pin for use as a system reference. If a different reference voltage is required, it can be supplied by an external source and applied to this pin. The valid range of values that can be supplied to the ADC is 1.0 V to 3.3 V. When VAREF0 is internally generated, a bypass capacitor must be connected from this pin to ground. The value of the bypass capacitor should be between 3.3 µF and 22 µF, which is based on the needs of the individual designs. The choice of the capacitor value has an impact on the settling time it takes the VAREF0 signal to reach the required specification of 2.56 V to initiate valid conversions by the ADC. If the lower capacitor value is chosen, the settling time required for VAREF0 to achieve 2.56 V will be shorter than when selecting the larger capacitor value. The above range of capacitor values supports the accuracy specification of the ADC, which is detailed in the datasheet. Designers choosing the smaller capacitor value will not obtain as much margin in the accuracy as that achieved with a larger capacitor value. See the Analog-to-Digital Converter (ADC) section in the *SmartFusion Programmable Analog User's Guide* for more information. The SoC Products Group recommends customers use 10 µF as the value of the bypass capacitor. Designers choosing to use an external VAREF0 need to ensure that a stable and clean VAREF0 source is supplied to the VAREF0 pin before initiating conversions by the ADC. To use the internal voltage reference, the VAREFOUT pin must be connected to the appropriate ADC VAREFx input on the PCB. For example, VAREFOUT can be connected to VAREF0 only, if ADC0 alone is used. VAREFOUT can be connected to VAREF1 only, if ADC1 alone is used. VAREFOUT can be connected to VAREF2 only, if ADC2 alone is used. VAREFOUT can be connected to VAREF0, VAREF1 and VAREF2 together, if ADC0, ADC1, and ADC2 all are used.
VAREF1	Input	1	Analog reference voltage for second ADC See "VAREF0" above for more information.
VAREF2	Input	1	Analog reference voltage for third ADC See "VAREF0" above for more.
VAREFOUT	Out	1	Internal 2.56 V voltage reference output. Can be used to provide the two ADCs with a unique voltage reference externally by connecting VAREFOUT to both VAREF0 and VAREF1. To use the internal voltage reference, you must connect the VAREFOUT pin to the appropriate ADC VAREFx input—either the VAREF0 or VAREF1 pin—on the PCB.

***Table 5-1* • Recommended Tie-Off Values for the TCK and TRST Pins**

VJTAG	Tie-Off Resistance[1, 2]
VJTAG at 3.3 V	200 Ω to 1 kΩ
VJTAG at 2.5 V	200 Ω to 1 kΩ
VJTAG at 1.8 V	500 Ω to 1 kΩ
VJTAG at 1.5 V	500 Ω to 1 kΩ

Notes:

1. *The TCK pin can be pulled up/down.*
2. *The TRST pin can only be pulled down.*

1. *Equivalent parallel resistance if more than one device is on JTAG chain.*

***Table 5-2* • Relationships Between Signals in the Analog Front-End**

Pin	ADC Channel	Dir.-In Option	Prescaler	Current Mon.	Temp. Mon.	Compar.	LVTTL	SDD MUX	SDD
SDD2	ADC2_CH15								SDD2_OUT
TM0	ADC0_CH4	Yes		CM0_L	TM0_IO	CMP0_N			
TM1	ADC0_CH8	Yes		CM1_L	TM1_IO	CMP2_N			
TM2	ADC1_CH4	Yes		CM2_L	TM2_IO	CMP4_N			
TM3	ADC1_CH8	Yes		CM3_L	TM3_IO	CMP6_N			
TM4	ADC2_CH4	Yes		CM4_L	TM4_IO	CMP8_N			

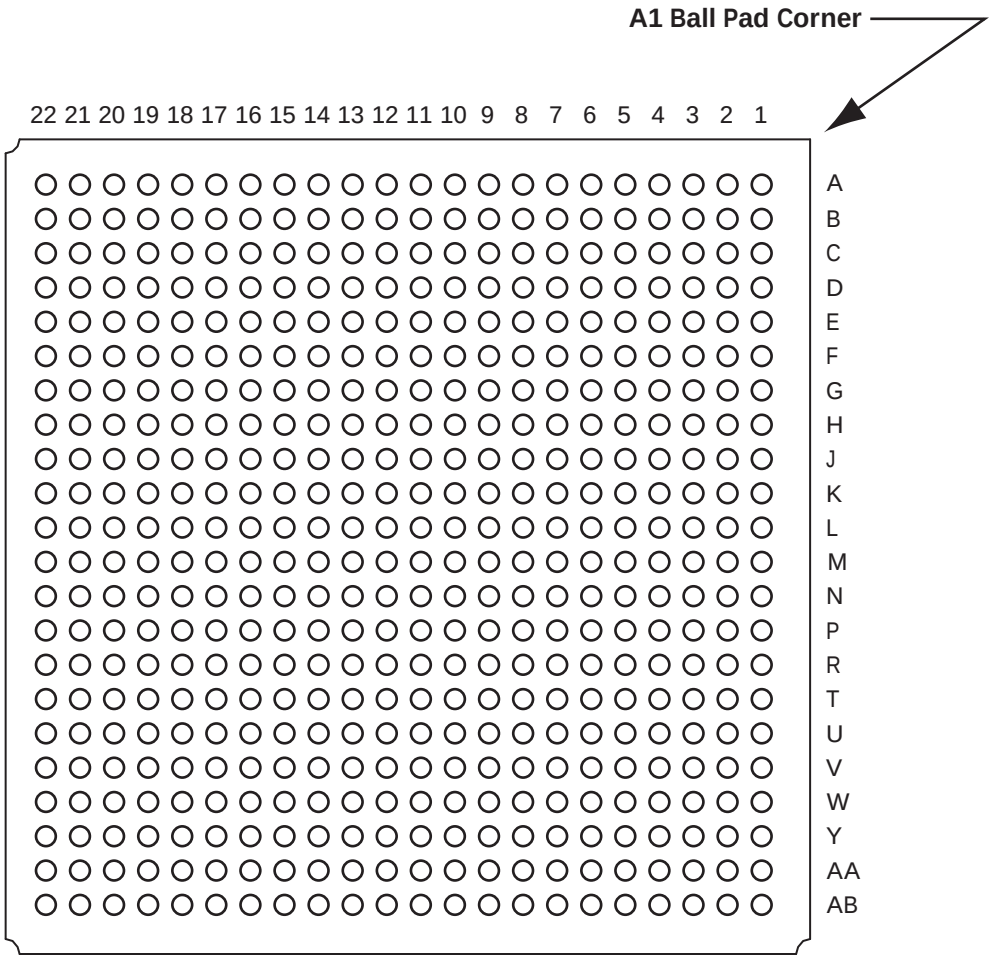
Notes:

1. *ABPSx_IN: Input to active bipolar prescaler channel x.*
2. *CMx_H/L: Current monitor channel x, high/low side.*
3. *TMx_IO: Temperature monitor channel x.*
4. *CMPx_P/N: Comparator channel x, positive/negative input.*
5. *LVTTLx_IN: LVTTL I/O channel x.*
6. *SDDMx_OUT: Output from sigma-delta DAC MUX channel x.*
7. *SDDx_OUT: Direct output from sigma-delta DAC channel x.*

TQ144	
Pin Number	**A2F060 Function**
73	VCC33A
74	PTEM
75	PTBASE
76	SPI_0_DO/GPIO_16
77	SPI_0_DI/GPIO_17
78	SPI_0_CLK/GPIO_18
79	SPI_0_SS/GPIO_19
80	UART_0_RXD/GPIO_21
81	UART_0_TXD/GPIO_20
82	UART_1_RXD/GPIO_29
83	UART_1_TXD/GPIO_28
84	VCC
85	VCCMSSIOB2
86	GND
87	I2C_1_SDA/GPIO_30
88	I2C_1_SCL/GPIO_31
89	I2C_0_SDA/GPIO_22
90	I2C_0_SCL/GPIO_23
91	GNDENVM
92	VCCENVM
93	JTAGSEL
94	TCK
95	TDI
96	TMS
97	TDO
98	TRSTB
99	VJTAG
100	VDDBAT
101	VCCLPXTAL
102	LPXOUT
103	LPXIN
104	GNDLPXTAL
105	GNDMAINXTAL
106	MAINXOUT
107	MAINXIN
108	VCCMAINXTAL

TQ144	
Pin Number	**A2F060 Function**
109	VPP
110	GNDQ
111	GCA1/IO20PDB0V0
112	GCA0/IO20NDB0V0
113	GCB1/IO19PDB0V0
114	GCB0/IO19NDB0V0
115	GCC1/IO18PDB0V0
116	GCC0/IO18NDB0V0
117	VCCFPGAIOB0
118	GND
119	VCC
120	IO14PDB0V0
121	IO14NDB0V0
122	IO13NSB0V0
123	IO11PDB0V0
124	IO11NDB0V0
125	IO09PDB0V0
126	IO09NDB0V0
127	VCCFPGAIOB0
128	GND
129	IO07PDB0V0
130	IO07NDB0V0
131	IO06PDB0V0
132	IO06NDB0V0
133	IO05PDB0V0
134	IO05NDB0V0
135	IO03PDB0V0
136	IO03NDB0V0
137	VCCFPGAIOB0
138	GND
139	VCC
140	IO01PDB0V0
141	IO01NDB0V0
142	IO00PDB0V0
143	IO00NDB0V0
144	GNDQ

FG484



Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx.

Pin Number	FG484	
	A2F200 Function	A2F500 Function
E5	NC	NC
E6	GNDQ	GNDQ
E7	VCCFPGAIOB0	VCCFPGAIOB0
E8	NC	IO00PPB0V0
E9	NC	NC
E10	VCCFPGAIOB0	VCCFPGAIOB0
E11	EMC_AB[4]/IO06NDB0V0	EMC_AB[4]/IO10NDB0V0
E12	EMC_AB[5]/IO06PDB0V0	EMC_AB[5]/IO10PDB0V0
E13	VCCFPGAIOB0	VCCFPGAIOB0
E14	GBC0/IO17NPB0V0	GBC0/IO22NPB0V0
E15	NC	NC
E16	VCCFPGAIOB0	VCCFPGAIOB0
E17	NC	VCOMPLA1
E18	NC	IO25NPB1V0
E19	GND	GND
E20	NC	NC
E21	VCCFPGAIOB1	VCCFPGAIOB1
E22	IO22NDB1V0	IO32NDB1V0
F1	GFB1/IO65PPB5V0	GFB1/IO82PPB5V0
F2	IO67NPB5V0	IO84NPB5V0
F3	GFB2/IO68NDB5V0	GFB2/IO85NDB5V0
F4	EMC_DB[10]/IO69NPB5V0	EMC_DB[10]/IO86NPB5V0
F5	VCCFPGAIOB5	VCCFPGAIOB5
F6	VCCPLL	VCCPLL0
F7	VCOMPLA	VCOMPLA0
F8	NC	NC
F9	NC	NC
F10	NC	NC
F11	NC	NC
F12	NC	NC
F13	EMC_AB[20]/IO14NDB0V0	EMC_AB[20]/IO21NDB0V0
F14	EMC_AB[21]/IO14PDB0V0	EMC_AB[21]/IO21PDB0V0
F15	GNDQ	GNDQ
F16	NC	VCCPLL1

Notes:

1. *Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.*
2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*