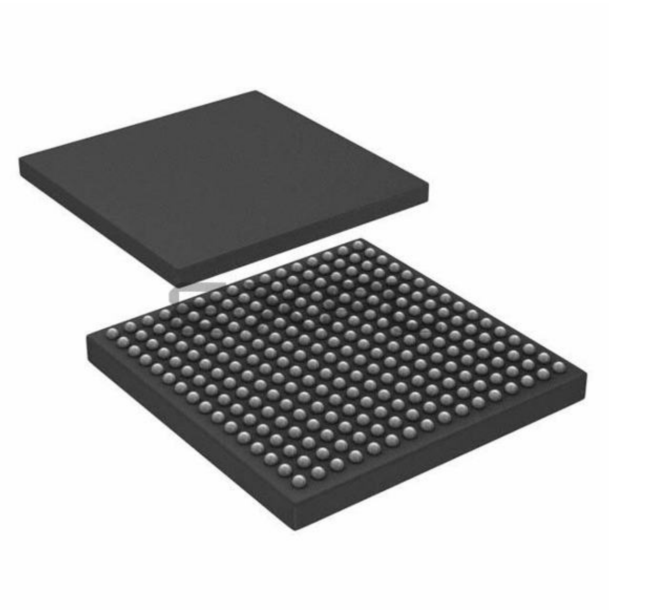

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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details	
Product Status	Obsolete
Architecture	MCU, FPGA
Core Processor	ARM® Cortex®-M3
Flash Size	128KB
RAM Size	16KB
Peripherals	DMA, POR, WDT
Connectivity	EBI/EMI, I²C, SPI, UART/USART
Speed	80MHz
Primary Attributes	ProASIC®3 FPGA, 60K Gates, 1536D-Flip-Flops
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/a2f060m3e-fgg256i

SmartFusion Family Overview

SmartFusion DC and Switching Characteristics

SmartFusion Development Tools

SmartFusion Programming

Pin Descriptions

Datasheet Information

VCCxxxxIOBx Trip Point:
Ramping up: 0.6 V < trip_point_up < 1.2 V
Ramping down: 0.5 V < trip_point_down < 1.1 V

VCC Trip Point:
Ramping up: 0.6 V < trip_point_up < 1.1 V
Ramping down: 0.5 V < trip_point_down < 1 V

VCC and VCCxxxxIOBx ramp-up trip points are about 100 mV higher than ramp-down trip points. This specifically built-in hysteresis prevents undesirable power-up oscillations and current surges. Note the following:

- By default, during programming I/Os become tristated and weakly pulled up to VCCxxxxIOBx. You can modify the I/O states during programming in FlashPro. For more details, refer to "Specifying I/O States During Programming" on page 1-3.
- JTAG supply, PLL power supplies, and charge pump VPUMP supply have no influence on I/O behavior.

PLL Behavior at Brownout Condition

The Microsemi SoC Products Group recommends using monotonic power supplies or voltage regulators to ensure proper power-up behavior. Power ramp-up should be monotonic at least until VCC and VCCPLLx exceed brownout activation levels. The VCC activation level is specified as 1.1 V worst-case (see Figure 2-1 on page 2-6 for more details).

When PLL power supply voltage and/or VCC levels drop below the VCC brownout levels (0.75 V ± 0.25 V), the PLL output lock signal goes low and/or the output clock is lost. Refer to the "Power-Up/-Down Behavior of Low Power Flash Devices" chapter of the *ProASIC3 FPGA Fabric User's Guide* for information on clock and lock recovery.

Internal Power-Up Activation Sequence

1. Core
2. Input buffers

Output buffers, after 200 ns delay from input buffer activation

Power Consumption of Various Internal Resources

***Table 2-14* • Different Components Contributing to Dynamic Power Consumption in SmartFusion cSoCs**

Parameter	Definition	Power Supply		Device			Units
		Name	Domain	A2F060	A2F200	A2F500	
PAC1	Clock contribution of a Global Rib	VCC	1.5 V	3.39	3.40	5.05	µW/MHz
PAC2	Clock contribution of a Global Spine	VCC	1.5 V	1.14	1.83	2.50	µW/MHz
PAC3	Clock contribution of a VersaTile row	VCC	1.5 V	1.15	1.15	1.15	µW/MHz
PAC4	Clock contribution of a VersaTile used as a sequential module	VCC	1.5 V	0.12	0.12	0.12	µW/MHz
PAC5	First contribution of a VersaTile used as a sequential module	VCC	1.5 V	0.07	0.07	0.07	µW/MHz
PAC6	Second contribution of a VersaTile used as a sequential module	VCC	1.5 V	0.29	0.29	0.29	µW/MHz
PAC7	Contribution of a VersaTile used as a combinatorial module	VCC	1.5 V	0.29	0.29	0.29	µW/MHz
PAC8	Average contribution of a routing net	VCC	1.5 V	1.04	0.79	0.79	µW/MHz
PAC9	Contribution of an I/O input pin (standard dependent)	VCCxxxxIOBx/VCC	See Table 2-10 and Table 2-11 on page 2-11				
PAC10	Contribution of an I/O output pin (standard dependent)	VCCxxxxIOBx/VCC	See Table 2-12 and Table 2-13 on page 2-11				
PAC11	Average contribution of a RAM block during a read operation	VCC	1.5 V	25.00			µW/MHz
PAC12	Average contribution of a RAM block during a write operation	VCC	1.5 V	30.00			µW/MHz
PAC13	Dynamic Contribution for PLL	VCC	1.5 V	2.60			µW/MHz
PAC15	Contribution of NVM block during a read operation (F < 33MHz)	VCC	1.5 V	358.00			µW/MHz
PAC16	1st contribution of NVM block during a read operation (F > 33MHz)	VCC	1.5 V	12.88			mW
PAC17	2nd contribution of NVM block during a read operation (F > 33MHz)	VCC	1.5 V	4.80			µW/MHz
PAC18	Main Crystal Oscillator contribution	VCCMAINXTAL	3.3 V	1.98			mW
PAC19a	RC Oscillator contribution	VCCRCOSC	3.3 V	3.30			mW
PAC19b	RC Oscillator contribution	VCC	1.5 V	3.00			mW
PAC20a	Analog Block Dynamic Power Contribution of the ADC	VCC33ADCx	3.3 V	8.25			mW
PAC20b	Analog Block Dynamic Power Contribution of the ADC	VCC15ADCx	1.5 V	3.00			mW
PAC21	Low Power Crystal Oscillator contribution	VCCLPXTAL	3.3 V	33.00			µW
PAC22	MSS Dynamic Power Contribution – Running Drysthone at 100MHz[1]	VCC	1.5 V	67.50			mW
PAC23	Temperature Monitor Power Contribution	See Table 2-94 on page 2-79	–	1.23			mW

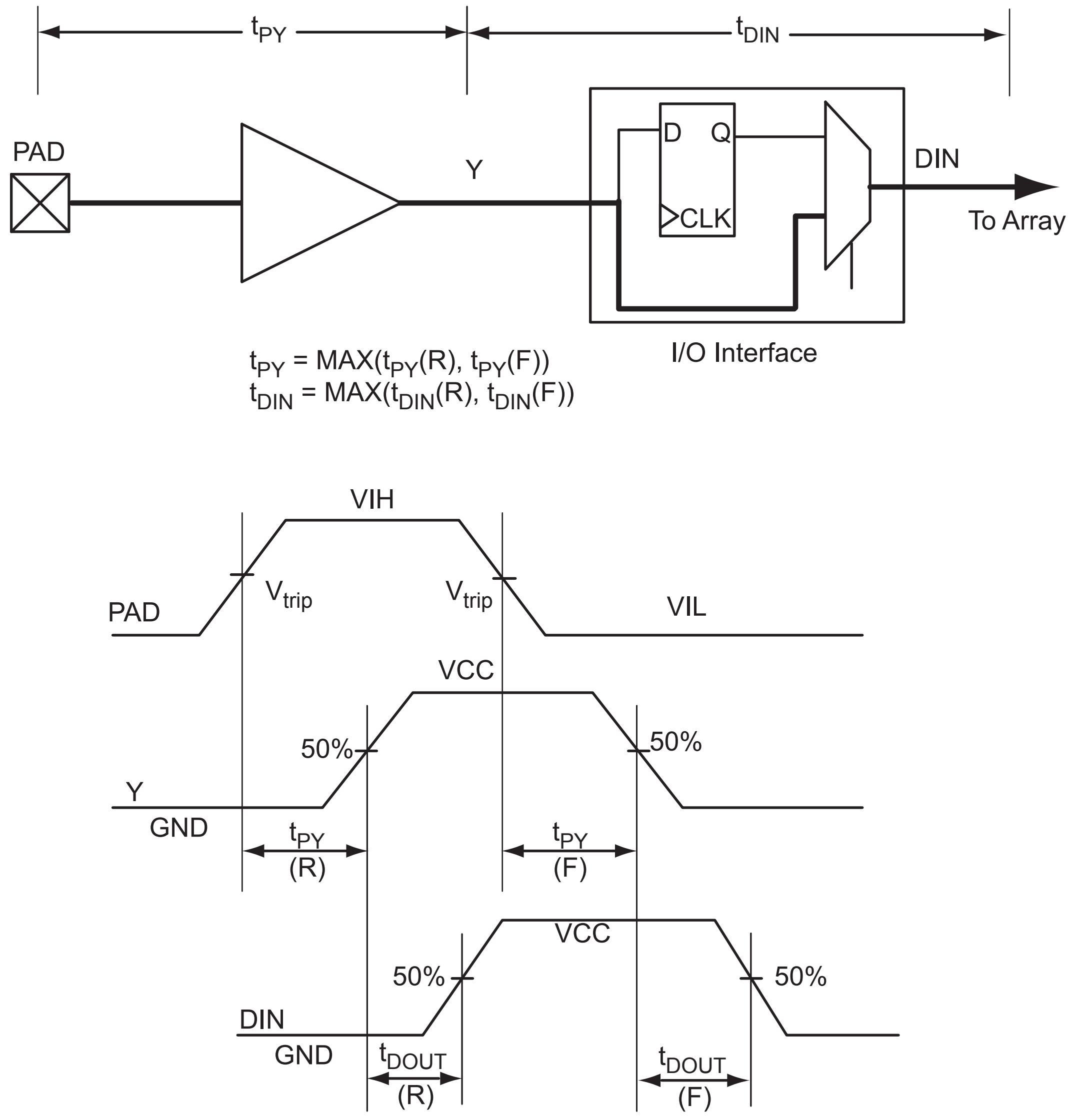


Figure 2-3 • **Input Buffer Timing Model and Delays (example)**

Single-Ended I/O Characteristics

3.3 V LVTTL / 3.3 V LVCMOS

Low-Voltage Transistor–Transistor Logic (LVTTL) is a general-purpose standard (EIA/JESD) for 3.3 V applications. It uses an LVTTL input buffer and push-pull output buffer.

***Table 2-35* • Minimum and Maximum DC Input and Output Levels Applicable to FPGA I/O Banks**

3.3 V LVTTL / 3.3 V LVCMOS	VIL		VIH		VOL	VOH	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[1]	Max. mA[1]	µA[2]	µA[2]
2 mA	–0.3	0.8	2	3.6	0.4	2.4	2	2	27	25	15	15
4 mA	–0.3	0.8	2	3.6	0.4	2.4	4	4	27	25	15	15
6 mA	–0.3	0.8	2	3.6	0.4	2.4	6	6	54	51	15	15
8 mA	–0.3	0.8	2	3.6	0.4	2.4	8	8	54	51	15	15
12 mA	–0.3	0.8	2	3.6	0.4	2.4	12	12	109	103	15	15
16 mA	–0.3	0.8	2	3.6	0.4	2.4	16	16	127	132	15	15
24 mA	–0.3	0.8	2	3.6	0.4	2.4	24	24	181	268	10	10

Notes:

1. *Currents are measured at 100°C junction temperature and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*
3. *Software default selection highlighted in gray.*

***Table 2-36* • Minimum and Maximum DC Input and Output Levels Applicable to MSS I/O Banks**

3.3 V LVTTL / 3.3 V LVCMOS	VIL		VIH		VOL	VOH	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[1]	Max. mA[1]	µA[2]	µA[2]
8 mA	–0.3	0.8	2	3.6	0.4	2.4	8	8	54	51	15	15

Notes:

1. *Currents are measured at 100°C junction temperature and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*
3. *Software default selection highlighted in gray.*

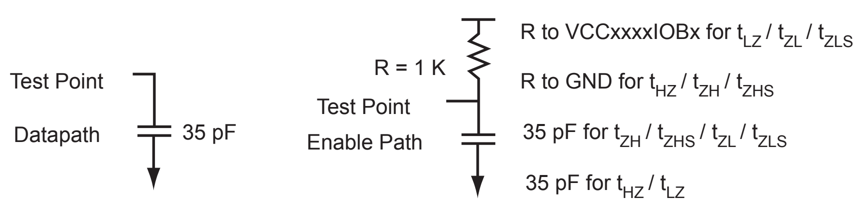


***Figure 2-6* • AC Loading**

***Table 2-37* • AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	V_{REF} (typ.) (V)	C_{LOAD} (pF)
0	3.3	1.4	–	35

*Note: *Measuring point = V_{trip}. See Table 2-22 on page 2-24 for a complete table of trip points.*

Differential I/O Characteristics

Physical Implementation

Configuration of the I/O modules as a differential pair is handled by SoC Products Group Designer software when the user instantiates a differential I/O macro in the design.

Differential I/Os can also be used in conjunction with the embedded Input Register (InReg), Output Register (OutReg), Enable Register (EnReg), and Double Data Rate (DDR). However, there is no support for bidirectional I/Os or tristates with the LVPECL standards.

LVDS

Low-Voltage Differential Signaling (ANSI/TIA/EIA-644) is a high-speed, differential I/O standard. It requires that one data bit be carried through two signal lines, so two pins are needed. It also requires external resistor termination.

The full implementation of the LVDS transmitter and receiver is shown in an example in Figure 2-11. The building blocks of the LVDS transmitter-receiver are one transmitter macro, one receiver macro, three board resistors at the transmitter end, and one resistor at the receiver end. The values for the three driver resistors are different from those used in the LVPECL implementation because the output standard specifications are different.

Along with LVDS I/O, SmartFusion cSoCs also support bus LVDS structure and multipoint LVDS (M-LVDS) configuration (up to 40 nodes).

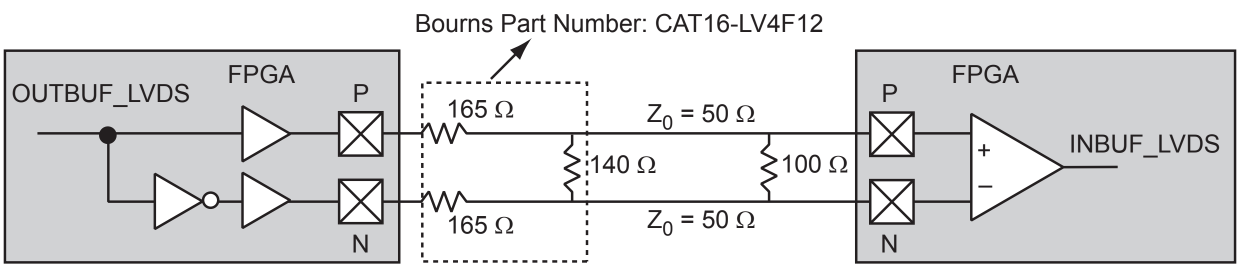


Figure 2-11 • **LVDS Circuit Diagram and Board-Level Implementation**

B-LVDS/M-LVDS

Bus LVDS (B-LVDS) and Multipoint LVDS (M-LVDS) specifications extend the existing LVDS standard to high-performance multipoint bus applications. Multidrop and multipoint bus configurations may contain any combination of drivers, receivers, and transceivers. SoC Products Group LVDS drivers provide the higher drive current required by B-LVDS and M-LVDS to accommodate the loading. The drivers require series terminations for better signal quality and to control voltage swing. Termination is also required at both ends of the bus since the driver can be located anywhere on the bus. These configurations can be implemented using the TRIBUF_LVDS and BIBUF_LVDS macros along with appropriate terminations. Multipoint designs using SoC Products Group LVDS macros can achieve up to 200 MHz with a maximum of 20 loads. A sample application is given in Figure 2-12. The input and output buffer delays are available in the LVDS section in Table 2-65.

Example: For a bus consisting of 20 equidistant loads, the following terminations provide the required differential voltage, in worst-case commercial operating conditions, at the farthest receiver: R_S = 60 Ω and R_T = 70 Ω, given Z_0 = 50 Ω (2") and Z_{stub} = 50 Ω (~1.5").

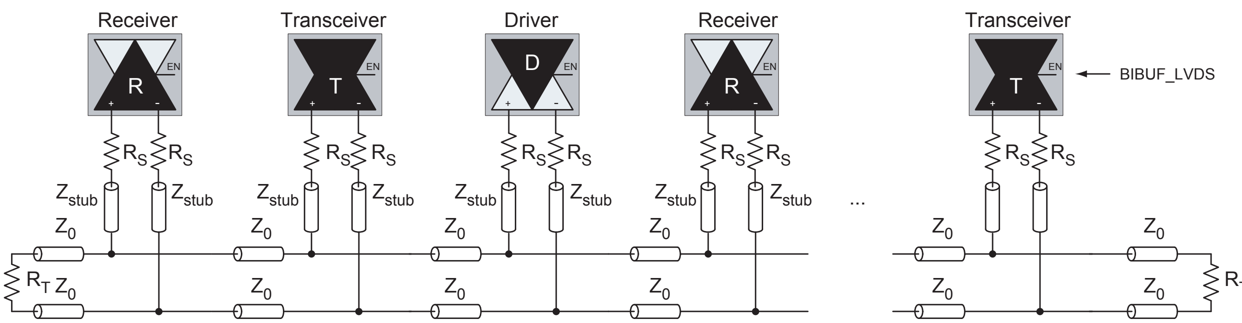


***Figure 2-12* • B-LVDS/M-LVDS Multipoint Application Using LVDS I/O Buffers**

LVPECL

Low-Voltage Positive Emitter-Coupled Logic (LVPECL) is another differential I/O standard. It requires that one data bit be carried through two signal lines. Like LVDS, two pins are needed. It also requires external resistor termination.

The full implementation of the LVDS transmitter and receiver is shown in an example in Figure 2-13. The building blocks of the LVPECL transmitter-receiver are one transmitter macro, one receiver macro, three board resistors at the transmitter end, and one resistor at the receiver end. The values for the three driver resistors are different from those used in the LVDS implementation because the output standard specifications are different.

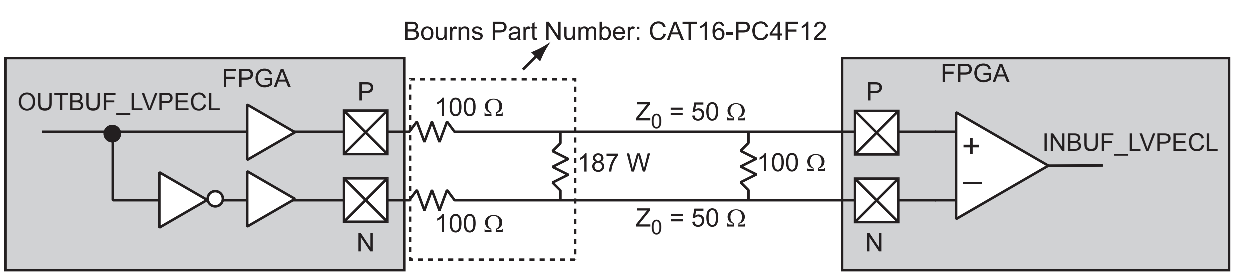


***Figure 2-13* • LVPECL Circuit Diagram and Board-Level Implementation**

Table 2-82 • A2F060 Global Resource
Worst Commercial-Case Conditions: T_J = 85°C, VCC = 1.425 V

Parameter	Description	–1		Std.		Units
		Min.[1]	Max.[2]	Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	0.75	0.96	0.90	1.15	ns
t_{RCKH}	Input High Delay for Global Clock	0.72	0.98	0.86	1.17	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	0.85		1.00		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	0.85		1.00		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.26		0.31	ns

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage-supply levels, refer to Table 2-7 on page 2-9 for derating values.*

RC Oscillator

The table below describes the electrical characteristics of the RC oscillator.

RC Oscillator Characteristics

Table 2-83 • Electrical Characteristics of the RC Oscillator

Parameter	Description	Condition	Min.	Typ.	Max.	Units
FRC	Operating frequency			100		MHz
	Accuracy	Temperature: –40°C to 100°C Voltage: 3.3 V ± 5%		1		%
	Output jitter	Period jitter (at 5 K cycles)		100		ps RMS
		Cycle-to-cycle jitter (at 5 K cycles)		100		ps RMS
		Period jitter (at 5 K cycles) with 1 KHz / 300 mV peak-to-peak noise on power supply		150		ps RMS
		Cycle-to-cycle jitter (at 5 K cycles) with 1 KHz / 300 mV peak-to-peak noise on power supply		150		ps RMS
	Output duty cycle			50		%
IDYNRC	Operating current	3.3 V domain		1		mA
		1.5 V domain		2		mA

Table 2-88 **• RAM512X18**
Worst Commercial-Case Conditions: T_J = 85°C, Worst-Case VCC = 1.425 V

Parameter	Description	–1	Std.	Units
t_{AS}	Address setup time	0.25	0.30	ns
t_{AH}	Address hold time	0.00	0.00	ns
t_{ENS}	REN, WEN setup time	0.09	0.11	ns
t_{ENH}	REN, WEN hold time	0.06	0.07	ns
t_{DS}	Input data (WD) setup time	0.19	0.22	ns
t_{DH}	Input data (WD) hold time	0.00	0.00	ns
t_{CKQ1}	Clock High to new data valid on RD (output retained, WMODE = 0)	2.19	2.63	ns
t_{CKQ2}	Clock High to new data valid on RD (pipelined)	0.91	1.09	ns
t_{C2CRWH}[1]	Address collision clk-to-clk delay for reliable read access after write on same address—applicable to opening edge	0.38	0.43	ns
t_{C2CWRH}[1]	Address collision clk-to-clk delay for reliable write access after read on same address—applicable to opening edge	0.44	0.50	ns
t_{RSTBQ}	RESET Low to data out Low on RD (flow-through)	0.94	1.12	ns
	RESET Low to data out Low on RD (pipelined)	0.94	1.12	ns
$t_{REMRSTB}$	RESET removal	0.29	0.35	ns
$t_{RECRSTB}$	RESET recovery	1.52	1.83	ns
$t_{MPWRSTB}$	RESET minimum pulse width	0.22	0.22	ns
t_{CYC}	Clock cycle time	3.28	3.28	ns
F_{MAX}	Maximum clock frequency	305	305	MHz

Notes:

1. *For more information, refer to the Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs application note.*
2. *For the derating values at specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.*

Voltage Regulator

***Table 2-99* • Voltage Regulator**

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
V_{OUT}	Output voltage	T_J = 25°C		1.425	1.5	1.575	V
V_{OS}	Output offset voltage	T_J = 25°C			11		mV
ICC33A	Operation current	T_J = 25°C	I_{LOAD} = 1 mA		3.4		mA
			I_{LOAD} = 100 mA		11		mA
			I_{LOAD} = 0.5 A		21		mA
ΔV_{OUT}	Load regulation	T_J = 25°C	I_{LOAD} = 1 mA to 0.5 A		5.8		mV
ΔV_{OUT}	Line regulation	T_J = 25°C	VCC33A = 2.97 V to 3.63 V I_{LOAD} = 1 mA		5.3		mV/V
			VCC33A = 2.97 V to 3.63 V I_{LOAD}= 100 mA		5.3		mV/V
			VCC33A = 2.97 V to 3.63 V I_{LOAD} = 500mA		5.3		mV/V
	Dropout voltage[1]	T_J = 25°C	I_{LOAD} = 1 mA		0.63		V
			I_{LOAD} = 100 mA		0.84		V
			I_{LOAD} = 0.5 A		1.35		V
I_{PTBASE}	PTBase current	T_J = 25°C	I_{LOAD} = 1 mA		48		µA
			I_{LOAD} = 100 mA		736		µA
			I_{LOAD} = 0.5 A		12		mA
	Startup time[2]	T_J = 25°C			200		µs

Notes:

1. *Dropout voltage is defined as the minimum VCC33A voltage. The parameter is specified with respect to the output voltage. The specification represents the minimum input-to-output differential voltage required to maintain regulation.*
2. *Assumes 10 µF.*

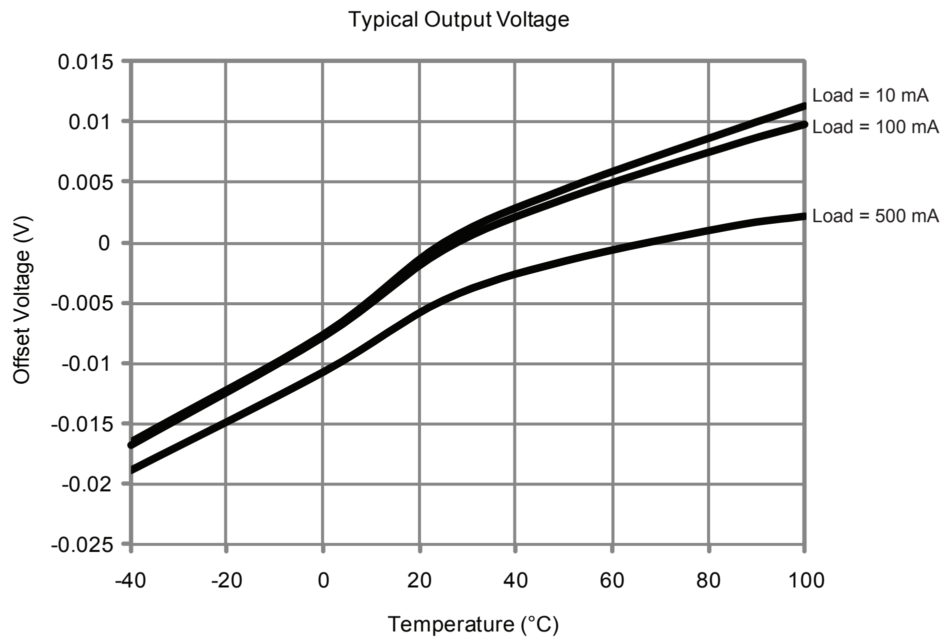


Figure 2-45 **• Typical Output Voltage**

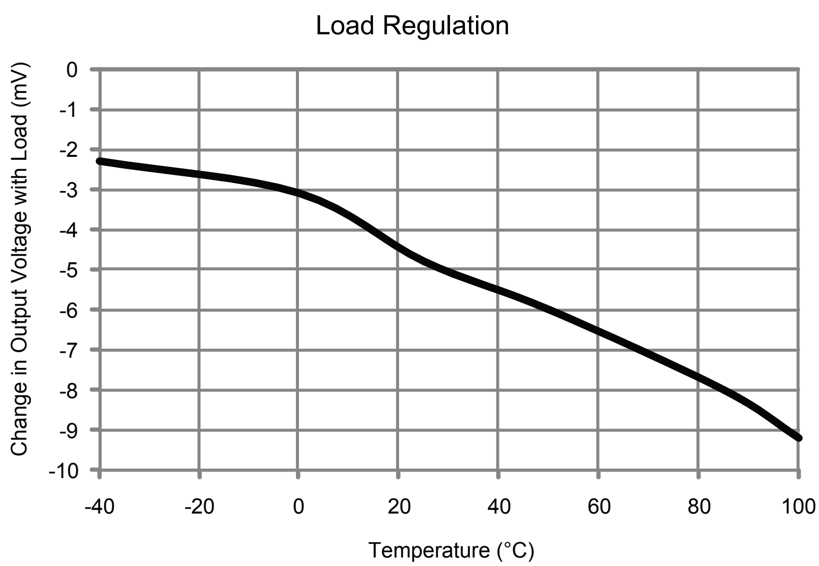


Figure 2-46 **• Load Regulation**

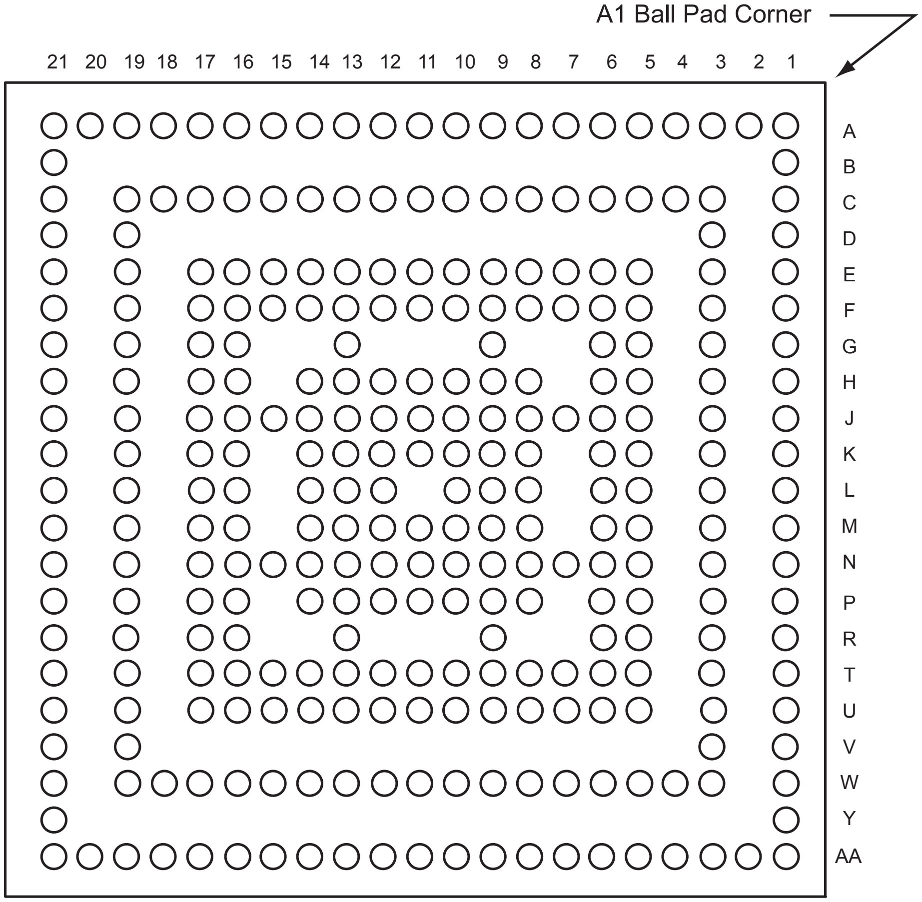
Table 5-2 **• Relationships Between Signals in the Analog Front-End**

Pin	ADC Channel	Dir.-In Option	Prescaler	Current Mon.	Temp. Mon.	Compar.	LVTTL	SDD MUX	SDD
SDD2	ADC2_CH15								SDD2_OUT
TM0	ADC0_CH4	Yes		CM0_L	TM0_IO	CMP0_N			
TM1	ADC0_CH8	Yes		CM1_L	TM1_IO	CMP2_N			
TM2	ADC1_CH4	Yes		CM2_L	TM2_IO	CMP4_N			
TM3	ADC1_CH8	Yes		CM3_L	TM3_IO	CMP6_N			
TM4	ADC2_CH4	Yes		CM4_L	TM4_IO	CMP8_N			

Notes:

1. *ABPSx_IN: Input to active bipolar prescaler channel x.*
2. *CMx_H/L: Current monitor channel x, high/low side.*
3. *TMx_IO: Temperature monitor channel x.*
4. *CMPx_P/N: Comparator channel x, positive/negative input.*
5. *LVTTLx_IN: LVTTL I/O channel x.*
6. *SDDMx_OUT: Output from sigma-delta DAC MUX channel x.*
7. *SDDx_OUT: Direct output from sigma-delta DAC channel x.*

CS288



Note: Bottom view

Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx.

Pin No.	CS288		
	A2F060 Function	A2F200 Function	A2F500 Function
AA11	ADC9	ADC6	ADC6
AA12	ABPS1	ABPS7	ABPS7
AA13	ADC6	TM2	TM2
AA14	NC	ABPS4	ABPS4
AA15	NC	SDD1	SDD1
AA16	GNDVAREF	GNDVAREF	GNDVAREF
AA17	VAREFOUT	VAREFOUT	VAREFOUT
AA18	PU_N	PU_N	PU_N
AA19	VCC33A	VCC33A	VCC33A
AA20	PTEM	PTEM	PTEM
AA21	GND	GND	GND
B1	GND	GND	GND
B21	IO17PDB0V0	GBB2/IO20NDB1V0	GBB2/IO27NDB1V0
C1	EMC_DB[15]/IO45PDB5V0	EMC_DB[15]/GAA2/IO71PDB5V0	EMC_DB[15]/GAA2/IO88PDB5V0
C3	VCOMPLA0	VCOMPLA	VCOMPLA0
C4	VCCPLL0	VCCPLL	VCCPLL0
C5	VCCFPGAIOB0	VCCFPGAIOB0	VCCFPGAIOB0
C6	EMC_AB[1]/IO04PPB0V0	EMC_AB[1]/IO04PPB0V0	EMC_AB[1]/IO06PPB0V0
C7	GND	GND	GND
C8	EMC_OEN0_N/IO03NDB0V0	EMC_OEN0_N/IO03NDB0V0	EMC_OEN0_N/IO08NDB0V0
C9	EMC_AB[2]/IO05NDB0V0	EMC_AB[2]/IO05NDB0V0	EMC_AB[2]/IO09NDB0V0
C10	EMC_AB[5]/IO06PDB0V0	EMC_AB[5]/IO06PDB0V0	EMC_AB[5]/IO10PDB0V0
C11	VCCFPGAIOB0	VCCFPGAIOB0	VCCFPGAIOB0
C12	EMC_AB[9]/IO08PPB0V0	EMC_AB[9]/IO08PPB0V0	EMC_AB[9]/IO13PPB0V0
C13	EMC_AB[15]/IO11PPB0V0	EMC_AB[15]/IO11PPB0V0	EMC_AB[15]/IO15PPB0V0
C14	EMC_AB[19]/IO13PDB0V0	EMC_AB[19]/IO13PDB0V0	EMC_AB[19]/IO18PDB0V0
C15	GND	GND	GND
C16	EMC_AB[22]/IO15NDB0V0	EMC_AB[22]/IO15NDB0V0	EMC_AB[22]/IO19NDB0V0
C17	EMC_AB[23]/IO15PDB0V0	EMC_AB[23]/IO15PDB0V0	EMC_AB[23]/IO19PDB0V0
C18	NC	NC	VCCPLL1
C19	NC	NC	VCOMPLA1

Notes:

1. *Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.*
2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*

Pin Number	PQ208	
	A2F200	A2F500
32	VCCRCOSC	VCCRCOSC
33	MSS_RESET_N	MSS_RESET_N
34	VCCESRAM	VCCESRAM
35	MAC_MDC/IO48RSB4V0	MAC_MDC/IO57RSB4V0
36	MAC_MDIO/IO49RSB4V0	MAC_MDIO/IO58RSB4V0
37	MAC_TXEN/IO52RSB4V0	MAC_TXEN/IO61RSB4V0
38	MAC_CRSDV/IO51RSB4V0	MAC_CRSDV/IO60RSB4V0
39	MAC_RXER/IO50RSB4V0	MAC_RXER/IO59RSB4V0
40	GND	GND
41	VCCMSSIOB4	VCCMSSIOB4
42	VCC	VCC
43	MAC_TXD[0]/IO56RSB4V0	MAC_TXD[0]/IO65RSB4V0
44	MAC_TXD[1]/IO55RSB4V0	MAC_TXD[1]/IO64RSB4V0
45	MAC_RXD[0]/IO54RSB4V0	MAC_RXD[0]/IO63RSB4V0
46	MAC_RXD[1]/IO53RSB4V0	MAC_RXD[1]/IO62RSB4V0
47	MAC_CLK	MAC_CLK
48	GNDSDD0	GNDSDD0
49	VCC33SDD0	VCC33SDD0
50	VCC15A	VCC15A
51	PCAP	PCAP
52	NCAP	NCAP
53	VCC33AP	VCC33AP
54	VCC33N	VCC33N
55	SDD0	SDD0
56	GNDA	GNDA
57	GNDAQ	GNDAQ
58	ABPS0	ABPS0
59	ABPS1	ABPS1
60	CM0	CM0
61	TM0	TM0
62	GNDTM0	GNDTM0

Notes:

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2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*

Pin No.	FG256		
	A2F060 Function	A2F200 Function	A2F500 Function
A1	GND	GND	GND
A2	VCCFPGAIOB0	VCCFPGAIOB0	VCCFPGAIOB0
A3	EMC_AB[0]/IO04NDB0V0	EMC_AB[0]/IO04NDB0V0	EMC_AB[0]/IO06NDB0V0
A4	EMC_AB[1]/IO04PDB0V0	EMC_AB[1]/IO04PDB0V0	EMC_AB[1]/IO06PDB0V0
A5	GND	GND	GND
A6	EMC_AB[3]/IO05PDB0V0	EMC_AB[3]/IO05PDB0V0	EMC_AB[3]/IO09PDB0V0
A7	EMC_AB[5]/IO06PDB0V0	EMC_AB[5]/IO06PDB0V0	EMC_AB[5]/IO10PDB0V0
A8	VCCFPGAIOB0	VCCFPGAIOB0	VCCFPGAIOB0
A9	GND	GND	GND
A10	EMC_AB[14]/IO11NDB0V0	EMC_AB[14]/IO11NDB0V0	EMC_AB[14]/IO15NDB0V0
A11	EMC_AB[15]/IO11PDB0V0	EMC_AB[15]/IO11PDB0V0	EMC_AB[15]/IO15PDB0V0
A12	GND	GND	GND
A13	EMC_AB[20]/IO14NDB0V0	EMC_AB[20]/IO14NDB0V0	EMC_AB[20]/IO21NDB0V0
A14	EMC_AB[24]/IO16NDB0V0	EMC_AB[24]/IO16NDB0V0	EMC_AB[24]/IO20NDB0V0
A15	VCCFPGAIOB0	VCCFPGAIOB0	VCCFPGAIOB0
A16	GND	GND	GND
B1	EMC_DB[15]/IO45PDB5V0	EMC_DB[15]/GAA2/IO71PDB5V0	EMC_DB[15]/GAA2/IO88PDB5V0
B2	GND	GND	GND
B3	EMC_BYTEN[1]/IO02PDB0V0	EMC_BYTEN[1]/GAC1/IO02PDB0V0	EMC_BYTEN[1]/GAC1/IO07PDB0V0
B4	EMC_OEN0_N/IO03NDB0V0	EMC_OEN0_N/IO03NDB0V0	EMC_OEN0_N/IO08NDB0V0
B5	EMC_OEN1_N/IO03PDB0V0	EMC_OEN1_N/IO03PDB0V0	EMC_OEN1_N/IO08PDB0V0
B6	EMC_AB[2]/IO05NDB0V0	EMC_AB[2]/IO05NDB0V0	EMC_AB[2]/IO09NDB0V0
B7	EMC_AB[4]/IO06NDB0V0	EMC_AB[4]/IO06NDB0V0	EMC_AB[4]/IO10NDB0V0
B8	EMC_AB[9]/IO08PDB0V0	EMC_AB[9]/IO08PDB0V0	EMC_AB[9]/IO13PDB0V0
B9	EMC_AB[12]/IO10NDB0V0	EMC_AB[12]/IO10NDB0V0	EMC_AB[12]/IO14NDB0V0
B10	EMC_AB[13]/IO10PDB0V0	EMC_AB[13]/IO10PDB0V0	EMC_AB[13]/IO14PDB0V0
B11	EMC_AB[16]/IO12NDB0V0	EMC_AB[16]/IO12NDB0V0	EMC_AB[16]/IO17NDB0V0
B12	EMC_AB[18]/IO13NDB0V0	EMC_AB[18]/IO13NDB0V0	EMC_AB[18]/IO18NDB0V0
B13	EMC_AB[21]/IO14PDB0V0	EMC_AB[21]/IO14PDB0V0	EMC_AB[21]/IO21PDB0V0
B14	EMC_AB[25]/IO16PDB0V0	EMC_AB[25]/IO16PDB0V0	EMC_AB[25]/IO20PDB0V0
B15	GND	GND	GND

Notes:

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2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*

Pin No.	FG256		
	A2F060 Function	A2F200 Function	A2F500 Function
H13	TDO	TDO	TDO
H14	TDI	TDI	TDI
H15	JTAGSEL	JTAGSEL	JTAGSEL
H16	GND	GND	GND
J1	EMC_DB[4]/IO38NPB5V0	EMC_DB[4]/GEA0/IO61NPB5V0	EMC_DB[4]/GEA0/IO78NPB5V0
J2	EMC_DB[3]/IO37PDB5V0	EMC_DB[3]/GEC2/IO60PDB5V0	EMC_DB[3]/GEC2/IO77PDB5V0
J3	EMC_DB[2]/IO37NDB5V0	EMC_DB[2]/IO60NDB5V0	EMC_DB[2]/IO77NDB5V0
J4	GNDRCOSC	GNDRCOSC	GNDRCOSC
J5	NC	GNDQ	GNDQ
J6	GND	GND	GND
J7	VCC	VCC	VCC
J8	GND	GND	GND
J9	VCC	VCC	VCC
J10	GND	GND	GND
J11	VCCMSSIOB2	VCCMSSIOB2	VCCMSSIOB2
J12	I2C_0_SCL/GPIO_23	I2C_0_SCL/GPIO_23	I2C_0_SCL/GPIO_23
J13	I2C_0_SDA/GPIO_22	I2C_0_SDA/GPIO_22	I2C_0_SDA/GPIO_22
J14	I2C_1_SCL/GPIO_31	I2C_1_SCL/GPIO_31	I2C_1_SCL/GPIO_31
J15	VCCMSSIOB2	VCCMSSIOB2	VCCMSSIOB2
J16	I2C_1_SDA/GPIO_30	I2C_1_SDA/GPIO_30	I2C_1_SDA/GPIO_30
K1	GPIO_1/IO32RSB4V0	MAC_MDIO/IO49RSB4V0	MAC_MDIO/IO58RSB4V0
K2	GPIO_0/IO33RSB4V0	MAC_MDC/IO48RSB4V0	MAC_MDC/IO57RSB4V0
K3	VCCMSSIOB4	VCCMSSIOB4	VCCMSSIOB4
K4	MSS_RESET_N	MSS_RESET_N	MSS_RESET_N
K5	VCCRCOSC	VCCRCOSC	VCCRCOSC
K6	VCCMSSIOB4	VCCMSSIOB4	VCCMSSIOB4
K7	GND	GND	GND
K8	VCC	VCC	VCC
K9	GND	GND	GND
K10	VCC	VCC	VCC
K11	GND	GND	GND

Notes:

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2. **: Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.*

Pin Number	FG484	
	A2F200 Function	A2F500 Function
C15	EMC_AB[17]/IO12PDB0V0	EMC_AB[17]/IO17PDB0V0
C16	EMC_AB[24]/IO16NDB0V0	EMC_AB[24]/IO20NDB0V0
C17	EMC_AB[22]/IO15NDB0V0	EMC_AB[22]/IO19NDB0V0
C18	EMC_AB[23]/IO15PDB0V0	EMC_AB[23]/IO19PDB0V0
C19	GBA0/IO19NPB0V0	GBA0/IO23NPB0V0
C20	NC	NC
C21	GBC2/IO21PDB1V0	GBC2/IO30PDB1V0
C22	GBB2/IO20NDB1V0	GBB2/IO27NDB1V0
D1	GND	GND
D2	EMC_DB[12]/IO70NDB5V0	EMC_DB[12]/IO87NDB5V0
D3	EMC_DB[13]/GAC2/IO70PDB5V0	EMC_DB[13]/GAC2/IO87PDB5V0
D4	NC	NC
D5	NC	NC
D6	GND	GND
D7	NC	IO00NPB0V0
D8	NC	IO03NPB0V0
D9	GND	GND
D10	EMC_OEN0_N/IO03NDB0V0	EMC_OEN0_N/IO08NDB0V0
D11	EMC_AB[10]/IO09NDB0V0	EMC_AB[10]/IO11NDB0V0
D12	EMC_AB[11]/IO09PDB0V0	EMC_AB[11]/IO11PDB0V0
D13	EMC_AB[9]/IO08PDB0V0	EMC_AB[9]/IO13PDB0V0
D14	GND	GND
D15	GBC1/IO17PPB0V0	GBC1/IO22PPB0V0
D16	EMC_AB[25]/IO16PDB0V0	EMC_AB[25]/IO20PDB0V0
D17	GND	GND
D18	GBA1/IO19PPB0V0	GBA1/IO23PPB0V0
D19	NC	NC
D20	NC	NC
D21	IO21NDB1V0	IO30NDB1V0
D22	GND	GND
E1	GFC2/IO67PPB5V0	GFC2/IO84PPB5V0
E2	VCCFPGAIOB5	VCCFPGAIOB5
E3	GFA2/IO68PDB5V0	GFA2/IO85PDB5V0
E4	GND	GND

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Pin Number	FG484	
	A2F200 Function	A2F500 Function
F17	NC	IO25PPB1V0
F18	VCCFPGAIOB1	VCCFPGAIOB1
F19	IO23NDB1V0	IO28NDB1V0
F20	NC	IO31PDB1V0
F21	NC	IO31NDB1V0
F22	IO22PDB1V0	IO32PDB1V0
G1	GND	GND
G2	GFB0/IO65NPB5V0	GFB0/IO82NPB5V0
G3	EMC_DB[9]/GEC1/IO63PDB5V0	EMC_DB[9]/GEC1/IO80PDB5V0
G4	GFC1/IO66PPB5V0	GFC1/IO83PPB5V0
G5	EMC_DB[11]/IO69PPB5V0	EMC_DB[11]/IO86PPB5V0
G6	GNDQ	GNDQ
G7	NC	NC
G8	GND	GND
G9	VCCFPGAIOB0	VCCFPGAIOB0
G10	GND	GND
G11	VCCFPGAIOB0	VCCFPGAIOB0
G12	GND	GND
G13	VCCFPGAIOB0	VCCFPGAIOB0
G14	GND	GND
G15	VCCFPGAIOB0	VCCFPGAIOB0
G16	GNDQ	GNDQ
G17	NC	IO26PDB1V0
G18	NC	IO26NDB1V0
G19	GCA2/IO23PDB1V0	GCA2/IO28PDB1V0 *
G20	IO24NDB1V0	IO33NDB1V0
G21	GCB2/IO24PDB1V0	GCB2/IO33PDB1V0
G22	GND	GND
H1	EMC_DB[7]/GEB1/IO62PDB5V0	EMC_DB[7]/GEB1/IO79PDB5V0
H2	VCCFPGAIOB5	VCCFPGAIOB5
H3	EMC_DB[8]/GEC0/IO63NDB5V0	EMC_DB[8]/GEC0/IO80NDB5V0
H4	GND	GND
H5	GFC0/IO66NPB5V0	GFC0/IO83NPB5V0
H6	GFA1/IO64PDB5V0	GFA1/IO81PDB5V0

Notes:

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Pin Number	FG484	
	A2F200 Function	A2F500 Function
W3	GND	GND
W4	MAC_CRSDV/IO51RSB4V0	MAC_CRSDV/IO60RSB4V0
W5	MAC_TXD[1]/IO55RSB4V0	MAC_TXD[1]/IO64RSB4V0
W6	NC	SDD2
W7	GNDA	GNDA
W8	TM0	TM0
W9	ABPS2	ABPS2
W10	GND33ADC0	GND33ADC0
W11	VCC15ADC1	VCC15ADC1
W12	ABPS6	ABPS6
W13	NC	CM4
W14	NC	ABPS9
W15	NC	VCC33ADC2
W16	GNDA	GNDA
W17	PU_N	PU_N
W18	GNDSDD1	GNDSDD1
W19	SPI_0_CLK/GPIO_18	SPI_0_CLK/GPIO_18
W20	GND	GND
W21	SPI_1_SS/GPIO_27	SPI_1_SS/GPIO_27
W22	UART_1_RXD/GPIO_29	UART_1_RXD/GPIO_29
Y1	GPIO_3/IO44RSB4V0	GPIO_3/IO53RSB4V0
Y2	VCCMSSIOB4	VCCMSSIOB4
Y3	GPIO_15/IO34RSB4V0	GPIO_15/IO43RSB4V0
Y4	MAC_TXEN/IO52RSB4V0	MAC_TXEN/IO61RSB4V0
Y5	VCCMSSIOB4	VCCMSSIOB4
Y6	GNDSDD0	GNDSDD0
Y7	CM0	CM0
Y8	GNDTM0	GNDTM0
Y9	ADC0	ADC0
Y10	VCC15ADC0	VCC15ADC0
Y11	ABPS7	ABPS7
Y12	TM3	TM3
Y13	NC	ABPS8
Y14	NC	GND33ADC2

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