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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	I ² C, IrDA, LINbus, MMC/SD/SDIO, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	81
Program Memory Size	256КВ (256К х 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-UFBGA
Supplier Device Package	100-UFBGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f411vch6

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

2.1 Compatibility with STM32F4 series

The STM32F411xC/xE are fully software and feature compatible with the STM32F4 series (STM32F42x, STM32F401, STM32F43x, STM32F41x, STM32F405 and STM32F407)

The STM32F411xC/xE can be used as drop-in replacement of the other STM32F4 products but some slight changes have to be done on the PCB board.







3.20 Timers and watchdogs

The devices embed one advanced-control timer, seven general-purpose timers and two watchdog timers.

All timer counters can be frozen in debug mode.

Table 4 compares the features of the advanced-control and general-purpose timers.

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/ compare channels	Complemen- tary output	Max. interface clock (MHz)	Max. timer clock (MHz)
Advanced -control	TIM1	16-bit	Up, Down, Up/down	Any integer between 1 and 65536	Yes	4	Yes	100	100
	TIM2, TIM5	32-bit	Up, Down, Up/down	Any integer between 1 and 65536	Yes	4	No	50	100
General	TIM3, TIM4	16-bit	Up, Down, Up/down	Any integer between 1 and 65536	Yes	4	No	50	100
purpose	TIM9	16-bit	Up	Any integer between 1 and 65536	No	2	No	100	100
	TIM10, TIM11	16-bit	Up	Any integer between 1 and 65536	No	1	No	100	100

	Table 4.	Timer	feature	comparison
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3.20.1 Advanced-control timers (TIM1)

The advanced-control timer (TIM1) can be seen as three-phase PWM generators multiplexed on 4 independent channels. It has complementary PWM outputs with programmable inserted dead times. It can also be considered as a complete general-purpose timer. Its 4 independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge- or center-aligned modes)
- One-pulse mode output



	Pir	n numl	oer							
UFQFPN48	LQFP64	WLCSP49	LQFP100	UFBGA100	Pin name (function after reset) ⁽¹⁾	Pin type	I/O structure	Notes	Alternate functions	Additional functions
21	29	E3	47	L10	PB10	I/O	I/O FT -		TIM2_CH3, I2C2_SCL, SPI2_SCK/I2S2_CK, I2S3_MCK, SDIO_D7, EVENTOUT	-
-	-	-	-	K9	PB11	I/O	I/O FT - 120 EV		TIM2_CH4, I2C2_SDA, I2S2_CKIN, EVENTOUT	-
22	30	G2	48	L11	VCAP_1	S	-	-	-	-
23	31	D3	49	F12	VSS	S	-	-	-	-
24	32	F2	50	G12	VDD	S	-	-	-	-
25	33	E2	51	L12	PB12	I/O	FT	-	TIM1_BKIN, I2C2_SMBA, SPI2_NSS/I2S2_WS, SPI4_NSS/I2S4_WS, SPI3_SCK/I2S3_CK, EVENTOUT	-
26	34	G1	52	K12	PB13	I/O	FT	-	TIM1_CH1N, SPI2_SCK/I2S2_CK, SPI4_SCK/I2S4_CK, EVENTOUT	-
27	35	F1	53	K11	PB14	I/O	/O FT - 12 S		TIM1_CH2N, SPI2_MISO, I2S2ext_SD, SDIO_D6, EVENTOUT	-
28	36	E1	54	K10	PB15	I/O	D FT -		RTC_50Hz, TIM1_CH3N, SPI2_MOSI/I2S2_SD, SDIO_CK, EVENTOUT	RTC_REFIN
-	-	-	55	-	PD8	I/O	FT	-	-	-
-	-	-	56	K8	PD9	I/O	FT	-	-	-
-	-	-	57	J12	PD10	I/O	FT	-	-	-
-	-	-	58	J11	PD11	I/O	FT	-	-	-
-	-	-	59	J10	PD12	I/O	FT	-	TIM4_CH1, EVENTOUT	-

Table 8. STM32F411xC/xE pin definitions (continued	F411xC/xE pin definitions (continued)
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Table 9. Alternate function mapping

_						Ius				Jing							
		AF00	AF01	AF02	AF03	AF04	AF05	AF06	AF07	AF08	AF09	AF10	AF11	AF12	AF13	AF14	AF15
	Port	SYS_AF	TIM1/TIM2	TIM3/ TIM4/ TIM5	TIM9/ TIM10/ TIM11	I2C1/I2C2/ I2C3	SPI1/I2S1S PI2/ I2S2/SPI3/ I2S3	SPI2/I2S2/ SPI3/ I2S3/SPI4/ I2S4/SPI5/ I2S5	SPI3/I2S3/ USART1/ USART2	USART6	12C2/ 12C3	OTG1_FS		SDIO			
	PA0	-	TIM2_CH1/ TIM2_ETR	TIM5_CH1	-	-	-	-	USART2_ CTS	-	-	-	-	-	-	-	EVENT OUT
	PA1	-	TIM2_CH2	TIM5_CH2	-	-	SPI4_MOSI /I2S4_SD	-	USART2_ RTS	-	-	-	-	-	-	-	EVENT OUT
	PA2	-	TIM2_CH3	TIM5_CH3	TIM9_CH1	-	I2S2_CKIN	-	USART2_ TX	-	-	-	-	-	-	-	EVENT OUT
	PA3	-	TIM2_CH4	TIM5_CH4	TIM9_CH2	-	I2S2_MCK	-	USART2_ RX	-	-	-	-	-	-	-	EVENT OUT
	PA4	-	-	-	-	-	SPI1_NSS/I 2S1_WS	SPI3_NSS/I2 S3_WS	USART2_ CK	-	-	-	-	-	-	-	EVENT OUT
	PA5	-	TIM2_CH1/ TIM2_ETR	-	-	-	SPI1_SCK/I 2S1_CK	-	-	-	-	-	-	-	-	-	EVENT OUT
	PA6	-	TIM1_BKIN	TIM3_CH1	-	-	SPI1_MISO	I2S2_MCK	-	-	-	-	-	SDIO_ CMD	-	-	EVENT OUT
4 A	PA7	-	TIM1_CH1N	TIM3_CH2	-	-	SPI1_MOSI /I2S1_SD	-	-	-	-	-	-	-	-	-	EVENT OUT
Pol	PA8	MCO_1	TIM1_CH1	-	-	I2C3_ SCL	-	-	USART1_ CK	-	-	USB_FS_ SOF	-	SDIO_ D1	-	-	EVENT OUT
	PA9	-	TIM1_CH2	-	-	I2C3_ SMBA	-	-	USART1_ TX	-	-	USB_FS_ VBUS	-	SDIO_ D2	-	-	EVENT OUT
	PA10	-	TIM1_CH3	-	-	-	-	SPI5_MOSI/I 2S5_SD	USART1_ RX	-	-	USB_FS_ ID	-	-	-	-	EVENT OUT
	PA11	-	TIM1_CH4	-	-	-	-	SPI4_MISO	USART1_ CTS	USART6_ TX	-	USB_FS_ DM	-	-	-	-	EVENT OUT
	PA12	-	TIM1_ETR	-	-	-	-	SPI5_MISO	USART1_ RTS	USART6_ RX	-	USB_FS_ DP	-	-	-	-	EVENT OUT
	PA13	JTMS- SWDIO	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
	PA14	JTCK- SWCLK	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
	PA15	JTDI	TIM2_CH1/ TIM2_ETR	-	-	-	SPI1_NSS/I 2S1_WS	SPI3_NSS/I2 S3_WS	USART1_ TX	-	-	-	-	-	-	-	EVENT OUT

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Pinouts and pin description

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					Т	able 9. A	Iternate f	unction ma	apping (c	continue	d)						
		AF00	AF01	AF02	AF03	AF04	AF05	AF06	AF07	AF08	AF09	AF10	AF11	AF12	AF13	AF14	AF15
	Port	SYS_AF	TIM1/TIM2	TIM3/ TIM4/ TIM5	TIM9/ TIM10/ TIM11	I2C1/I2C2/ I2C3	SPI1/I2S1S PI2/ I2S2/SPI3/ I2S3	SPI2/I2S2/ SPI3/ I2S3/SPI4/ I2S4/SPI5/ I2S5	SPI3/I2S3/ USART1/ USART2	USART6	12C2/ 12C3	OTG1_FS		SDIO			
	PB0	-	TIM1_CH2N	TIM3_CH3	-	-	-	SPI5_SCK /I2S5_CK		-	-	-	-	-	-	-	EVENT OUT
	PB1	-	TIM1_CH3N	TIM3_CH4	-	-	-	SPI5_NSS /I2S5_WS		-	-	-	-	-	-	-	EVENT OUT
	PB2	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
	PB3	JTDO- SWO	TIM2_CH2	-	-	-	SPI1_SCK/I 2S1_CK	SPI3_SCK /I2S3_CK	USART1_ RX	-	I2C2_SDA	-	-	-	-	-	EVENT OUT
	PB4	JTRST		TIM3_CH1	-	-	SPI1_MISO	SPI3_MISO	I2S3ext_S D	-	I2C3_SDA			SDIO_ D0	-	-	EVENT OUT
	PB5	-	-	TIM3_CH2	-	I2C1_SMB A	SPI1_MOSI /I2S1_SD	SPI3_MOSI/ I2S3_SD		-	-	-	-	SDIO_ D3	-	-	EVENT OUT
	PB6	-	-	TIM4_CH1	-	I2C1_SCL	-	-	USART1_ TX	-	-	-	-		-	-	EVENT OUT
t B	PB7	-	-	TIM4_CH2	-	I2C1_SDA	-	-	USART1_ RX	-	-	-	-	SDIO_ D0	-	-	EVENT OUT
Por	PB8	-	-	TIM4_CH3	TIM10_CH1	I2C1_SCL	-	SPI5_MOSI/ I2S5_SD	-	-	I2C3_SDA	-	-	SDIO_ D4	-	-	EVENT OUT
	PB9	-	-	TIM4_CH4	TIM11_CH1	I2C1_SDA	SPI2_NSS/I 2S2_WS	-	-	-	I2C2_SDA	-	-	SDIO_ D5	-	-	EVENT OUT
	PB10	-	TIM2_CH3	-	-	I2C2_SCL	SPI2_SCK/I 2S2_CK	I2S3_MCK	-	-	-	-	-	SDIO_ D7	-	-	EVENT OUT
	PB11	-	TIM2_CH4	-	-	I2C2_SDA	I2S2_CKIN	-	-	-	-	-	-	-	-	-	EVENT OUT
	PB12	-	TIM1_BKIN	-	-	I2C2_SMB A	SPI2_NSS/I 2S2_WS	SPI4_NSS /I2S4_WS	SPI3_SCK /I2S3_CK	-	-	-	-	-	-	-	EVENT OUT
	PB13	-	TIM1_CH1N	-	-	-	SPI2_SCK/I 2S2_CK	SPI4_SCK/ I2S4_CK	-	-	-	-	-	-	-	-	EVENT OUT
	PB14	-	TIM1_CH2N	-	-	-	SPI2_MISO	I2S2ext_SD	-	-	-	-	-	SDIO_ D6	-	-	EVENT OUT
	PB15	RTC_50H z	TIM1_CH3N	-	-	-	SPI2_MOSI /I2S2_SD	-	-	-	-	-	-	SDIO_ CK	-	-	EVENT OUT

Pinouts and pin description

STM32F411xC STM32F411xE

Bus	Boundary address	Peripheral
	0x4000 7000 - 0x4000 73FF	PWR
	0x4000 6000 - 0x4000 6FFF	Reserved
	0x4000 5C00 - 0x4000 5FFF	12C3
	0x4000 5800 - 0x4000 5BFF	12C2
	0x4000 5400 - 0x4000 57FF	12C1
	0x4000 4800 - 0x4000 53FF	Reserved
	0x4000 4400 - 0x4000 47FF	USART2
	0x4000 4000 - 0x4000 43FF	I2S3ext
	0x4000 3C00 - 0x4000 3FFF	SPI3 / I2S3
APB1	0x4000 3800 - 0x4000 3BFF	SPI2 / I2S2
	0x4000 3400 - 0x4000 37FF	I2S2ext
	0x4000 3000 - 0x4000 33FF	IWDG
	0x4000 2C00 - 0x4000 2FFF	WWDG
	0x4000 2800 - 0x4000 2BFF	RTC & BKP Registers
	0x4000 1000 - 0x4000 27FF	Reserved
	0x4000 0C00 - 0x4000 0FFF	TIM5
	0x4000 0800 - 0x4000 0BFF	TIM4
	0x4000 0400 - 0x4000 07FF	ТІМЗ
	0x4000 0000 - 0x4000 03FF	TIM2

Table 10. STM32F411xC/xE register boundary addresses (continued)



6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 16*.







Symbol	Parameter	Conditions	Min	Тур	Max	Unit
I _{RUSH} ⁽²⁾	In-Rush current on voltage regulator power- on (POR or wakeup from Standby)	-	-	160	200	mA
E _{RUSH} ⁽²⁾	In-Rush energy on voltage regulator power- on (POR or wakeup from Standby)	V _{DD} = 1.7 V, T _A = 125 °C, I _{RUSH} = 171 mA for 31 µs	-	-	5.4	μC

 Table 19. Embedded reset and power control block characteristics (continued)

1. The product behavior is guaranteed by design down to the minimum V_{POR/PDR} value.

2. Guaranteed by design.

3. The reset timing is measured from the power-on (POR reset or wakeup from V_{BAT}) to the instant when first instruction is fetched by the user application code.

6.3.6 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

The current consumption is measured as described in *Figure 18: Current consumption measurement scheme*.

All the run-mode current consumption measurements given in this section are performed with a reduced code that gives a consumption equivalent to CoreMark code.

Typical and maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in input mode with a static value at VDD or VSS (no load).
- All peripherals are disabled except if it is explicitly mentioned.
- The Flash memory access time is adjusted to both f_{HCLK} frequency and VDD ranges (refer to *Table 15: Features depending on the operating power supply range*).
- The voltage scaling is adjusted to f_{HCLK} frequency as follows:
 - Scale 3 for $f_{HCLK} \le 64$ MHz
 - Scale 2 for 64 MHz < $f_{HCLK} \le 84$ MHz
 - Scale 1 for 84 MHz < f_{HCLK} ≤ 100 MHz
- The system clock is HCLK, $f_{PCLK1} = f_{HCLK}/2$, and $f_{PCLK2} = f_{HCLK}$.
- External clock is 4 MHz and PLL is ON except if it is explicitly mentioned.
- The maximum values are obtained for V_{DD} = 3.6 V and a maximum ambient temperature (T_A), and the typical values for T_A= 25 °C and V_{DD} = 3.3 V unless otherwise specified.



I/O system current consumption

The current consumption of the I/O system has two components: static and dynamic.

I/O static current consumption

All the I/Os used as inputs with pull-up generate current consumption when the pin is externally held low. The value of this current consumption can be simply computed by using the pull-up/pull-down resistors values given in *Table 53: I/O static characteristics*.

For the output pins, any external pull-down or external load must also be considered to estimate the current consumption.

Additional I/O current consumption is due to I/Os configured as inputs if an intermediate voltage level is externally applied. This current consumption is caused by the input Schmitt trigger circuits used to discriminate the input value. Unless this specific configuration is required by the application, this supply current consumption can be avoided by configuring these I/Os in analog mode. This is notably the case of ADC input pins which should be configured as analog inputs.

Caution: Any floating input pin can also settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid current consumption related to floating pins, they must either be configured in analog mode, or forced internally to a definite digital value. This can be done either by using pull-up/down resistors or by configuring the pins in output mode.

I/O dynamic current consumption

In addition to the internal peripheral current consumption (see *Table 33: Peripheral current consumption*), the I/Os used by an application also contribute to the current consumption. When an I/O pin switches, it uses the current from the MCU supply voltage to supply the I/O pin circuitry and to charge/discharge the capacitive load (internal or external) connected to the pin:

$$I_{SW} = V_{DD} \times f_{SW} \times C$$

where

 ${\rm I}_{\rm SW}$ is the current sunk by a switching I/O to charge/discharge the capacitive load

V_{DD} is the MCU supply voltage

 f_{SW} is the I/O switching frequency

C is the total capacitance seen by the I/O pin: C = C_{INT} + C_{EXT}

The test pin is configured in push-pull output mode and is toggled by software at a fixed frequency.





Figure 27. ACC_{LSI} versus temperature

6.3.10 PLL characteristics

The parameters given in *Table 41* and *Table 42* are derived from tests performed under temperature and V_{DD} supply voltage conditions summarized in *Table 14*.

Symbol	Parameter	Conditions	Min	Тур	Мах	Unit		
f _{PLL_IN}	PLL input clock ⁽¹⁾			0.95 ⁽²⁾	1	2.10	MHz	
f _{PLL_OUT}	PLL multiplier output clock			24	-	100	MHz	
f _{PLL48_OUT}	48 MHz PLL multiplier output clock			-	48	75	MHz	
f _{VCO_OUT}	PLL VCO output			100	-	432	MHz	
t	PLL lock time	VCO freq = 100 N	75	-	200	116		
LOCK		VCO freq = 432 N	100	-	300	μο		
Jitter ⁽³⁾			RMS	-	25	-		
	Cycle-to-cycle jitter	System clock	peak to peak	-	±150	-	ns	
		100 MHz	RMS	-	15	-	ps	
	Period Jitter		peak to peak	-	±200	-		

Table	41.	Main	PLL	characteristics
10010				



Static latchup

Two complementary static tests are required on six parts to assess the latchup performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD 78A IC latchup standard.

Table	51.	Electrical	sensitivities
10010	••••	LIGOUIOUI	001101111100

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	$T_A = + 125 \text{ °C conforming to JESD78A}$	II level A

6.3.15 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard, 3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (>5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of -5μ A/+0 μ A range), or other functional failure (for example reset, oscillator frequency deviation).

Negative induced leakage current is caused by negative injection and positive induced leakage current by positive injection.

The test results are given in Table 52.

		Functional s			
Symbol	Description	Negative injection	Positive injection	Unit	
I _{INJ}	Injected current on BOOT0 pin	-0	NA		
	Injected current on NRST pin	-0	NA		
	Injected current on PB3, PB4, PB5, PB6, PB7, PB8, PB9, PC13, PC14, PC15, PH1, PDR_ON, PC0, PC1,PC2, PC3, PD1, PD5, PD6, PD7, PE0, PE2, PE3, PE4, PE5, PE6	-0	NA	mA	
	Injected current on any other FT pin	-5	NA		
	Injected current on any other pins	-5	+5		

Table 52. I/O current injection susceptibility⁽¹⁾

1. NA = not applicable.



Symbol	Param	eter	Conditions	Min	Тур	Мах	Unit
R _{PU}	Weak pull-up equivalent resistor ⁽⁶⁾	All pins except for PA10 (OTG_FS_ID)	$V_{IN} = V_{SS}$	30	40	50	
		PA10 (OTG_FS_ID)	-	7	10	14	kO
Weak pull-down R _{PD} equivalent resistor ⁽⁷⁾	All pins except for PA10 (OTG_FS_ID)	$V_{IN} = V_{DD}$	30	40	50	K22	
	resistor	PA10 (OTG_FS_ID)	-	7	10	14	
C _{IO} ⁽⁸⁾	I/O pin capacitanc	e	-	-	5	-	pF

Table 53. I/O static characteristics (continued)

1. Guaranteed by test in production.

2. Guaranteed by design.

3. With a minimum of 200 mV.

- 4. Leakage could be higher than the maximum value, if negative current is injected on adjacent pins, Refer to Table 52: I/O current injection susceptibility
- To sustain a voltage higher than VDD +0.3 V, the internal pull-up/pull-down resistors must be disabled. Leakage could be higher than the maximum value, if negative current is injected on adjacent pins.Refer to Table 52: I/O current injection susceptibility
- 6. Pull-up resistors are designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance is minimum (~10% order).
- Pull-down resistors are designed with a true resistance in series with a switchable NMOS. This NMOS contribution to the series resistance is minimum (~10% order).
- 8. Hysteresis voltage between Schmitt trigger switching levels. Guaranteed by characterization results.

All I/Os are CMOS and TTL compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements for FT and TC I/Os is shown in *Figure 30*.





Figure 30. FT/TC I/O input characteristics

Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to ± 8 mA, and sink or source up to ± 20 mA (with a relaxed V_{OL}/V_{OH}) except PC13, PC14 and PC15 which can sink or source up to ± 3 mA. When using the PC13 to PC15 GPIOs in output mode, the speed should not exceed 2 MHz with a maximum load of 30 pF.

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 6.2*. In particular:

- The sum of the currents sourced by all the I/Os on V_{DD}, plus the maximum Run consumption of the MCU sourced on V_{DD}, cannot exceed the absolute maximum rating ΣI_{VDD} (see *Table 12*).
- The sum of the currents sunk by all the I/Os on V_{SS} plus the maximum Run consumption of the MCU sunk on V_{SS} cannot exceed the absolute maximum rating ΣI_{VSS} (see *Table 12*).



SPI interface characteristics

Unless otherwise specified, the parameters given in *Table 60* for the SPI interface are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 14*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: 0.5V_{DD}

Refer to Section 6.3.16: I/O port characteristics for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI).

Symbol	Parameter	Conditions	Min	Тур	Мах	Unit
		Master full duplex/receiver mode, 2.7 V < V _{DD} < 3.6 V SPI1/4/5	-	-	42	
		Master full duplex/receiver mode, 3.0 V < V _{DD} < 3.6 V SPI1/4/5	-	-	50	
		Master transmitter mode 1.7 V < V _{DD} < 3.6 V SPI1/4/5	-	-	50	
f _{SCK} 1/t _{c(SCK)}	SPI clock frequency	Master mode 1.7 V < V _{DD} < 3.6 V SPI1/2/3/4/5	-	-	25	MHz
		Slave transmitter/full duplex mode 2.7 V < V_{DD} < 3.6 V SPI1/4/5	-	-	38 ⁽²⁾	
		Slave receiver mode, 1.8 V < V _{DD} < 3.6 V SPI1/4/5	-	-	50	
		Slave mode, 1.8 V < V _{DD} < 3.6 V SPI1/2/3/4/5	-	-	25	
Duty(SCK)	Duty cycle of SPI clock frequency	Slave mode	30	50	70	%
t _{w(SCKH)} t _{w(SCKL)}	SCK high and low time	Master mode, SPI presc = 2	T _{PCLK} –1.5	T _{PCLK}	Т _{РСLК} +1.5	ns
t _{su(NSS)}	NSS setup time	Slave mode, SPI presc = 2	3T _{PCLK}	-	-	ns
t _{h(NSS)}	NSS hold time	Slave mode, SPI presc = 2	2T _{PCLK}	-	-	ns
t _{su(MI)}	Data input setup time	Master mode	4	-	-	ns
t _{su(SI)}		Slave mode	2.5	-	-	ns
t _{h(MI)}	Data input hold time	Master mode	7.5	-	-	ns
t _{h(SI)}		Slave mode	3.5	-	-	ns

Table 60. SPI dynamic charact	eristics ⁽¹⁾
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Symbol	Parameter	Conditions	Min	Тур	Max	Unit
t _{a(SO})	Data output access time	Slave mode	7	-	21	ns
t _{dis(SO)}	Data output disable time	Slave mode	5	-	12	ns
+	t _{v(SO)} Data output valid time	Slave mode (after enable edge), 2.7 V < V_{DD} < 3.6 V	-	11	13	ns
t _{v(SO)}		Slave mode (after enable edge), 1.7 V < V_{DD} < 3.6 V	-	11	18.5	ns
t _{h(SO)}	Data output hold time	Slave mode (after enable edge), 1.7 V < V_{DD} < 3.6 V	8	-	-	ns
t _{v(MO)}	Data output valid time	Master mode (after enable edge)	-	4	6	ns
t _{h(MO)}	Data output hold time	Master mode (after enable edge)	0	-	-	ns

Table 60. SPI dynamic	characteristics ⁽¹⁾	(continued)
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1. Guaranteed by characterization results.

2. Maximum frequency in Slave transmitter mode is determined by the sum of $t_{v(SO)}$ and $t_{su(MI)}$ which has to fit into SCK low or high phase preceding the SCK sampling edge. This value can be achieved when the SPI communicates with a master having $t_{su(MI)} = 0$ while Duty(SCK) = 50%







Symbol	Parameter	Test conditions	Min	Тур	Max	Unit
ENOB	Effective number of bits	fade =18 MHz	10.3	10.4	-	bits
SINAD	Signal-to-noise and distortion ratio	$V_{DDA} = V_{REF+} = 1.7 V$	64	64.2	-	
SNR	Signal-to-noise ratio	Input Frequency = 20 KHz	64	65	-	dB
THD	Total harmonic distortion	Iemperature = 25 °C	-	-72	-67	

Table 69. ADC dynamic accuracy at f_{ADC} = 18 MHz - limited test conditions⁽¹⁾

1. Guaranteed by characterization results.

Table 70. ADC dynamic accuracy at f_{ADC} = 36 MHz - limited test conditions⁽¹⁾

Symbol	Parameter	Test conditions	Min	Тур	Max	Unit
ENOB	Effective number of bits	fade = 36 MHz	10.6	10.8	-	bits
SINAD	Signal-to noise and distortion ratio	$V_{DDA} = V_{REF+} = 3.3 V$	66	67	-	
SNR	Signal-to noise ratio	Input Frequency = 20 KHz	64	68	-	dB
THD	Total harmonic distortion	Temperature = 25 °C	-	-72	-70	

1. Guaranteed by characterization results.

Note: ADC accuracy vs. negative injection current: injecting a negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents.

Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in Section 6.3.16 does not affect the ADC accuracy.





Figure 40. ADC accuracy characteristics

- 1. See also Table 67.
- 2. Example of an actual transfer curve.
- 3. Ideal transfer curve.
- 4. End point correlation line.

 E_T = Total Unadjusted Error: maximum deviation between the actual and the ideal transfer curves. EO = Offset Error: deviation between the first actual transition and the first ideal one. EG = Gain Error: deviation between the last ideal transition and the last actual one.

EG = Gain Error: deviation between the last ideal transition and the last actual one. ED = Differential Linearity Error: maximum deviation between actual steps and the ideal one. EL = Integral Linearity Error: maximum deviation between any actual transition and the end point correlation line.





- 1. Refer to Table 65 for the values of $\mathsf{R}_{AIN},\,\mathsf{R}_{ADC}$ and $\mathsf{C}_{ADC}.$
- C_{parasitic} represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 5 pF). A high C_{parasitic} value downgrades conversion accuracy. To remedy this, f_{ADC} should be reduced.



General PCB design guidelines

Power supply decoupling should be performed as shown in *Figure 42* or *Figure 43*, depending on whether V_{REF+} is connected to V_{DDA} or not. The 10 nF capacitors should be ceramic (good quality). They should be placed them as close as possible to the chip.





1. V_{REF+} and V_{REF-} inputs are both available on UFBGA100. V_{REF+} is also available on LQFP100. When V_{REF+} and V_{REF-} are not available, they are internally connected to V_{DDA} and V_{SSA} .



Symbol	Parameter	Conditions	Min	Тур	Мах	Unit	
f _{PP}	Clock frequency in data transfer mode	-	0	-	50	MHz	
-	SDIO_CK/fPCLK2 frequency ratio	-	-	-	8/3	-	
t _{W(CKL)}	Clock low time	fpp = 50 MHz	10.5	11	-	ne	
t _{W(CKH)}	Clock high time	fpp = 50 MHz	8.5	9	-	115	
CMD, D in	puts (referenced to CK) in MMC and	SD HS mode					
t _{ISU}	Input setup time HS	fpp = 50 MHz	2.5	-	-		
tıн	Input hold time HS	fpp = 50 MHz -40°C <t<sub>A< 125°C</t<sub>	5	-	-	ns	
		fpp = 50 MHz -40°C <t<sub>A<+85°C</t<sub>	2.5	-	-		
CMD, D o	utputs (referenced to CK) in MMC an	d SD HS mode					
t _{OV}	Output valid time HS	fpp = 50 MHz	-	3.5	4	20	
t _{OH}	Output hold time HS	fpp = 50 MHz	2	-	-	115	
CMD, D in	puts (referenced to CK) in SD defau	lt mode					
t _{ISUD}	Input setup time SD	fpp = 25 MHz	3	-	-	-	
t _{IHD}	Input hold time SD	fpp = 25 MHz	4	-	-	115	
CMD, D outputs (referenced to CK) in SD default mode							
t _{OVD}	Output valid default time SD	fpp =25 MHz	-	5	5.5		
t _{OHD}	Output hold default time SD	fpp =25 MHz	4.5	-	-	115	

Table 76. Dy	ynamic characteristics: \$	SD / MMC	characteristics ⁽¹⁾	(2)
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1. Guaranteed by characterization results.

2. V_{DD} = 2.7 to 3.6 V.



7.6 Thermal characteristics

The maximum chip junction temperature (T_Jmax) must never exceed the values given in *Table 14: General operating conditions on page 59.*

The maximum chip-junction temperature, T_J max., in degrees Celsius, may be calculated using the following equation:

 $T_J \max = T_A \max + (PD \max x \Theta_{JA})$

Where:

- T_A max is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in ° C/W,
- PD max is the sum of P_{INT} max and P_{I/O} max (PD max = P_{INT} max + P_{I/O}max),
- P_{INT} max is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.

 $\mathsf{P}_{\mathsf{I}\!/\!\mathsf{O}}$ max represents the maximum power dissipation on output pins where:

 $\mathsf{P}_{\mathsf{I/O}} \max = \Sigma \; (\mathsf{V}_{\mathsf{OL}} \times \mathsf{I}_{\mathsf{OL}}) + \Sigma ((\mathsf{V}_{\mathsf{DD}} - \mathsf{V}_{\mathsf{OH}}) \times \mathsf{I}_{\mathsf{OH}}),$

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Symbol	Parameter	Value	Unit
Θ _{JA}	Thermal resistance junction-ambient UFQFPN48	32	
	Thermal resistance junction-ambient WLCSP49	51	
	Thermal resistance junction-ambient LQFP64	47	°C/W
	Thermal resistance junction-ambient LQFP100	43	
	Thermal resistance junction-ambient UFBGA100	62	

Table 85. Package thermal characteristics

7.6.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org.

