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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	I²C, IrDA, LINbus, MMC/SD/SDIO, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	81
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f411vet6

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2 Description

The STM32F411xC/xE devices are based on the high-performance ARM® Cortex®-M4 32-bit RISC core operating at a frequency of up to 100 MHz. The Cortex®-M4 core features a Floating point unit (FPU) single precision which supports all ARM single-precision data-processing instructions and data types. It also implements a full set of DSP instructions and a memory protection unit (MPU) which enhances application security.

The STM32F411xC/xE belongs to the STM32 Dynamic Efficiency™ product line (with products combining power efficiency, performance and integration) while adding a new innovative feature called Batch Acquisition Mode (BAM) allowing to save even more power consumption during data batching.

The STM32F411xC/xE incorporate high-speed embedded memories (up to 512 Kbytes of Flash memory, 128 Kbytes of SRAM), and an extensive range of enhanced I/Os and peripherals connected to two APB buses, two AHB bus and a 32-bit multi-AHB bus matrix.

All devices offer one 12-bit ADC, a low-power RTC, six general-purpose 16-bit timers including one PWM timer for motor control, two general-purpose 32-bit timers. They also feature standard and advanced communication interfaces.

- Up to three I^2Cs
- Five SPIs
- Five I^2Ss out of which two are full duplex. To achieve audio class accuracy, the I^2S peripherals can be clocked via a dedicated internal audio PLL or via an external clock to allow synchronization.
- Three USARTs
- SDIO interface
- USB 2.0 OTG full speed interface

Refer to *Table 2: STM32F411xC/xE features and peripheral counts* for the peripherals available for each part number.

The STM32F411xC/xE operate in the - 40 to + 125 °C temperature range from a 1.7 (PDR OFF) to 3.6 V power supply. A comprehensive set of power-saving mode allows the design of low-power applications.

These features make the STM32F411xC/xE microcontrollers suitable for a wide range of applications:

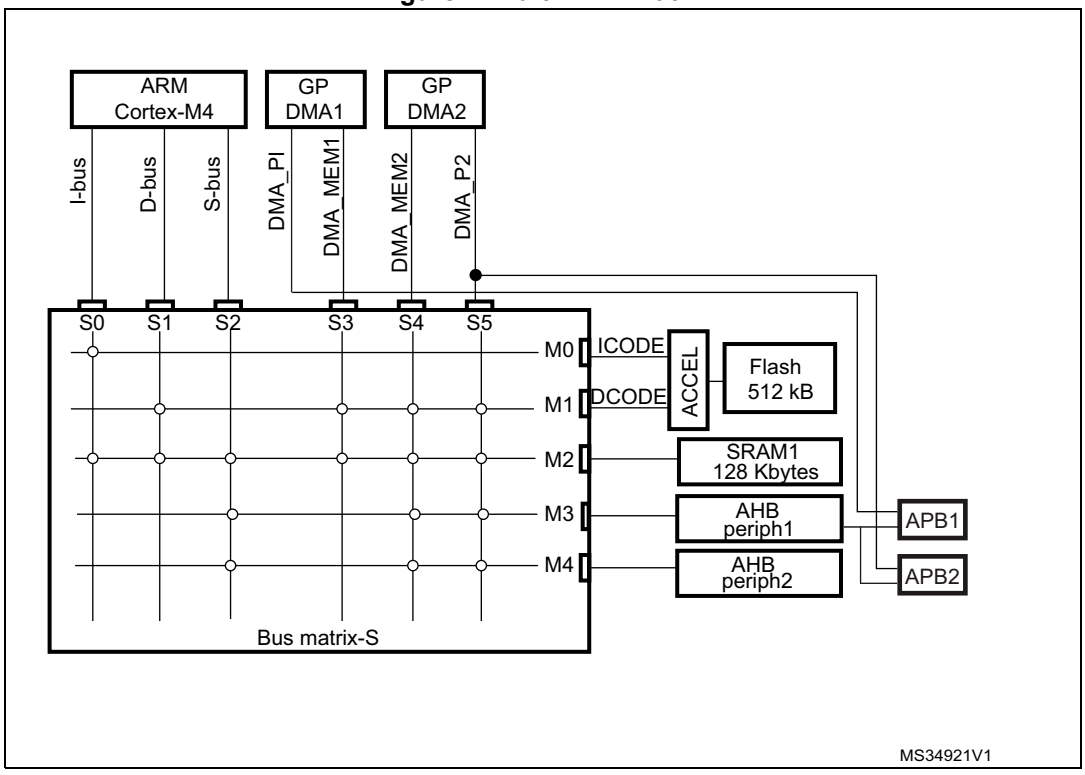
- Motor drive and application control
- Medical equipment
- Industrial applications: PLC, inverters, circuit breakers
- Printers, and scanners
- Alarm systems, video intercom, and HVAC
- Home audio appliances
- Mobile phone sensor hub

Figure 3 shows the general block diagram of the devices.

3.8 Multi-AHB bus matrix

The 32-bit multi-AHB bus matrix interconnects all the masters (CPU, DMAs) and the slaves (Flash memory, RAM, AHB and APB peripherals) and ensures a seamless and efficient operation even when several high-speed peripherals work simultaneously.

Figure 4. Multi-AHB matrix



3.9 DMA controller (DMA)

The devices feature two general-purpose dual-port DMAs (DMA1 and DMA2) with 8 streams each. They are able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. They feature dedicated FIFOs for APB/AHB peripherals, support burst transfer and are designed to provide the maximum peripheral bandwidth (AHB/APB).

The two DMA controllers support circular buffer management, so that no specific code is needed when the controller reaches the end of the buffer. The two DMA controllers also have a double buffering feature, which automates the use and switching of two memory buffers without requiring any special code.

Each stream is connected to dedicated hardware DMA requests, with support for software trigger on each stream. Configuration is made by software and transfer sizes between source and destination are independent.

3.16.3 Regulator ON/OFF and internal power supply supervisor availability

Table 3. Regulator ON/OFF and internal power supply supervisor availability

Package	Regulator ON	Regulator OFF	Power supply supervisor ON	Power supply supervisor OFF
UFQFPN48	Yes	No	Yes	No
WLCSP49	Yes	No	Yes PDR_ON set to VDD	Yes PDR_ON external control(1)
LQFP64	Yes	No	Yes	No
LQFP100	Yes	No	Yes	No
UFBGA100	Yes BYPASS_REG set to VSS	Yes BYPASS_REG set to VDD	Yes PDR_ON set to VDD	Yes PDR_ON external control (1)

1. Refer to *Section 3.15: Power supply supervisor*

3.17 Real-time clock (RTC) and backup registers

The backup domain includes:

- The real-time clock (RTC)
- 20 backup registers

The real-time clock (RTC) is an independent BCD timer/counter. Dedicated registers contain the second, minute, hour (in 12/24 hour), week day, date, month, year, in BCD (binary-coded decimal) format. Correction for 28, 29 (leap year), 30, and 31 day of the month are performed automatically. The RTC features a reference clock detection, a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision. The RTC provides a programmable alarm and programmable periodic interrupts with wakeup from Stop and Standby modes. The sub-seconds value is also available in binary format.

It is clocked by a 32.768 kHz external crystal, resonator or oscillator, the internal low-power RC oscillator or the high-speed external clock divided by 128. The internal low-speed RC has a typical frequency of 32 kHz. The RTC can be calibrated using an external 512 Hz output to compensate for any natural quartz deviation.

Two alarm registers are used to generate an alarm at a specific time and calendar fields can be independently masked for alarm comparison. To generate a periodic interrupt, a 16-bit programmable binary auto-reload downcounter with programmable resolution is available and allows automatic wakeup and periodic alarms from every 120 µs to every 36 hours.

A 20-bit prescaler is used for the time base clock. It is by default configured to generate a time base of 1 second from a clock at 32.768 kHz.

The backup registers are 32-bit registers used to store 80 bytes of user application data when V_{DD} power is not present. Backup registers are not reset by a system, a power reset, or when the device wakes up from the Standby mode (see *Section 3.18: Low-power modes*).

Additional 32-bit registers contain the programmable alarm subseconds, seconds, minutes, hours, day, and date.

The RTC and backup registers are supplied through a switch that is powered either from the V_{DD} supply when present or from the V_{BAT} pin.

3.18 Low-power modes

The devices support three low-power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

- **Sleep mode**

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

  To further reduce the power consumption, the Flash memory can be switched off before entering in Sleep mode. Note that this requires a code execution from the RAM.

- **Stop mode**

  The Stop mode achieves the lowest power consumption while retaining the contents of SRAM and registers. All clocks in the 1.2 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled. The voltage regulator can also be put either in normal or in low-power mode.

  The devices can be woken up from the Stop mode by any of the EXTI line (the EXTI line source can be one of the 16 external lines, the PVD output, the RTC alarm/ wakeup/ tamper/ time stamp events).

- **Standby mode**

  The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.2 V domain is powered off. The PLL, the HSI RC and the HSE crystal oscillators are also switched off. After entering Standby mode, the SRAM and register contents are lost except for registers in the backup domain when selected.

  The devices exit the Standby mode when an external reset (NRST pin), an IWDG reset, a rising edge on the WKUP pin, or an RTC alarm/ wakeup/ tamper/time stamp event occurs.

  Standby mode is not supported when the embedded voltage regulator is bypassed and the 1.2 V domain is controlled by an external power.

3.19 V_{BAT} operation

The VBAT pin allows to power the device V_{BAT} domain from an external battery, an external super-capacitor, or from V_{DD} when no external battery and an external super-capacitor are present.

V_{BAT} operation is activated when V_{DD} is not present.

The VBAT pin supplies the RTC and the backup registers.

Note: When the microcontroller is supplied from VBAT, external interrupts and RTC alarm/events do not exit it from V_{BAT} operation. When PDR_ON pin is not connected to V_{DD} (internal Reset OFF), the V_{BAT} functionality is no more available and VBAT pin should be connected to V_{DD}.

Table 9. Alternate function mapping (continued)

Port		AF00	AF01	AF02	AF03	AF04	AF05	AF06	AF07	AF08	AF09	AF10	AF11	AF12	AF13	AF14	AF15
		SYS_AF	TIM1/TIM2	TIM3/ TIM4/ TIM5	TIM9/ TIM10/ TIM11	I2C1/I2C2/ I2C3	SPI1/I2S1SPI2/ I2S2/SPI3/ I2S3	SPI2/I2S2/ SPI3/ I2S3/SPI4/ I2S4/SPI5/ I2S5	SPI3/I2S3/ USART1/ USART2	USART6	I2C2/ I2C3	OTG1_FS		SDIO			
Port C	PC0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
	PC1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
	PC2	-	-	-	-	-	SPI2_MISO	I2S2ext_SD	-	-	-	-	-	-	-	-	EVENT OUT
	PC3	-	-	-	-	-	SPI2_MOSI /I2S2_SD	-	-	-	-	-	-	-	-	-	EVENT OUT
	PC4	-	-	-	-	-		-	-	-	-	-	-	-	-	-	EVENT OUT
	PC5	-	-	-	-	-		-	-	-	-	-	-	-	-	-	EVENT OUT
	PC6	-	-	TIM3_CH1	-	-	I2S2_MCK	-	-	USART6_ TX	-	-	-	SDIO_ D6	-	-	EVENT OUT
	PC7	-	-	TIM3_CH2	-	-	SPI2_SCK/I 2S2_CK	I2S3_MCK	-	USART6_ RX	-	-	-	SDIO_ D7	-	-	EVENT OUT
	PC8	-	-	TIM3_CH3	-	-	-	-	-	USART6_ CK	-	-	-	SDIO_ D0	-	-	EVENT OUT
	PC9	MCO_2	-	TIM3_CH4	-	I2C3_SDA	I2S2_CKIN	-	-		-	-	-	SDIO_ D1	-	-	EVENT OUT
	PC10	-	-	-	-	-	-	SPI3_SCK/I2 S3_CK	-	-	-	-	-	SDIO_ D2	-	-	EVENT OUT
	PC11	-	-	-	-	-	I2S3ext_SD	SPI3_MISO	-	-	-	-	-	SDIO_ D3	-	-	EVENT OUT
	PC12	-	-	-	-	-	-	SPI3_MOSI/I 2S3_SD	-	-	-	-	-	SDIO_ CK	-	-	EVENT OUT
	PC13	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	PC14	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	PC15	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

5 Memory mapping

The memory map is shown in *Figure 14*.

Figure 14. Memory map

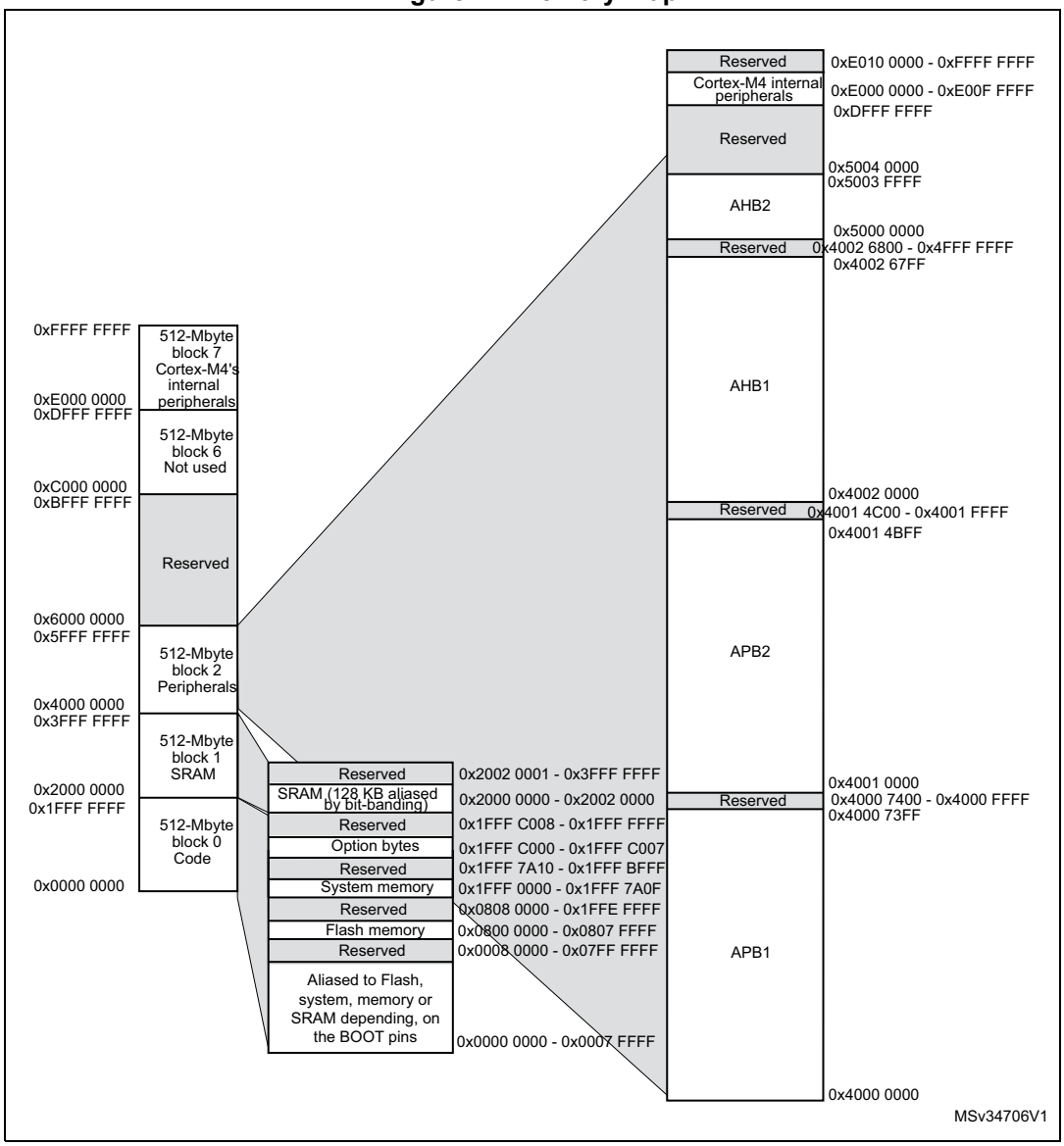


Table 10. STM32F411xC/xE register boundary addresses

Bus	Boundary address	Peripheral
	0xE010 0000 - 0xFFFF FFFF	Reserved
Cortex®-M4	0xE000 0000 - 0xE00F FFFF	Cortex-M4 internal peripherals
	0x5004 0000 - 0xDFFF FFFF	Reserved

Table 22. Typical and maximum current consumption in run mode, code with data processing (ART accelerator enabled except prefetch) running from Flash memory- V_{DD} = 1.7 V

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Typ	Max(1)				Unit
					T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	T_A= 125 °C	
I_{DD}	Supply current in **Run mode**	External clock, PLL ON(2), all peripherals enabled(3)(4)	100	20.4	21.8	22.1	22.8	23.8	mA
			84	16.5	17.6	17.8	18.6	19.6	
			64	11.4	12.3	12.5	13.1	14.1	
			50	9.0	9.7	10.0	10.6	11.6	
			20	4.6	5.0	5.3	6.0	7.0	
		HSI, PLL OFF(2), all peripherals enabled(3)	16	2.9	3.2	3.6	4.3	5.3	
			1	0.7	0.8	1.3	1.9	2.9	
		External clock, PLL ON(2) all peripherals disabled(3)	100	11.2	12.2	12.4	13.2	14.2	
			84	9.1	9.9	10.1	10.9	11.9	
			64	6.4	7.0	7.3	7.9	8.9	
			50	5.1	5.6	5.9	6.6	7.6	
			20	2.6	3.0	3.3	4.0	5.0	
		HSI, PLL OFF(2), all peripherals disabled(3)	16	1.8	2.0	2.4	3.0	4.0	
			1	0.6	0.7	1.2	1.9	2.9	

1. Guaranteed by characterization results.
2. Refer to *Table 41* and RM0383 for the possible PLL VCO setting
3. Add an additional power consumption of 1.6 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is ON (ADON bit is set in the ADC_CR2 register).
4. When the ADC is ON (ADON bit set in the ADC_CR2), add an additional power consumption of 1.6mA per ADC for the analog part.

Table 32. Switching output I/O current consumption

Symbol	Parameter	Conditions[1]	I/O toggling frequency (f_{SW})	Typ	Unit
IDDIO	I/O switching current	V_{DD} = 3.3 V C = C_{INT}	2 MHz	0.05	mA
			8 MHz	0.15	
			25 MHz	0.45	
			50 MHz	0.85	
			60 MHz	1.00	
			84 MHz	1.40	
			90 MHz	1.67	
		V_{DD} = 3.3 V C_{EXT} = 0 pF C = C_{INT} + C_{EXT} + C_S	2 MHz	0.10	
			8 MHz	0.35	
			25 MHz	1.05	
			50 MHz	2.20	
			60 MHz	2.40	
			84 MHz	3.55	
			90 MHz	4.23	
		V_{DD} = 3.3 V C_{EXT} =10 pF C = C_{INT} + C_{EXT} + C_S	2 MHz	0.20	
			8 MHz	0.65	
			25 MHz	1.85	
			50 MHz	2.45	
			60 MHz	4.70	
			84 MHz	8.80	
			90 MHz	10.47	
		V_{DD} = 3.3 V C_{EXT} = 22 pF C = C_{INT} + C_{EXT} + C_S	2 MHz	0.25	
			8 MHz	1.00	
			25 MHz	3.45	
			50 MHz	7.15	
			60 MHz	11.55	
		V_{DD} = 3.3 V C_{EXT} = 33 pF C = C_{INT} + C_{EXT} + C_S	2 MHz	0.32	
			8 MHz	1.27	
			25 MHz	3.88	
			50 MHz	12.34	

1. CS is the PCB board capacitance including the pad pin. CS = 7 pF (estimated value).

On-chip peripheral current consumption

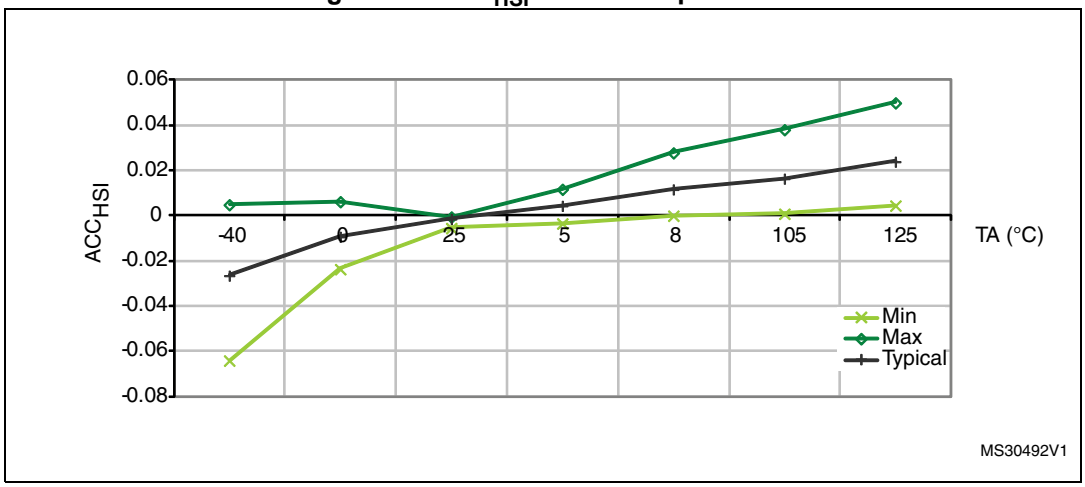
The MCU is placed under the following conditions:

- At startup, all I/O pins are in analog input configuration.
- All peripherals are disabled unless otherwise mentioned.
- The ART accelerator is ON.
- Voltage Scale 2 mode selected, internal digital voltage V12 = 1.26 V.
- HCLK is the system clock at 84 MHz. $f_{PCLK1} = f_{HCLK}/2$, and $f_{PCLK2} = f_{HCLK}$.
  The given value is calculated by measuring the difference of current consumption
  - with all peripherals clocked off
  - with only one peripheral clocked on
- Ambient operating temperature is 25 °C and V_{DD}=3.3 V.

Table 33. Peripheral current consumption

Peripheral		I_{DD} (Typ)	Unit
AHB1 (up to 100 MHz)	GPIOA	1.55	µA/MHz
	GPIOB	1.55	
	GPIOC	1.55	
	GPIOD	1.55	
	GPIOE	1.55	
	GPIOH	1.55	
	CRC	0.36	
	DMA1(1)	14.96	
	DMA1(2)	1.54N+2.66	
	DMA2(1)	14.96	
	DMA2(2)	1.54N+2.66	
APB1 (up to 50 MHz)	TIM2	11.19	µA/MHz
	TIM3	8.57	
	TIM4	8.33	
	TIM5	11.19	
	PWR	0.71	
	USART2	3.33	
	I2C1/2/3	3.10	
	SPI2(3)	2.62	
	SPI3(3)	2.86	
	I2S2	1.90	
	I2S3	1.67	
	WWDG	0.71	

Figure 26. ACC_{HSI} versus temperature



1. Guaranteed by characterization results.

Low-speed internal (LSI) RC oscillator

Table 40. LSI oscillator characteristics (1)

Symbol	Parameter	Min	Typ	Max	Unit
f_{LSI}(2)	Frequency	17	32	47	kHz
$t_{su(LSI)}$(3)	LSI oscillator startup time	-	15	40	µs
$I_{DD(LSI)}$(3)	LSI oscillator power consumption	-	0.4	0.6	µA

1. V_{DD} = 3 V, T_A = –40 to 125 °C unless otherwise specified.
2. Guaranteed by characterization results.
3. Guaranteed by design.

6.3.11 PLL spread spectrum clock generation (SSCG) characteristics

The spread spectrum clock generation (SSCG) feature allows to reduce electromagnetic interferences (see *Table 49: EMI characteristics for LQFP100*). It is available only on the main PLL.

Table 43. SSCG parameter constraints

Symbol	Parameter	Min	Typ	Max(1)	Unit
f_{Mod}	Modulation frequency	-	-	10	kHz
md	Peak modulation depth	0.25	-	2	%
MODEPER * INCSTEP	(Modulation period) * (Increment Step)	-	-	2^{15}-1	-

1. Guaranteed by design.

Equation 1

The frequency modulation period (MODEPER) is given by the equation below:

$$MODEPER = round[f_{PLL\_IN} / (4 \times f_{Mod})]$$

f_{PLL_IN} and f_{Mod} must be expressed in Hz.

As an example:

If f_{PLL_IN} = 1 MHz, and f_{MOD} = 1 kHz, the modulation depth (MODEPER) is given by equation 1:

$$MODEPER = round[10^6 / (4 \times 10^3)] = 250$$

Equation 2

Equation 2 allows to calculate the increment step (INCSTEP):

$$INCSTEP = round[((2^{15} - 1) \times md \times PLLN) / (100 \times 5 \times MODEPER)]$$

f_{VCO_OUT} must be expressed in MHz.

With a modulation depth (md) = ±2 % (4 % peak to peak), and PLLN = 240 (in MHz):

$$INCSTEP = round[((2^{15} - 1) \times 2 \times 240) / (100 \times 5 \times 250)] = 126md(quantitazed)\%$$

An amplitude quantization error may be generated because the linear modulation profile is obtained by taking the quantized values (rounded to the nearest integer) of MODPER and INCSTEP. As a result, the achieved modulation depth is quantized. The percentage quantized modulation depth is given by the following formula:

$$md_{quantized}\% = (MODEPER \times INCSTEP \times 100 \times 5) / ((2^{15} - 1) \times PLLN)$$

As a result:

$$md_{quantized}\% = (250 \times 126 \times 100 \times 5) / ((2^{15} - 1) \times 240) = 2.002\%(peak)$$

Table 48. EMS characteristics for LQFP100 package

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, LQFP100, WLCSP49, T_A = +25 °C, f_{HCLK} = 100 MHz, conforms to IEC 61000-4-2	2B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, LQFP100, WLCSP49, T_A = +25 °C, f_{HCLK} = 100 MHz, conforms to IEC 61000-4-4	4A

When the application is exposed to a noisy environment, it is recommended to avoid pin exposition to disturbances. The pins showing a middle range robustness are: PA0, PA1, PA2, on LQFP100 packages and PDR_ON on WLCSP49.

As a consequence, it is recommended to add a serial resistor (1 kΩ maximum) located as close as possible to the MCU to the pins exposed to noise (connected to tracks longer than 50 mm on PCB).

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Table 60. SPI dynamic characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{a(SO)}$	Data output access time	Slave mode	7	-	21	ns
$t_{dis(SO)}$	Data output disable time	Slave mode	5	-	12	ns
$t_{v(SO)}$	Data output valid time	Slave mode (after enable edge), 2.7 V < V_{DD} < 3.6 V	-	11	13	ns
		Slave mode (after enable edge), 1.7 V < V_{DD} < 3.6 V	-	11	18.5	ns
$t_{h(SO)}$	Data output hold time	Slave mode (after enable edge), 1.7 V < V_{DD} < 3.6 V	8	-	-	ns
$t_{v(MO)}$	Data output valid time	Master mode (after enable edge)	-	4	6	ns
$t_{h(MO)}$	Data output hold time	Master mode (after enable edge)	0	-	-	ns

1. Guaranteed by characterization results.
2. Maximum frequency in Slave transmitter mode is determined by the sum of $t_{v(SO)}$ and $t_{su(MI)}$ which has to fit into SCK low or high phase preceding the SCK sampling edge. This value can be achieved when the SPI communicates with a master having $t_{su(MI)}$ = 0 while Duty(SCK) = 50%

Figure 34. SPI timing diagram - slave mode and CPHA = 0

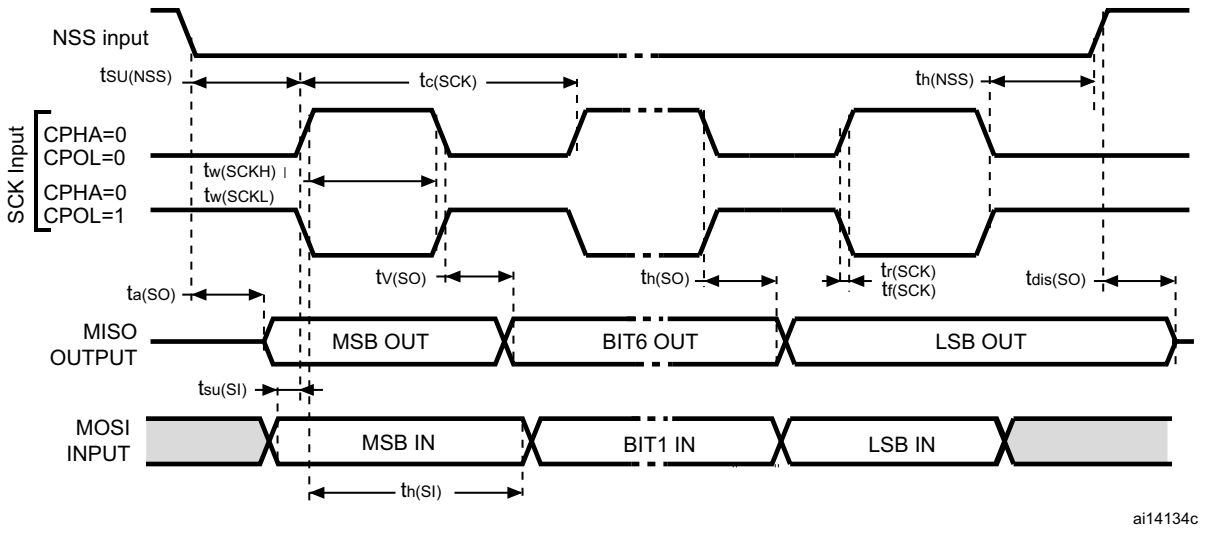
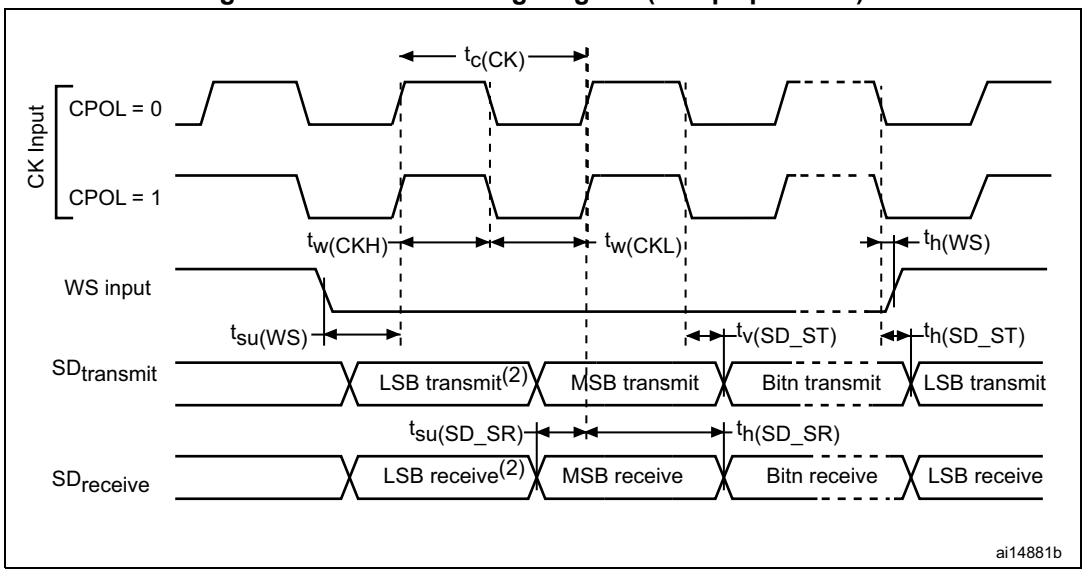
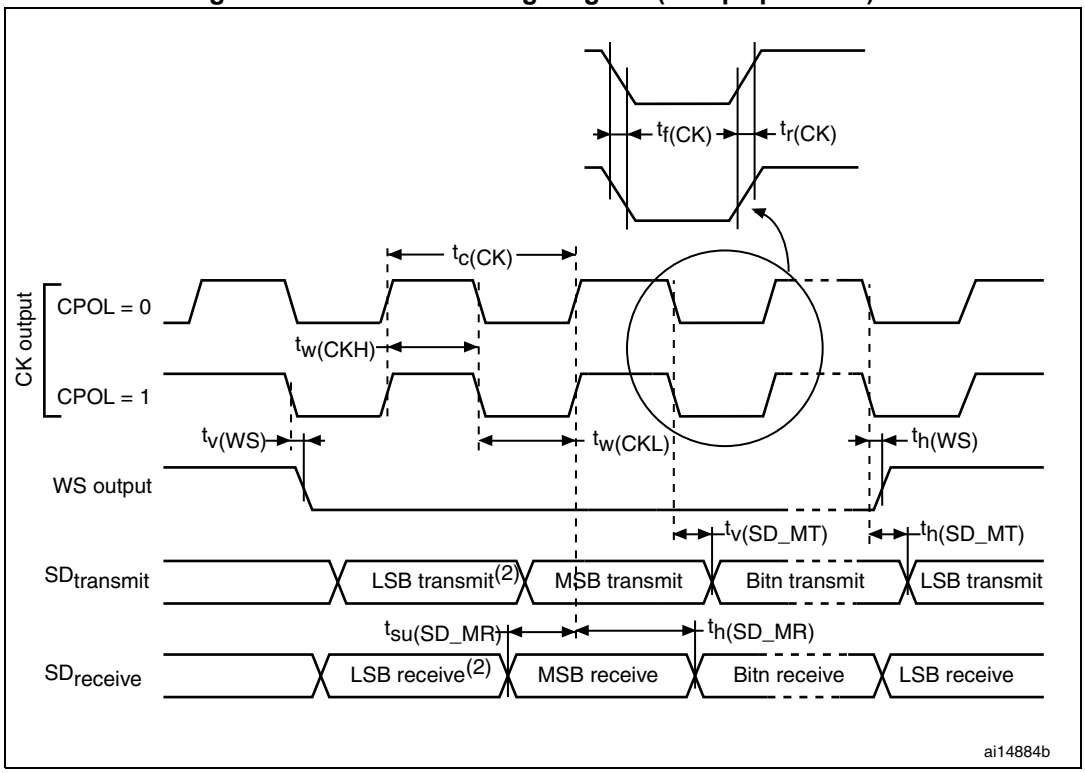


Figure 37. I²S slave timing diagram (Philips protocol)(1)



1. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Figure 38. I²S master timing diagram (Philips protocol)(1)



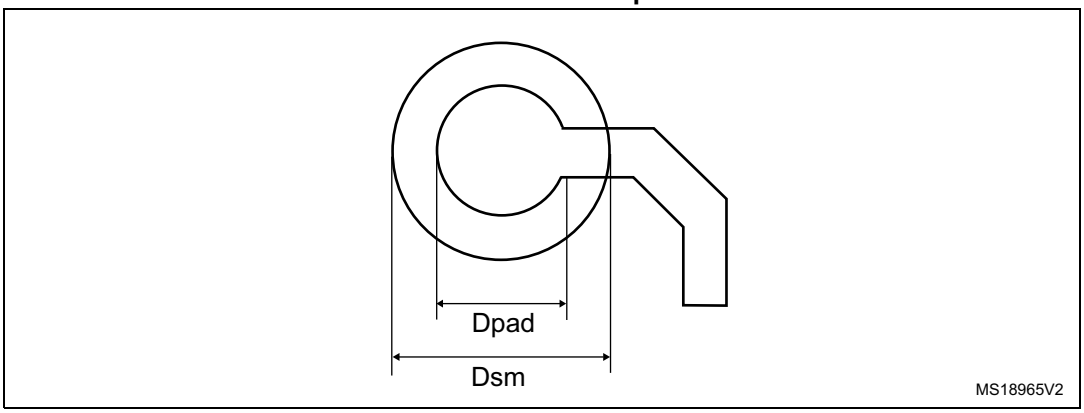
1. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Table 79. WLCSP49 - 49-ball, 2.999 x 3.185 mm, 0.4 mm pitch wafer level chip scale package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.525	0.555	0.585	0.0207	0.0219	0.0230
A1	-	0.175	-	-	0.0069	-
A2	-	0.380	-	-	0.0150	-
A3[2]	-	0.025	-	-	0.0010	-
b[3]	0.220	0.250	0.280	0.0087	0.0098	0.0110
D	2.964	2.999	3.034	0.1167	0.1181	0.1194
E	3.150	3.185	3.220	0.1240	0.1254	0.1268
e	-	0.400	-	-	0.0157	-
e1	-	2.400	-	-	0.0945	-
e2	-	2.400	-	-	0.0945	-
F	-	0.2995	-	-	0.0118	-
G	-	0.3925	-	-	0.0155	-
aaa	-	0.100	-	-	0.0039	-
bbb	-	0.100	-	-	0.0039	-
ccc	-	0.100	-	-	0.0039	-
ddd	-	0.050	-	-	0.0020	-
eee	-	0.050	-	-	0.0020	-

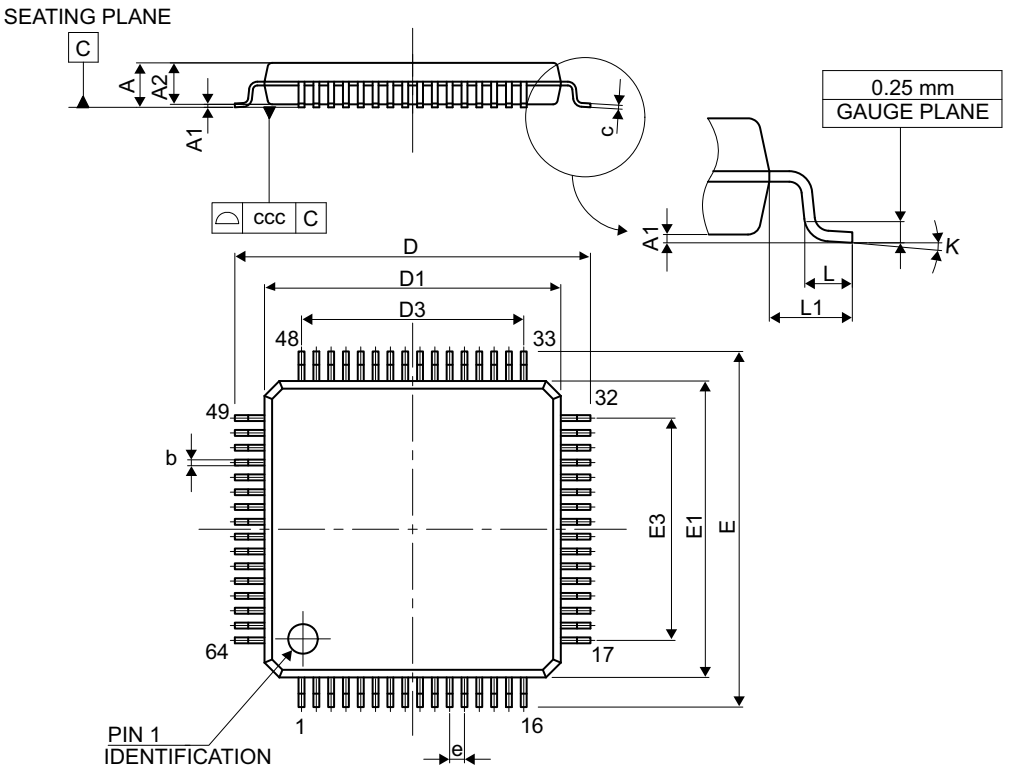
1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. Back side coating
3. Dimension is measured at the maximum bump diameter parallel to primary datum Z.

Figure 47. WLCSP49 - 49-ball, 2.999 x 3.185 mm, 0.4 mm pitch wafer level chip scale recommended footprint



7.3 LQFP64 package information

Figure 52. LQFP64 - 64-pin, 10 x 10 mm, 64-pin low-profile quad flat package outline

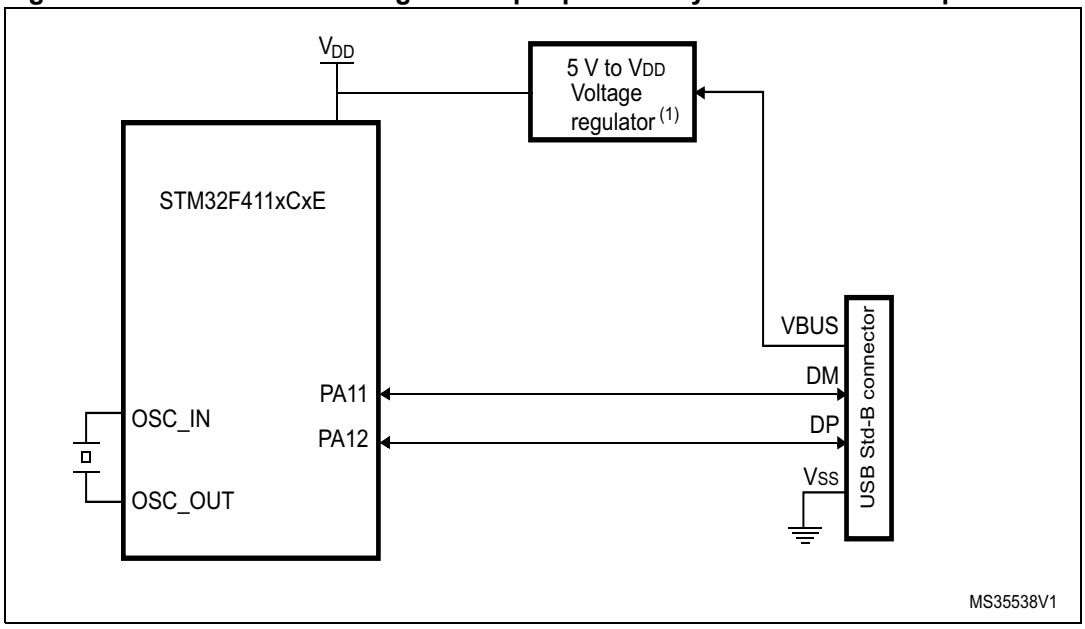


1. Drawing is not to scale.

Appendix B Application block diagrams

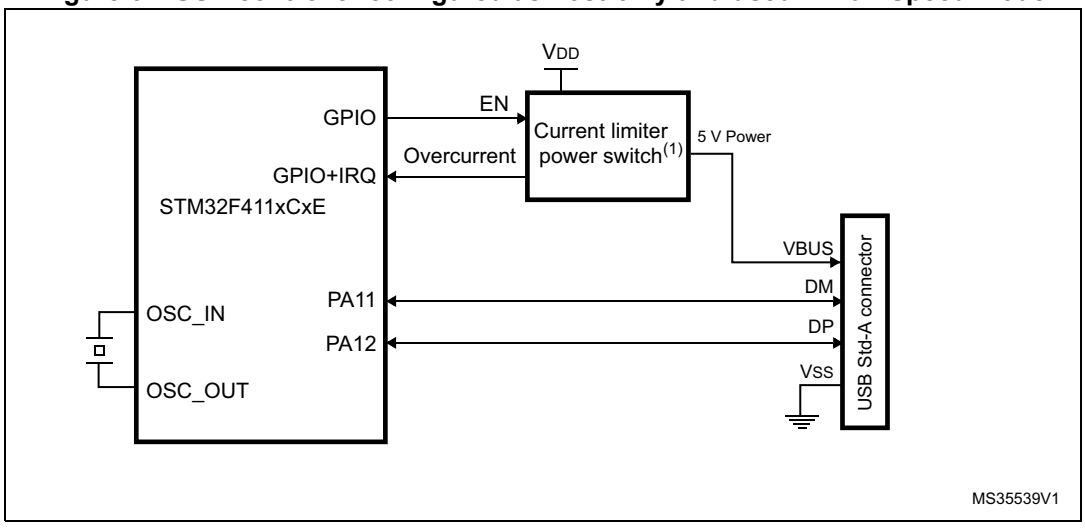
B.1 USB OTG Full Speed (FS) interface solutions

Figure 61. USB controller configured as peripheral-only and used in Full-Speed mode



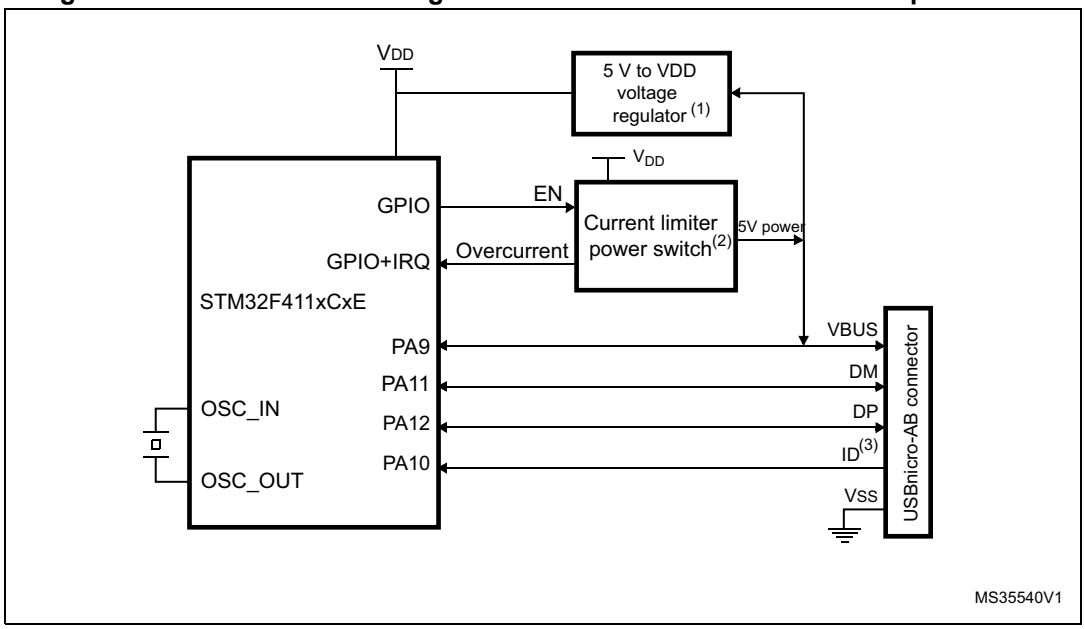
1. The external voltage regulator is only needed when building a V_{BUS} powered device.

Figure 62. USB controller configured as host-only and used in Full-Speed mode



1. The current limiter is required only if the application has to support a V_{BUS} powered device. A basic power switch can be used if 5V are available on the application board.

Figure 63. USB controller configured in dual mode and used in Full-Speed mode



1. The external voltage regulator is only needed when building a V_{BUS} powered device.
2. The current limiter is required only if the application has to support a V_{BUS} powered device. A basic power switch can be used if 5 V are available on the application board.
3. The ID pin is required in dual role only.

Revision history

Table 88. Document revision history

Date	Revision	Changes
19-Jun-2014	1	Initial release.
10-Sep-2014	2	Introduced the BAM feature in *Features*, *Section 2: Description*., and *Section 3.3: Batch Acquisition mode (BAM)*. Updated *Section 3.5: Embedded Flash memory*, *Section 3.14: Power supply schemes* and *Section 3.18: Low-power modes*, *Section 3.20.2: General-purpose timers (TIMx)* and *Section 3.30: Temperature sensor*. Modified *Table 8: STM32F411xC/xE pin definitions*, *Table 9: Alternate function mapping* and APB2 in *Table 10: STM32F411xC/xE register boundary addresses*. Modified *Table 34: Low-power mode wakeup timings(1)*, *Table 20: Typical and maximum current consumption, code with data processing (ART accelerator disabled) running from SRAM - VDD = 1.7 V*, *Table 21: Typical and maximum current consumption, code with data processing (ART accelerator disabled) running from SRAM - VDD = 3.6 V*, *Table 25: Typical and maximum current consumption in run mode, code with data processing (ART accelerator enabled with prefetch) running from Flash memory - VDD = 3.6 V*, *Table 26: Typical and maximum current consumption in Sleep mode - VDD = 3.6 V* and *Table 58: I2C characteristics* and *Figure 33: I2C bus AC waveforms and measurement circuit*. Added *Figure 21: Low-power mode wakeup*, *Section Appendix A: Recommendations when using the internal reset OFF* and *Section Appendix B: Application block diagrams*.
27-Nov-2014	3	Changed datasheet status to Production Data. Updated *Table 31: Typical and maximum current consumptions in VBAT mode*. *Section : On-chip peripheral current consumption*: changed HCLK frequency and updated DMA1 and DMA2 current consumption in *Table 33: Peripheral current consumption*. Updated *Table 55: I/O AC characteristics*. Updated THD in *Table 69: ADC dynamic accuracy at fADC = 18 MHz - limited test conditions* and *Table 70: ADC dynamic accuracy at fADC = 36 MHz - limited test conditions*. Updated *Table 55: I/O AC characteristics*. Updated *Figure 46: WLCSP49 - 49-ball, 2.999 x 3.185 mm, 0.4 mm pitch wafer level chip scale package outline* and *Figure 48: WLCSP49 marking (package top view)*. Added *Figure 47: WLCSP49 - 49-ball, 2.999 x 3.185 mm, 0.4 mm pitch wafer level chip scale recommended footprint* and *Table 80: WLCSP49 recommended PCB design rules (0.4 mm pitch)*. Updated *Figure 51: UFQFPN48 marking example (package top view)*, *Figure 54: LQFP64 marking example (package top view)*, *Figure 57: LQPF100 marking example (package top view)*, and *Figure 58: UFBGA100 - 100-ball, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package outline*.
04-Feb-2015	4	Added VPP alternate function for BOOT0 in *Table 8: STM32F411xC/xE pin definitions*. Added TC inputs in *Table 11: Voltage characteristics*, *Table 12: Current characteristics*, *Table 14: General operating conditions*, *Table 53: I/O static characteristics* and *Figure 30: FT/TC I/O input characteristics*. Updated $V_{ESD(CDM)}$ in *Table 50: ESD absolute maximum ratings*. A3 minimum and maximum values removed in *Table 83: UFBGA100 - 100-ball, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package mechanical data*.