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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M4 |
| Core Size | 32-Bit Single-Core |
| Speed | 100MHz |
| Connectivity | I²C, IrDA, LINbus, MMC/SD/SDIO, SPI, UART/USART, USB OTG |
| Peripherals | Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT |
| Number of I/O | 81 |
| Program Memory Size | 512KB (512K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 128K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.7V ~ 3.6V |
| Data Converters | A/D 16x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 100-LQFP |
| Supplier Device Package | 100-LQFP (14x14) |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f411vet6u |

# 3 Functional overview

## 3.1 ARM® Cortex®-M4 with FPU core with embedded Flash and SRAM

The ARM® Cortex®-M4 with FPU processor is the latest generation of ARM processors for embedded systems. It was developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced response to interrupts.

The ARM® Cortex®-M4 with FPU 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices. The processor supports a set of DSP instructions which allow efficient signal processing and complex algorithm execution. Its single precision FPU (floating point unit) speeds up software development by using metalanguage development tools, while avoiding saturation.

The STM32F411xC/xE devices are compatible with all ARM tools and software.

*Figure 3* shows the general block diagram of the STM32F411xC/xE.

*Note: Cortex®-M4 with FPU is binary compatible with Cortex®-M3.*

## 3.2 Adaptive real-time memory accelerator (ART Accelerator™)

The ART Accelerator™ is a memory accelerator which is optimized for STM32 industry-standard ARM® Cortex®-M4 with FPU processors. It balances the inherent performance advantage of the ARM® Cortex®-M4 with FPU over Flash memory technologies, which normally requires the processor to wait for the Flash memory at higher frequencies.

To release the processor full 105 DMIPS performance at this frequency, the accelerator implements an instruction prefetch queue and branch cache, which increases program execution speed from the -bit Flash memory. Based on CoreMark benchmark, the performance achieved thanks to the ART accelerator is equivalent to 0 wait state program execution from Flash memory at a CPU frequency up to 100 MHz.

## 3.3 Batch Acquisition mode (BAM)

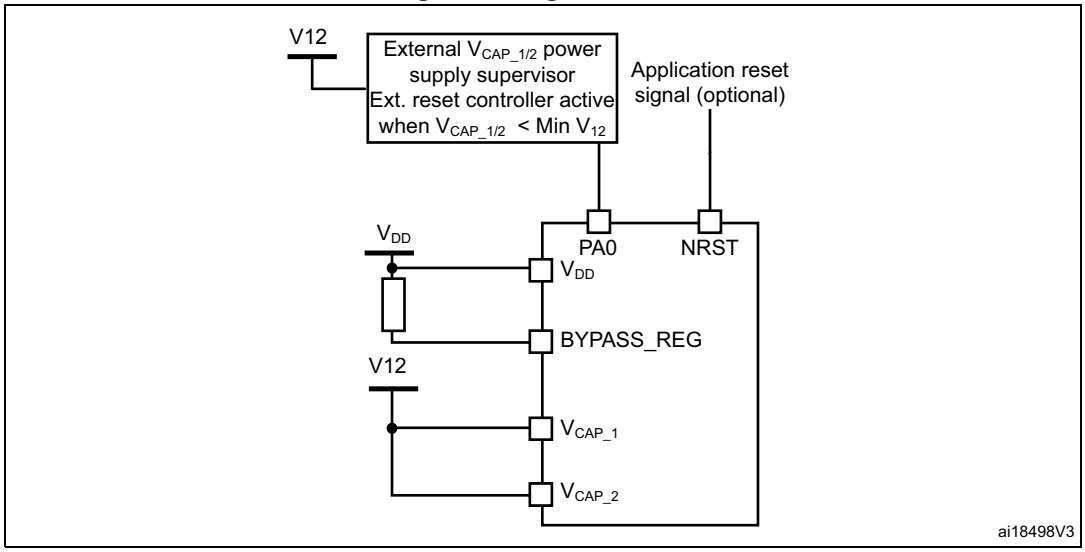
The Batch acquisition mode allows enhanced power efficiency during data batching. It enables data acquisition through any communication peripherals directly to memory using the DMA in reduced power consumption as well as data processing while the rest of the system is in low-power mode (including the flash and ART). For example in an audio system, a smart combination of PDM audio sample acquisition and processing from the I2S directly to RAM (flash and ART™ stopped) with the DMA using BAM followed by some very short processing from flash allows to drastically reduce the power consumption of the application. A dedicated application note (AN4515) describes how to implement the BAM to allow the best power efficiency.

When the regulator is OFF, there is no more internal monitoring on V12. An external power supply supervisor should be used to monitor the V12 of the logic power domain. PA0 pin should be used for this purpose, and act as power-on reset on V12 power domain.

In regulator OFF mode, the following features are no more supported:

- PA0 cannot be used as a GPIO pin since it allows to reset a part of the V12 logic power domain which is not reset by the NRST pin.
- As long as PA0 is kept low, the debug mode cannot be used under power-on reset. As a consequence, PA0 and NRST pins must be managed separately if the debug connection under reset or pre-reset is required.

**Figure 6. Regulator OFF**

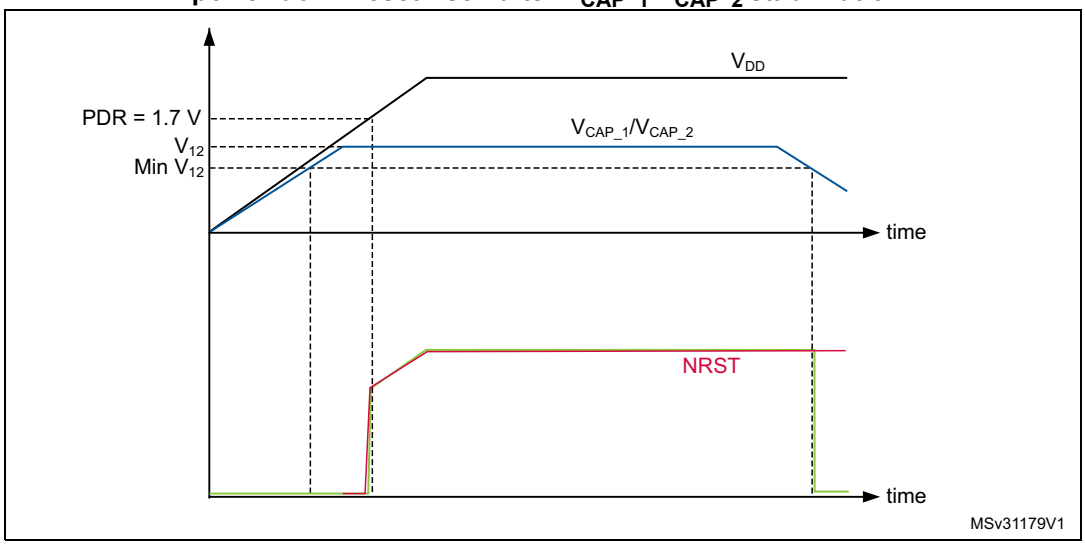



The following conditions must be respected:

- $V_{DD}$ should always be higher than $V_{CAP\_1}$ and $V_{CAP\_2}$ to avoid current injection between power domains.
- If the time for $V_{CAP\_1}$ and $V_{CAP\_2}$ to reach $V_{12}$ minimum value is faster than the time for $V_{DD}$ to reach 1.7 V, then PA0 should be kept low to cover both conditions: until $V_{CAP\_1}$ and $V_{CAP\_2}$ reach $V_{12}$ minimum value and until $V_{DD}$ reaches 1.7 V (see *Figure 7*).
- Otherwise, if the time for $V_{CAP\_1}$ and $V_{CAP\_2}$ to reach $V_{12}$ minimum value is slower than the time for $V_{DD}$ to reach 1.7 V, then PA0 could be asserted low externally (see *Figure 8*).
- If $V_{CAP\_1}$ and $V_{CAP\_2}$ go below $V_{12}$ minimum value and $V_{DD}$ is higher than 1.7 V, then a reset must be asserted on PA0 pin.

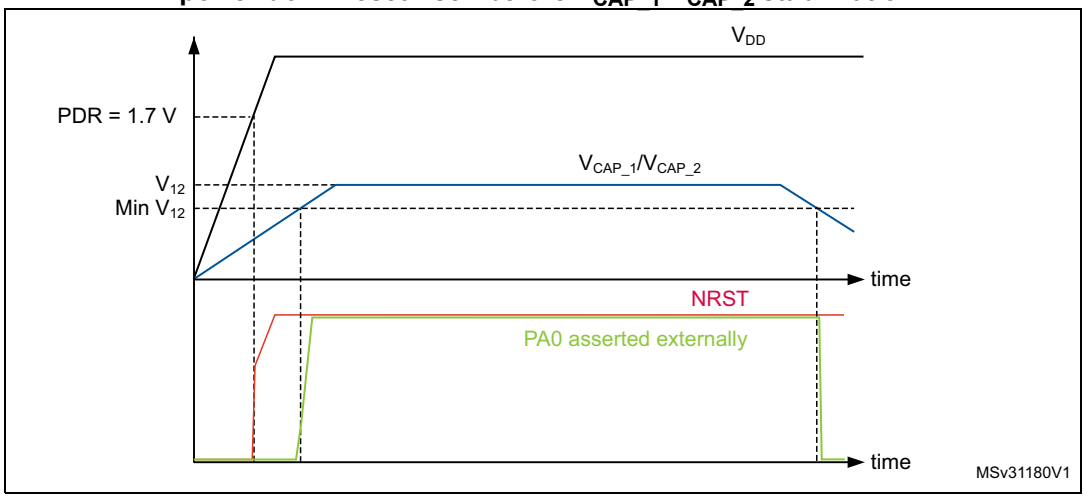
*Note: The minimum value of $V_{12}$ depends on the maximum frequency targeted in the application*

**Figure 7. Startup in regulator OFF: slow $V_{DD}$ slope - power-down reset risen after $V_{CAP\_1}/V_{CAP\_2}$ stabilization**




1. This figure is valid whatever the internal reset mode (ON or OFF).

**Figure 8. Startup in regulator OFF mode: fast $V_{DD}$ slope - power-down reset risen before $V_{CAP\_1}/V_{CAP\_2}$ stabilization**




1. This figure is valid whatever the internal reset mode (ON or OFF).

Table 6. USART feature comparison

| USART name | Standard features | Modem (RTS/CTS) | LIN | SPI master | irDA | Smartcard (ISO 7816) | Max. baud rate in Mbit/s (oversampling by 16) | Max. baud rate in Mbit/s (oversampling by 8) | APB mapping |
|---|---|---|---|---|---|---|---|---|---|
| USART1 | X | X | X | X | X | X | 6.25 | 12.5 | APB2 (max. 100 MHz) |
| USART2 | X | X | X | X | X | X | 3.12 | 6.25 | APB1 (max. 50 MHz) |
| USART6 | X | N.A | X | X | X | X | 6.25 | 12.5 | APB2 (max. 100 MHz) |

## 3.23 Serial peripheral interface (SPI)

The devices feature five SPIs in slave and master modes in full-duplex and simplex communication modes. SPI1, SPI4 and SPI5 can communicate at up to 50 Mbit/s, SPI2 and SPI3 can communicate at up to 25 Mbit/s. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC modes. All SPIs can be served by the DMA controller.

The SPI interface can be configured to operate in TI mode for communications in master mode and slave mode.

## 3.24 Inter-integrated sound ($I^2S$)

Five standard $I^2S$ interfaces (multiplexed with SPI1 to SPI5) are available.They can be operated in master or slave mode, in simplex communication modes and full duplex for I2S2 and I2S3 and can be configured to operate with a 16-/32-bit resolution as an input or output channel. All the I2Sx audio sampling frequencies from 8 kHz up to 192 kHz are supported. When either or both of the $I^2S$ interfaces is/are configured in master mode, the master clock can be output to the external DAC/CODEC at 256 times the sampling frequency.

All $I^2Sx$ can be served by the DMA controller.

## 3.25 Audio PLL (PLLI2S)

The devices feature an additional dedicated PLL for audio $I^2S$ application. It allows to achieve error-free $I^2S$ sampling clock accuracy without compromising on the CPU performance.

The PLLI2S configuration can be modified to manage an $I^2S$ sample rate change without disabling the main PLL (PLL) used for the CPU.

The audio PLL can be programmed with very low error to obtain sampling rates ranging from 8 kHz to 192 kHz.

In addition to the audio PLL, a master clock input pin can be used to synchronize the I2S flow with an external PLL (or Codec output).

## 3.26 Secure digital input/output interface (SDIO)

An SD/SDIO/MMC/eMMC host interface is available, that supports MultiMediaCard System Specification Version 4.2 in three different databus modes: 1-bit (default), 4-bit and 8-bit.

The interface allows data transfer at up to 50 MHz, and is compliant with the SD Memory Card Specification Version 2.0.

The SDIO Card Specification Version 2.0 is also supported with two different databus modes: 1-bit (default) and 4-bit.

The current version supports only one SD/SDIO/MMC4.2 card at any one time and a stack of MMC4.1 or previous.

In addition to SD/SDIO/MMC/eMMC, this interface is fully compliant with the CE-ATA digital protocol Rev1.1.

## 3.27 Universal serial bus on-the-go full-speed (OTG_FS)

The devices embed an USB OTG full-speed device/host/OTG peripheral with integrated transceivers. The USB OTG FS peripheral is compliant with the USB 2.0 specification and with the OTG 1.0 specification. It has software-configurable endpoint setting and supports suspend/resume. The USB OTG full-speed controller requires a dedicated 48 MHz clock that is generated by a PLL connected to the HSE oscillator. The major features are:

- Combined Rx and Tx FIFO size of 320 × 35 bits with dynamic FIFO sizing
- Supports the session request protocol (SRP) and host negotiation protocol (HNP)
- 4 bidirectional endpoints
- 8 host channels with periodic OUT support
- HNP/SNP/IP inside (no need for any external resistor)
- For OTG/Host modes, a power switch is needed in case bus-powered devices are connected

## 3.28 General-purpose input/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain, with or without pull-up or pull-down), as input (floating, with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high-current-capable and have speed selection to better manage internal noise, power consumption and electromagnetic emission.

The I/O configuration can be locked if needed by following a specific sequence in order to avoid spurious writing to the I/Os registers.

Fast I/O handling allowing maximum I/O toggling up to 100 MHz.

## 3.29 Analog-to-digital converter (ADC)

One 12-bit analog-to-digital converter is embedded and shares up to 16 external channels, performing conversions in the single-shot or scan mode. In scan mode, automatic conversion is performed on a selected group of analog inputs.

The ADC can be served by the DMA controller. An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

To synchronize A/D conversion and timers, the ADCs could be triggered by any of TIM1, TIM2, TIM3, TIM4 or TIM5 timer.

## 3.30 Temperature sensor

The temperature sensor has to generate a voltage that varies linearly with temperature. The conversion range is between 1.7 V and 3.6 V. The temperature sensor is internally connected to the ADC_IN18 input channel which is used to convert the sensor output voltage into a digital value. Refer to the reference manual for additional information.

As the offset of the temperature sensor varies from chip to chip due to process variation, the internal temperature sensor is mainly suitable for applications that detect temperature changes instead of absolute temperatures. If an accurate temperature reading is needed, then an external temperature sensor part should be used.

## 3.31 Serial wire JTAG debug port (SWJ-DP)

The ARM SWJ-DP interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

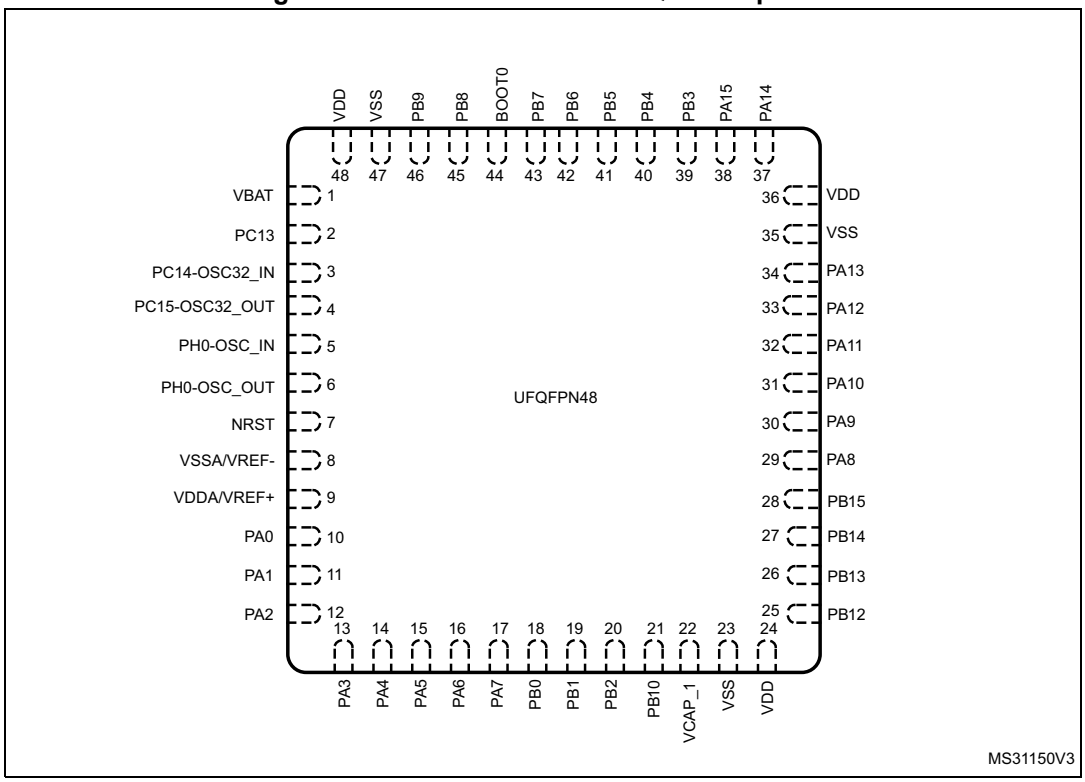
Debug is performed using 2 pins only instead of 5 required by the JTAG (JTAG pins could be re-use as GPIO with alternate function): the JTAG TMS and TCK pins are shared with SWDIO and SWCLK, respectively, and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

## 3.32 Embedded Trace Macrocell™

The ARM Embedded Trace Macrocell provides a greater visibility of the instruction and data flow inside the CPU core by streaming compressed data at a very high rate from the STM32F411xC/xE through a small number of ETM pins to an external hardware trace port analyzer (TPA) device. The TPA is connected to a host computer using any high-speed channel available. Real-time instruction and data flow activity can be recorded and then formatted for display on the host computer that runs the debugger software. TPA hardware is commercially available from common development tool vendors.

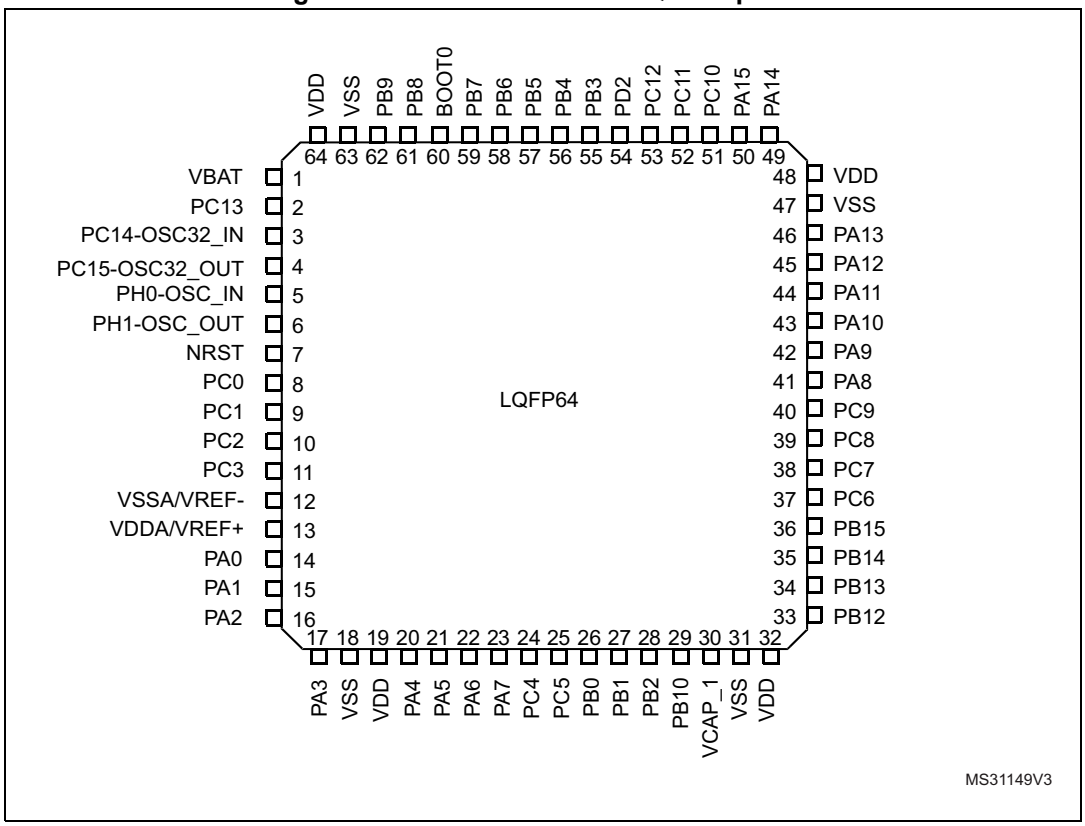
The Embedded Trace Macrocell operates with third party debugger software tools.

**Figure 10. STM32F411xC/xE UFQFPN48 pinout**




1. The above figure shows the package top view.

**Figure 11. STM32F411xC/xE LQFP64 pinout**




1. The above figure shows the package top view.

Table 8. STM32F411xC/xE pin definitions (continued)

| Pin number | | | | | Pin name (function after reset)[1] | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|
| UFQFPN48 | LQFP64 | WLCSP49 | LQFP100 | UFBGA100 | | | | | | |
| - | 24 | - | 33 | K5 | PC4 | I/O | FT | - | EVENTOUT | ADC1_14 |
| - | 25 | - | 34 | L5 | PC5 | I/O | FT | - | EVENTOUT | ADC1_15 |
| 18 | 26 | G5 | 35 | M5 | PB0 | I/O | FT | - | TIM1_CH2N, TIM3_CH3, SPI5_SCK/I2S5_CK, EVENTOUT | ADC1_8 |
| 19 | 27 | G4 | 36 | M6 | PB1 | I/O | FT | - | TIM1_CH3N, TIM3_CH4, SPI5_NSS/I2S5_WS, EVENTOUT | ADC1_9 |
| 20 | 28 | G3 | 37 | L6 | PB2 | I/O | FT | - | EVENTOUT | BOOT1 |
| - | - | - | 38 | M7 | PE7 | I/O | FT | - | TIM1_ETR, EVENTOUT | - |
| - | - | - | 39 | L7 | PE8 | I/O | FT | - | TIM1_CH1N, EVENTOUT | - |
| - | - | - | 40 | M8 | PE9 | I/O | FT | - | TIM1_CH1, EVENTOUT | - |
| - | - | - | 41 | L8 | PE10 | I/O | FT | - | TIM1_CH2N, EVENTOUT | - |
| - | - | - | 42 | M9 | PE11 | I/O | FT | - | TIM1_CH2, SPI4_NSS/I2S4_WS, SPI5_NSS/I2S5_WS, EVENTOUT | - |
| - | - | - | 43 | L9 | PE12 | I/O | FT | - | TIM1_CH3N, SPI4_SCK/I2S4_CK, SPI5_SCK/I2S5_CK, EVENTOUT | - |
| - | - | - | 44 | M10 | PE13 | I/O | FT | - | TIM1_CH3, SPI4_MISO, SPI5_MISO, EVENTOUT | - |
| - | - | - | 45 | M11 | PE14 | I/O | FT | - | TIM1_CH4, SPI4_MOSI/I2S4_SD, SPI5_MOSI/I2S5_SD, EVENTOUT | - |
| - | - | - | 46 | M12 | PE15 | I/O | FT | - | TIM1_BKIN, EVENTOUT | - |

**Table 19. Embedded reset and power control block characteristics (continued)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{RUSH}$(2) | In-Rush current on voltage regulator power-on (POR or wakeup from Standby) | - | - | 160 | 200 | mA |
| $E_{RUSH}$(2) | In-Rush energy on voltage regulator power-on (POR or wakeup from Standby) | $V_{DD}$ = 1.7 V, $T_A$ = 125 °C, $I_{RUSH}$ = 171 mA for 31 µs | - | - | 5.4 | µC |

1. The product behavior is guaranteed by design down to the minimum $V_{POR/PDR}$ value.
2. Guaranteed by design.
3. The reset timing is measured from the power-on (POR reset or wakeup from $V_{BAT}$) to the instant when first instruction is fetched by the user application code.

## 6.3.6 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.
The current consumption is measured as described in *Figure 18: Current consumption measurement scheme*.

All the run-mode current consumption measurements given in this section are performed with a reduced code that gives a consumption equivalent to CoreMark code.

### Typical and maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in input mode with a static value at VDD or VSS (no load).
- All peripherals are disabled except if it is explicitly mentioned.
- The Flash memory access time is adjusted to both $f_{HCLK}$ frequency and VDD ranges (refer to *Table 15: Features depending on the operating power supply range*).
- The voltage scaling is adjusted to $f_{HCLK}$ frequency as follows:
  - Scale 3 for $f_{HCLK} \leq 64$ MHz
  - Scale 2 for 64 MHz < $f_{HCLK} \leq 84$ MHz
  - Scale 1 for 84 MHz < $f_{HCLK} \leq 100$ MHz
- The system clock is HCLK, $f_{PCLK1} = f_{HCLK}/2$, and $f_{PCLK2} = f_{HCLK}$.
- External clock is 4 MHz and PLL is ON except if it is explicitly mentioned.
- The maximum values are obtained for $V_{DD}$ = 3.6 V and a maximum ambient temperature ($T_A$), and the typical values for $T_A$= 25 °C and $V_{DD}$ = 3.3 V unless otherwise specified.

**Table 21. Typical and maximum current consumption, code with data processing (ART accelerator disabled) running from SRAM - $V_{DD}$ = 3.6 V**

| Symbol | Parameter | Conditions | $f_{HCLK}$ (MHz) | Typ | Max(1) | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | $T_A$= 25 °C | $T_A$= 85 °C | $T_A$= 105 °C | $T_A$= 125 °C | |
| $I_{DD}$ | Supply current in **Run mode** | External clock, PLL ON(2), all peripherals enabled(3)(4) | 100 | 21.7 | 23.3 | 23.9 | 24.3 | 25.3 | mA |
| | | | 84 | 17.5 | 19.2(5) | 19.4 | 19.5 | 20.5 | |
| | | | 64 | 12.2 | 13.2 | 13.5 | 14.0 | 14.9 | |
| | | | 50 | 9.6 | 10.4 | 10.7 | 11.2 | 12.1 | |
| | | | 20 | 4.5 | 5.0 | 5.3 | 5.9 | 6.8 | |
| | | HSI, PLL OFF, all peripherals enabled(3) | 16 | 3.0 | 3.3 | 3.6 | 4.3 | 5.2 | |
| | | | 1 | 0.5 | 0.7 | 1.0 | 1.7 | 2.6 | |
| | | External clock, PLL OFF(2), all peripherals disabled(3) | 100 | 13.0 | 14.6(5) | 14.6 | 14.9 | 16.0 | |
| | | | 84 | 10.5 | 11.9(5) | 12.1 | 12.2 | 13.2 | |
| | | | 64 | 7.4 | 8.4(5) | 8.8 | 8.9 | 9.9 | |
| | | | 50 | 5.9 | 6.6 | 6.8 | 7.3 | 8.2 | |
| | | | 20 | 2.8 | 3.3 | 3.5 | 4.2 | 5.1 | |
| | | HSI, PLL OFF, all peripherals disabled(3) | 16 | 1.9 | 2.1 | 2.4 | 3.1 | 4.0 | |
| | | | 1 | 0.4 | 0.5 | 0.9 | 1.6 | 2.5 | |

1. Guaranteed by characterization results.
2. Refer to *Table 41* and RM0383 for the possible PLL VCO setting
3. When analog peripheral blocks such as ADC, HSE, LSE, HSI, or LSI are ON, an additional power consumption has to be considered.
4. When the ADC is ON (ADON bit set in the ADC_CR2 register), add an additional power consumption of 1.6 mA for the analog part.
5. Guaranteed by test in production.

**Table 28. Typical and maximum current consumption in Stop mode - $V_{DD}$=3.6 V**

| Symbol | Conditions | Parameter | Typ | Max(1) | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | $T_A$ = 25 °C | $T_A$ = 25 °C | $T_A$ = 85 °C | $T_A$ = 105 °C | $T_A$ = 125 °C | |
| $I_{DD\_STOP}$ | Flash in Stop mode, all oscillators OFF, no independent watchdog | Main regulator usage | 113.7 | 145(2) | 410 | 720(2) | 1217 | µA |
| | | Low power regulator usage | 43.1 | 68(2) | 310 | 600(2) | 1073 | |
| | Flash in Deep power down mode, all oscillators OFF, no independent watchdog | Main regulator usage | 76.2 | 105(2) | 320 | 600(2) | 1019 | |
| | | Low power regulator usage | 14 | 38(2) | 275 | 560(2) | 1025 | |
| | | Low power low voltage regulator usage | 10 | 30(2) | 235 | 510(2) | 928 | |

1. Guaranteed by characterization results.
2. Guaranteed by test in production.

**Table 29. Typical and maximum current consumption in Standby mode - $V_{DD}$= 1.7 V**

| Symbol | Parameter | Conditions | Typ(1) | Max(2) | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | $T_A$ = 25 °C | $T_A$ = 25 °C | $T_A$ = 85 °C | $T_A$ = 105 °C | $T_A$ = 125 °C | |
| $I_{DD\_STBY}$ | Supply current in Standby mode | Low-speed oscillator (LSE) and RTC ON | 2.4 | 4 | 12 | 25 | 50 | µA |
| | | RTC and LSE OFF | 1.8 | 3(3) | 11 | 24(3) | 49 | |

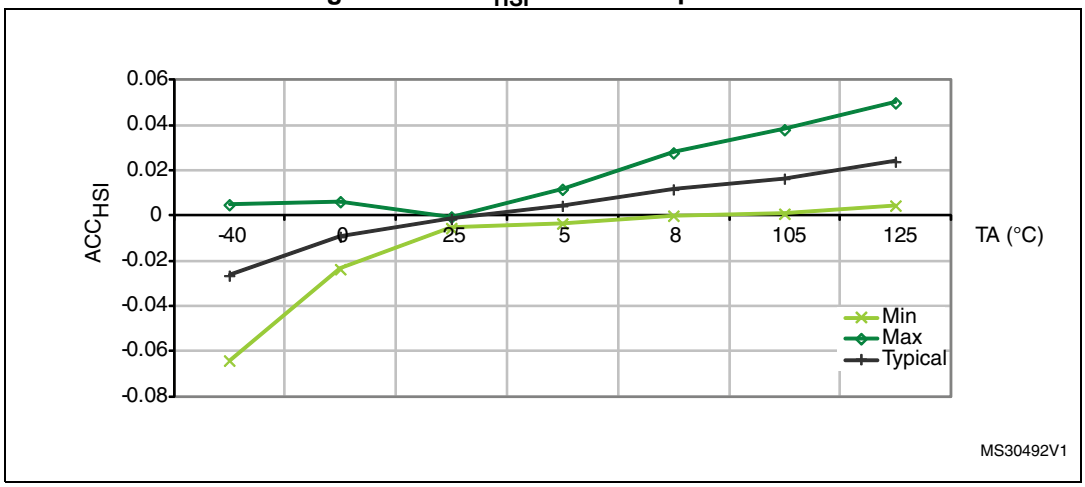
1. When the PDR is OFF (internal reset is OFF), the typical current consumption is reduced by 1.2 µA.
2. Guaranteed by characterization results.
3. Guaranteed by test in production.

**Table 30. Typical and maximum current consumption in Standby mode - $V_{DD}$= 3.6 V**

| Symbol | Parameter | Conditions | Typ(1) | Max(2) | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | $T_A$ = 25 °C | $T_A$ = 25 °C | $T_A$ = 85 °C | $T_A$ = 105 °C | $T_A$ = 125 °C | |
| $I_{DD\_STBY}$ | Supply current in Standby mode | Low-speed oscillator (LSE) and RTC ON | 2.8 | 5 | 14 | 29 | 59 | µA |
| | | RTC and LSE OFF | 2.1 | 4(3) | 13.5 | 28(3) | 58 | |

1. When the PDR is OFF (internal reset is OFF), the typical current consumption is reduced by 1.2 µA.
2. Guaranteed by characterization results.
3. Guaranteed by test in production.

Figure 26. $ACC_{HSI}$ versus temperature




1. Guaranteed by characterization results.

## Low-speed internal (LSI) RC oscillator

Table 40. LSI oscillator characteristics (1)

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $f_{LSI}$(2) | Frequency | 17 | 32 | 47 | kHz |
| $t_{su(LSI)}$(3) | LSI oscillator startup time | - | 15 | 40 | µs |
| $I_{DD(LSI)}$(3) | LSI oscillator power consumption | - | 0.4 | 0.6 | µA |

1. $V_{DD}$ = 3 V, $T_A$ = –40 to 125 °C unless otherwise specified.
2. Guaranteed by characterization results.
3. Guaranteed by design.

### SPI interface characteristics

Unless otherwise specified, the parameters given in *Table 60* for the SPI interface are derived from tests performed under the ambient temperature, $f_{PCLKx}$ frequency and $V_{DD}$ supply voltage conditions summarized in *Table 14*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$

Refer to *Section 6.3.16: I/O port characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI).

**Table 60. SPI dynamic characteristics(1)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{SCK}$<br>$1/t_{c(SCK)}$ | SPI clock frequency | Master full duplex/receiver mode,<br>2.7 V < $V_{DD}$ < 3.6 V<br>SPI1/4/5 | - | - | 42 | MHz |
| | | Master full duplex/receiver mode,<br>3.0 V < $V_{DD}$ < 3.6 V<br>SPI1/4/5 | - | - | 50 | |
| | | Master transmitter mode<br>1.7 V < $V_{DD}$ < 3.6 V<br>SPI1/4/5 | - | - | 50 | |
| | | Master mode<br>1.7 V < $V_{DD}$ < 3.6 V<br>SPI1/2/3/4/5 | - | - | 25 | |
| | | Slave transmitter/full duplex mode<br>2.7 V < $V_{DD}$ < 3.6 V<br>SPI1/4/5 | - | - | 38(2) | |
| | | Slave receiver mode,<br>1.8 V < $V_{DD}$ < 3.6 V<br>SPI1/4/5 | - | - | 50 | |
| | | Slave mode,<br>1.8 V < $V_{DD}$ < 3.6 V<br>SPI1/2/3/4/5 | - | - | 25 | |
| Duty(SCK) | Duty cycle of SPI clock frequency | Slave mode | 30 | 50 | 70 | % |
| $t_{w(SCKH)}$<br>$t_{w(SCKL)}$ | SCK high and low time | Master mode, SPI presc = 2 | $T_{PCLK}$-1.5 | $T_{PCLK}$ | $T_{PCLK}$ +1.5 | ns |
| $t_{su(NSS)}$ | NSS setup time | Slave mode, SPI presc = 2 | $3T_{PCLK}$ | - | - | ns |
| $t_{h(NSS)}$ | NSS hold time | Slave mode, SPI presc = 2 | $2T_{PCLK}$ | - | - | ns |
| $t_{su(MI)}$ | Data input setup time | Master mode | 4 | - | - | ns |
| $t_{su(SI)}$ | | Slave mode | 2.5 | - | - | ns |
| $t_{h(MI)}$ | Data input hold time | Master mode | 7.5 | - | - | ns |
| $t_{h(SI)}$ | | Slave mode | 3.5 | - | - | ns |

### I²S interface characteristics

Unless otherwise specified, the parameters given in *Table 61* for the I²S interface are derived from tests performed under the ambient temperature, $f_{PCLKx}$ frequency and $V_{DD}$ supply voltage conditions summarized in *Table 14*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$

Refer to *Section 6.3.16: I/O port characteristics* for more details on the input/output alternate function characteristics (CK, SD, WS).

**Table 61. I²S dynamic characteristics(1)**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $f_{MCK}$ | I2S Main clock output | - | 256x8K | 256xFs(2) | MHz |
| $f_{CK}$ | I2S clock frequency | Master data: 32 bits | - | 64xFs | MHz |
| | | Slave data: 32 bits | - | 64xFs | |
| $D_{CK}$ | I2S clock frequency duty cycle | Slave receiver | 30 | 70 | % |
| $t_{v(WS)}$ | WS valid time | Master mode | 0 | 7 | ns |
| $t_{h(WS)}$ | WS hold time | Master mode | 1.5 | - | |
| $t_{su(WS)}$ | WS setup time | Slave mode | 1.5 | - | |
| $t_{h(WS)}$ | WS hold time | Slave mode | 3 | - | |
| $t_{su(SD\_MR)}$ | Data input setup time | Master receiver | 1 | - | |
| $t_{su(SD\_SR)}$ | | Slave receiver | 2.5 | - | |
| $t_{h(SD\_MR)}$ | Data input hold time | Master receiver | 7 | - | |
| $t_{h(SD\_SR)}$ | | Slave receiver | 2.5 | - | |
| $t_{v(SD\_ST)}$ | Data output valid time | Slave transmitter (after enable edge) | - | 20 | |
| $t_{v(SD\_MT)}$ | | Master transmitter (after enable edge) | - | 6 | |
| $t_{h(SD\_ST)}$ | Data output hold time | Slave transmitter (after enable edge) | 8 | - | |
| $t_{h(SD\_MT)}$ | | Master transmitter (after enable edge) | 2 | - | |

1. Guaranteed by characterization results.
2. The maximum value of 256xFs is 50 MHz (APB1 maximum frequency).

*Note: Refer to the I2S section of RM0383 reference manual for more details on the sampling frequency ($F_S$).*

*$f_{MCK}$, $f_{CK}$, and $D_{CK}$ values reflect only the digital peripheral behavior. The values of these parameters might be slightly impacted by the source clock precision. $D_{CK}$ depends mainly on the value of ODD bit. The digital contribution leads to a minimum value of (I2SDIV/(2*I2SDIV+ODD) and a maximum value of (I2SDIV+ODD)/(2*I2SDIV+ODD). $F_S$ maximum value is supported for each mode/condition.*

**Table 65. ADC characteristics (continued)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{lat}$(2) | Injection trigger conversion latency | $f_{ADC}$ = 30 MHz | - | - | 0.100 | µs |
| | | | - | - | 3(5) | $1/f_{ADC}$ |
| $t_{latr}$(2) | Regular trigger conversion latency | $f_{ADC}$ = 30 MHz | - | - | 0.067 | µs |
| | | | - | - | 2(5) | $1/f_{ADC}$ |
| $t_S$(2) | Sampling time | $f_{ADC}$ = 30 MHz | 0.100 | - | 16 | µs |
| | | | 3 | - | 480 | $1/f_{ADC}$ |
| $t_{STAB}$(2) | Power-up time | | - | 2 | 3 | µs |
| $t_{CONV}$(2) | Total conversion time (including sampling time) | $f_{ADC}$ = 30 MHz 12-bit resolution | 0.50 | - | 16.40 | µs |
| | | $f_{ADC}$ = 30 MHz 10-bit resolution | 0.43 | - | 16.34 | µs |
| | | $f_{ADC}$ = 30 MHz 8-bit resolution | 0.37 | - | 16.27 | µs |
| | | $f_{ADC}$ = 30 MHz 6-bit resolution | 0.30 | - | 16.20 | µs |
| | | 9 to 492 ($t_S$ for sampling +n-bit resolution for successive approximation) | | | | $1/f_{ADC}$ |
| $f_S$(2) | Sampling rate ($f_{ADC}$ = 30 MHz, and $t_S$ = 3 ADC cycles) | 12-bit resolution Single ADC | - | - | 2 | Msps |
| | | 12-bit resolution Interleave Dual ADC mode | - | - | 3.75 | Msps |
| | | 12-bit resolution Interleave Triple ADC mode | - | - | 6 | Msps |
| $I_{VREF+}$(2) | ADC $V_{REF}$ DC current consumption in conversion mode | | - | 300 | 500 | µA |
| $I_{VDDA}$(2) | ADC $V_{DDA}$ DC current consumption in conversion mode | | - | 1.6 | 1.8 | mA |

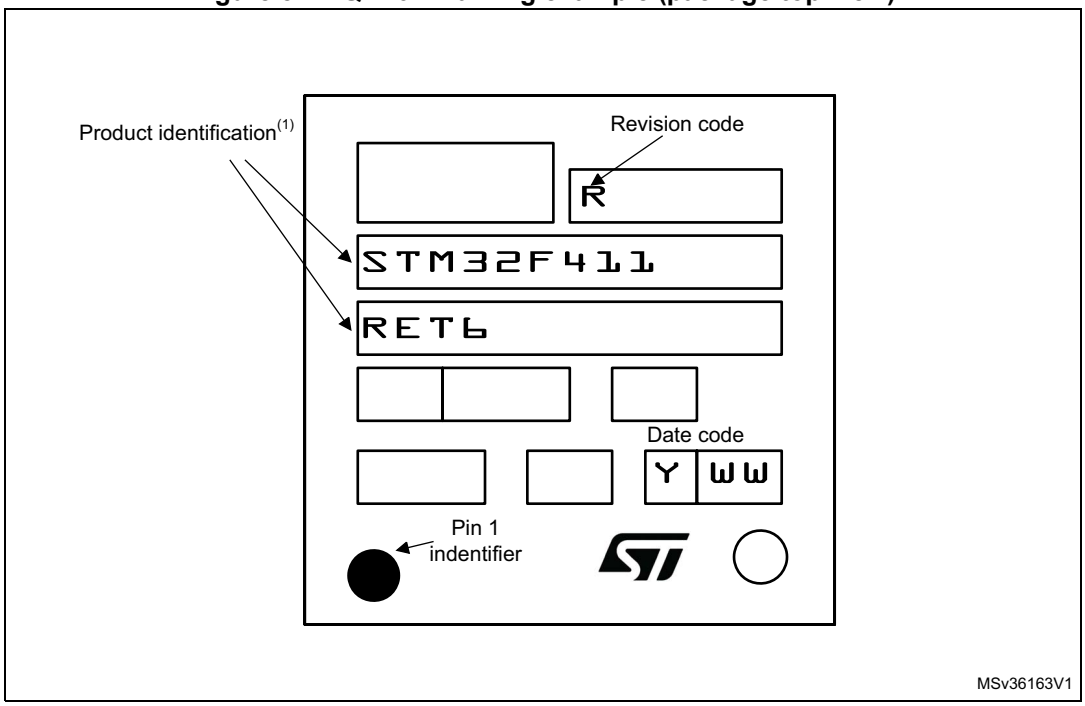
1. $V_{DDA}$ minimum value of 1.7 V is possible with the use of an external power supply supervisor (refer to *Section 3.15.2: Internal reset OFF*).
2. Guaranteed by characterization results.
3. $V_{REF+}$ is internally connected to $V_{DDA}$ and $V_{REF-}$ is internally connected to $V_{SSA}$.
4. $R_{ADC}$ maximum value is given for $V_{DD}$=1.7 V, and minimum value for $V_{DD}$=3.3 V.
5. For external triggers, a delay of $1/f_{PCLK2}$ must be added to the latency specified in *Table 65*.

### Device marking for LQFP64

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which depend on supply chain operations, are not indicated below.

**Figure 54. LQFP64 marking example (package top view)**



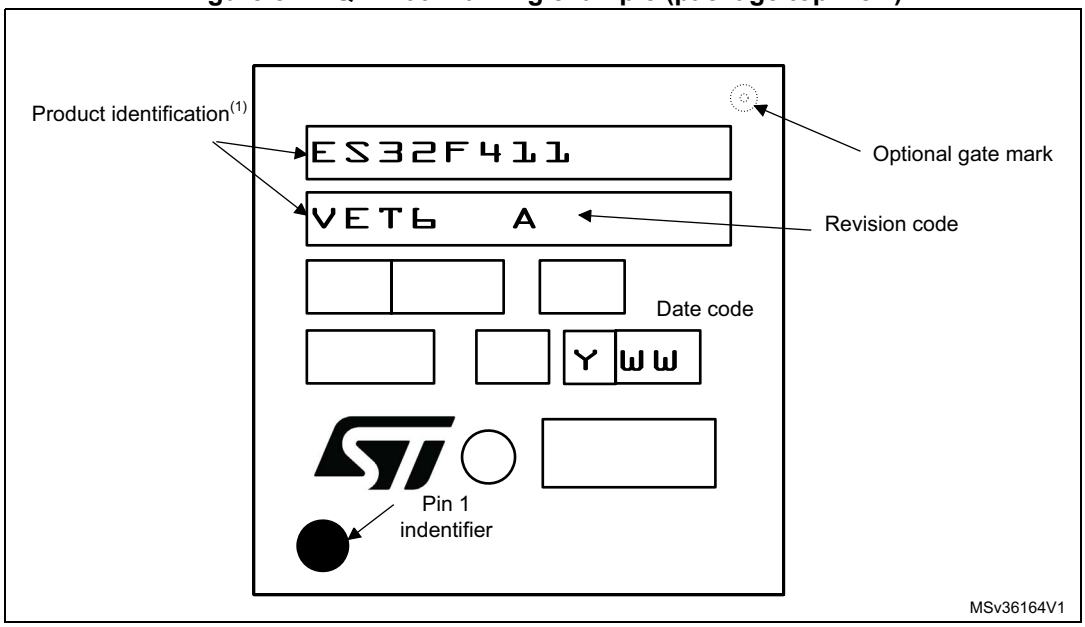

1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

### Device marking for LQFP100

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which depend on supply chain operations, are not indicated below.

**Figure 57. LQPF100 marking example (package top view)**

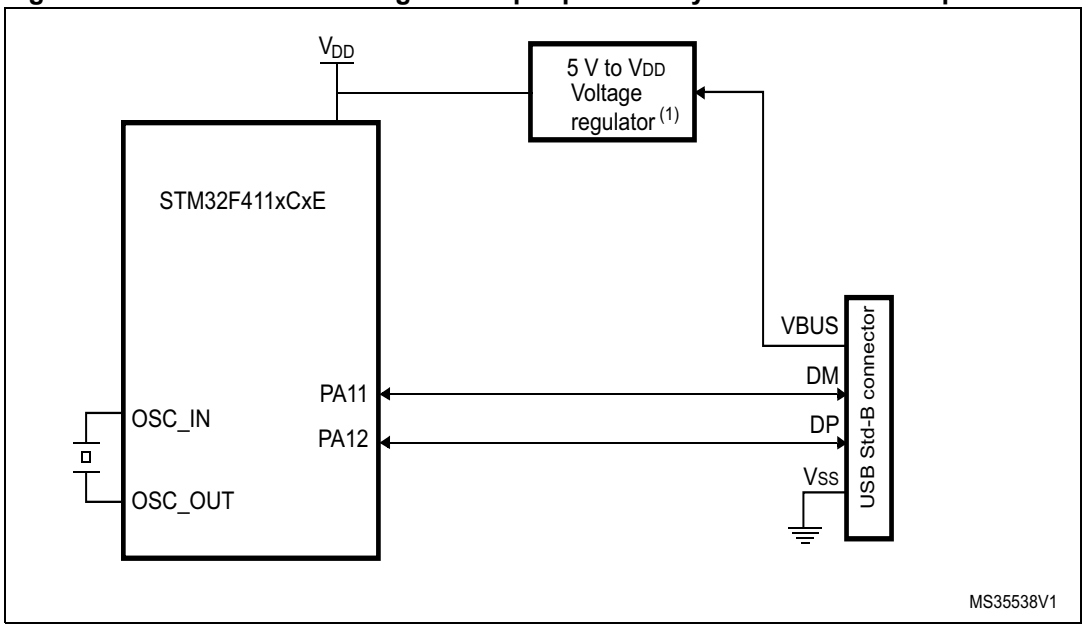



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

# Appendix B Application block diagrams

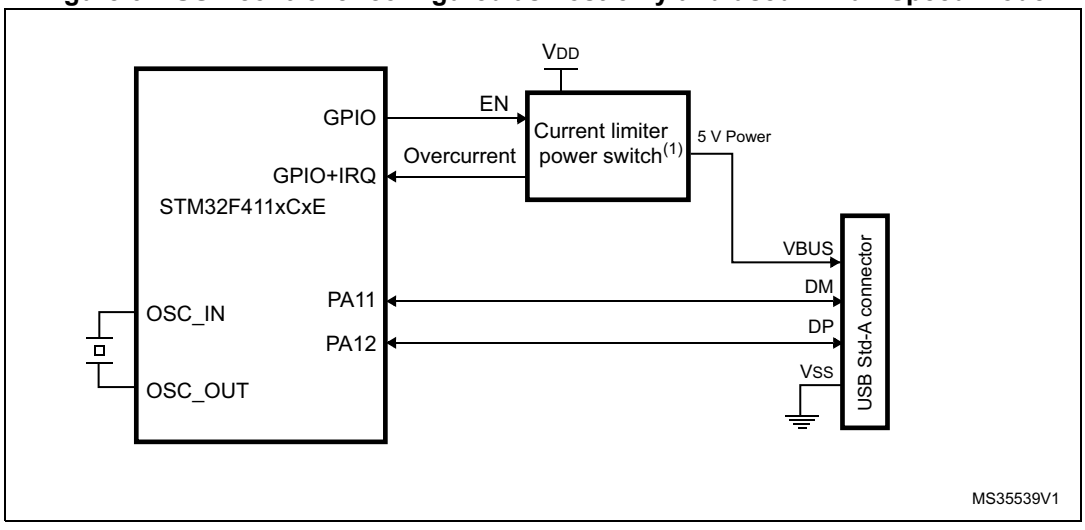
## B.1 USB OTG Full Speed (FS) interface solutions

**Figure 61. USB controller configured as peripheral-only and used in Full-Speed mode**




1. The external voltage regulator is only needed when building a $V_{BUS}$ powered device.

**Figure 62. USB controller configured as host-only and used in Full-Speed mode**




1. The current limiter is required only if the application has to support a $V_{BUS}$ powered device. A basic power switch can be used if 5V are available on the application board.