Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	18MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LED, POR, PWM, WDT
Number of I/O	26
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 3.6V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	28-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/p89lpc9311fdh-129

4. Block diagram

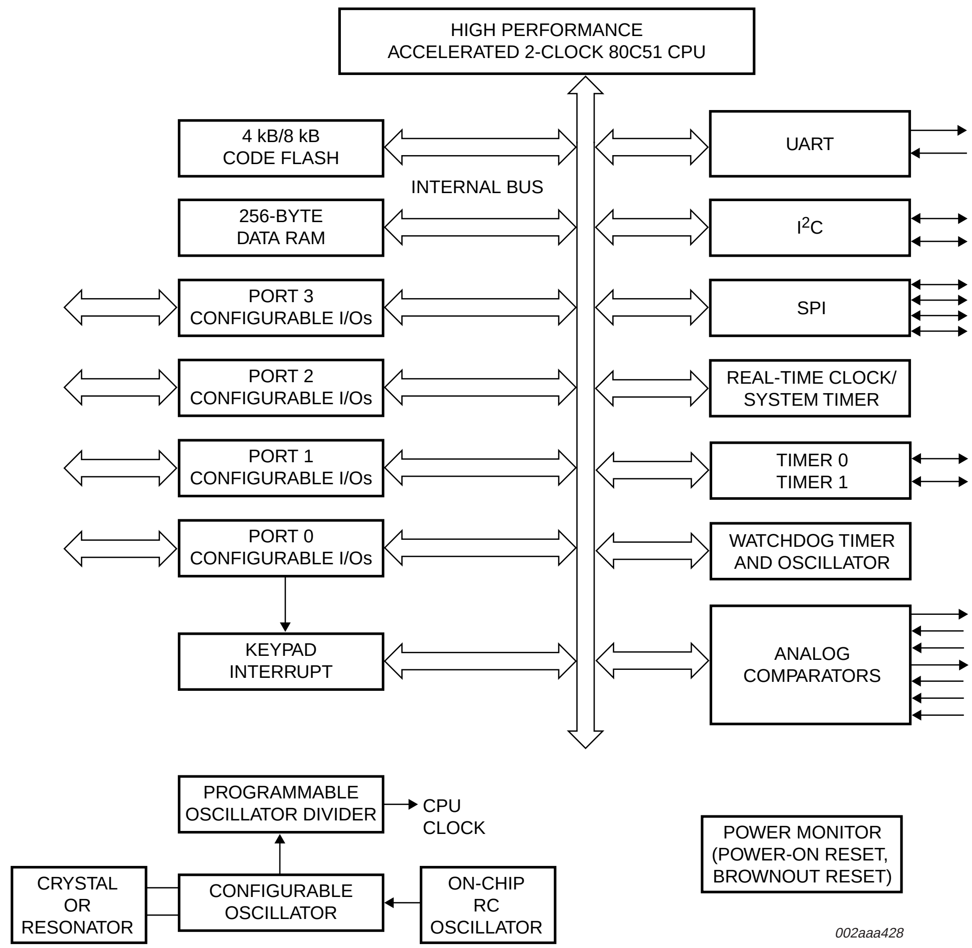


Fig 1. Block diagram.

5.2 Pin description

Table 3: Pin description

Symbol	Pin	Type	Description
P0.0 - P0.7	3, 26, 25, 24, 23, 22, 20, 19	I/O	**Port 0:** Port 0 is an 8-bit I/O port with a user-configurable output type. During reset Port 0 latches are configured in the input only mode with the internal pull-up disabled. The operation of Port 0 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to Section 8.11.1 “Port configurations” and Table 7 “DC electrical characteristics” for details. The Keypad Interrupt feature operates with Port 0 pins. All pins have Schmitt triggered inputs. Port 0 also provides various special functions as described below:
	3	I/O	**P0.0** — Port 0 bit 0.
		O	**CMP2** — Comparator 2 output.
		I	**KBI0** — Keyboard input 0.
	26	I/O	**P0.1** — Port 0 bit 1.
		I	**CIN2B** — Comparator 2 positive input B.
		I	**KBI1** — Keyboard input 1.
	25	I/O	**P0.2** — Port 0 bit 2.
		I	**CIN2A** — Comparator 2 positive input A.
		I	**KBI2** — Keyboard input 2.
	24	I/O	**P0.3** — Port 0 bit 3.
		I	**CIN1B** — Comparator 1 positive input B.
		I	**KBI3** — Keyboard input 3.
	23	I/O	**P0.4** — Port 0 bit 4.
		I	**CIN1A** — Comparator 1 positive input A.
		I	**KBI4** — Keyboard input 4.
	22	I/O	**P0.5** — Port 0 bit 5.
		I	**CMPREF** — Comparator reference (negative) input.
		I	**KBI5** — Keyboard input 5.
	20	I/O	**P0.6** — Port 0 bit 6.
		O	**CMP1** — Comparator 1 output.
		I	**KBI6** — Keyboard input 6.
	19	I/O	**P0.7** — Port 0 bit 7.
		I/O	**T1** — Timer/counter 1 external count input or overflow output.
		I	**KBI7** — Keyboard input 7.

Table 3: Pin description...*continued*

Symbol	Pin	Type	Description
P2.0 - P2.7	1, 2, 13, 14, 15, 16, 27, 28	I/O	**Port 2:** Port 2 is a 8-bit I/O port with a user-configurable output type. During reset Port 2 latches are configured in the input only mode with the internal pull-up disabled. The operation of port 2 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to the section on I/O port configuration and the DC Electrical Characteristics for details. This port is not available in 20-pin package and is configured automatically as outputs to conserve power. The alternate functions for these pins must not be enabled. All pins have Schmitt triggered inputs. Port 2 also provides various special functions as described below.
	1	I/O	**P2.0** — Port 2 bit 0.
	2	I/O	**P2.1** — Port 2 bit 1.
	13	I/O	**P2.2** — Port 2 bit 2.
		I/O	**MOSI** — SPI master out slave in. When configured as master, this pin is output, when configured as slave, this pin is input.
	14	I/O	**P2.3** — Port 2 bit 3.
		I/O	**MISO** — SPI master in slave out. When configured as master, this pin is input, when configured as slave, this pin is output.
	15	I/O	**P2.4** — Port 2 bit 4.
		I	$\overline{\textbf{SS}}$ — SPI Slave select.
	16	I/O	**P2.5** — Port 2 bit 5.
		I/O	**SPICLK** — SPI clock. When configured as master, this pin is output, when configured as slave, this pin is input.
	27	I/O	**P2.6** — Port 2 bit 6.
	28	I/O	**P2.7** — Port 2 bit 7.

Table 4: Special function registers

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
		Bit address	E7	E6	E5	E4	E3	E2	E1	E0		
ACC*	Accumulator	E0H									00	00000000
AUXR1	Auxiliary function register	A2H	CLKLP	EBRR	ENT1	ENT0	SRST	0	-	DPS	00[1]	000000x0
		Bit address	F7	F6	F5	F4	F3	F2	F1	F0		
B*	B register	F0H									00	00000000
BRGR0[2]	Baud rate generator rate LOW	BEH									00	00000000
BRGR1[2]	Baud rate generator rate HIGH	BFH									00	00000000
BRGCON	Baud rate generator control	BDH	-	-	-	-	-	-	SBRGS	BRGEN	00[6]	xxxxxx00
CMP1	Comparator 1 control register	ACH	-	-	CE1	CP1	CN1	OE1	CO1	CMF1	00[1]	xx000000
CMP2	Comparator 2 control register	ADH	-	-	CE2	CP2	CN2	OE2	CO2	CMF2	00[1]	xx000000
DIVM	CPU clock divide-by-M control	95H									00	00000000
DPTR	Data pointer (2 bytes)											
DPH	Data pointer HIGH	83H									00	00000000
DPL	Data pointer LOW	82H									00	00000000
FMADRH	Program Flash address HIGH	E7H	-	-	-	-	-	-			00	00000000
FMADRL	Program Flash address LOW	E6H									00	00000000
FMCON	Program Flash Control (Read)	E4H	BUSY	-	-	-	HVA	HVE	SV	OI	70	01110000
	Program Flash Control (Write)		FMCMD.7	FMCMD.6	FMCMD.5	FMCMD.4	FMCMD.3	FMCMD.2	FMCMD.1	FMCMD.0		
FMDATA	Program Flash data	E5H									00	00000000
I2ADR	I2C slave address register	DBH	I2ADR.6	I2ADR.5	I2ADR.4	I2ADR.3	I2ADR.2	I2ADR.1	I2ADR.0	GC	00	00000000
		Bit address	DF	DE	DD	DC	DB	DA	D9	D8		
I2CON*	I2C control register	D8H	-	I2EN	STA	STO	SI	AA	-	CRSEL	00	x00000x0
I2DAT	I2C data register	DAH										

8. Functional description

Remark: Please refer to the *P89LPC930/931 User's Manual* for a more detailed functional description.

8.1 Enhanced CPU

The P89LPC930/931 uses an enhanced 80C51 CPU which runs at 6 times the speed of standard 80C51 devices. A machine cycle consists of two CPU clock cycles, and most instructions execute in one or two machine cycles.

8.2 Clocks

8.2.1 Clock definitions

The P89LPC930/931 device has several internal clocks as defined below:

OSCCLK — Input to the DIVM clock divider. OSCCLK is selected from one of four clock sources (see Figure 4) and can also be optionally divided to a slower frequency (see Section 8.7 "CPU CLOCK (CCLK) modification: DIVM register").

Note: f_{osc} is defined as the OSCCLK frequency.

CCLK — CPU clock; output of the clock divider. There are two CCLK cycles per machine cycle, and most instructions are executed in one to two machine cycles (two or four CCLK cycles).

RCCLK — The internal 7.373 MHz RC oscillator output.

PCLK — Clock for the various peripheral devices and is CCLK/2

8.2.2 CPU clock (OSCCLK)

The P89LPC930/931 provides several user-selectable oscillator options in generating the CPU clock. This allows optimization for a range of needs from high precision to lowest possible cost. These options are configured when the FLASH is programmed and include an on-chip Watchdog oscillator, an on-chip RC oscillator, an oscillator using an external crystal, or an external clock source. The crystal oscillator can be optimized for low, medium, or high frequency crystals covering a range from 20 kHz to 12 MHz.

8.2.3 Low speed oscillator option

This option supports an external crystal in the range of 20 kHz to 100 kHz. Ceramic resonators are also supported in this configuration.

8.2.4 Medium speed oscillator option

This option supports an external crystal in the range of 100 kHz to 4 MHz. Ceramic resonators are also supported in this configuration.

8.2.5 High speed oscillator option

This option supports an external crystal in the range of 4 MHz to 18 MHz. Ceramic resonators are also supported in this configuration. **When using an oscillator frequency above 12 MHz, the reset input function of P1.5 must be enabled. An external circuit is required to hold the device in reset at power-up until V_{DD} has reached its specified level. When system power is removed V_{DD} will fall below**

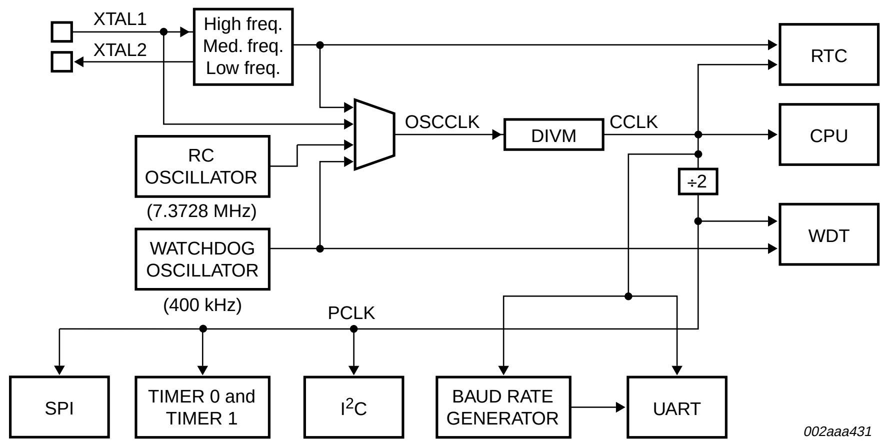


Fig 4. Block diagram of oscillator control.

8.6 CPU CLock (CCLK) wake-up delay

The P89LPC930/931 has an internal wake-up timer that delays the clock until it stabilizes depending to the clock source used. If the clock source is any of the three crystal selections (low, medium and high frequencies) the delay is 992 OSCCLK cycles plus 60 to 100 µs. If the clock source is either the internal RC oscillator, Watchdog oscillator, or external clock, the delay is 224 OSCCLK cycles plus 60 to 100 µs.

8.7 CPU CLOCK (CCLK) modification: DIVM register

The OSCCLK frequency can be divided down up to 256 times by configuring a dividing register, DIVM, to generate CCLK. This feature makes it possible to temporarily run the CPU at a lower rate, reducing power consumption. By dividing the clock, the CPU can retain the ability to respond to events that would not exit Idle mode by executing its normal program at a lower rate. This can also allow bypassing the oscillator start-up time in cases where Power-down mode would otherwise be used. The value of DIVM may be changed by the program at any time without interrupting code execution.

8.8 Low power select

The P89LPC930/931 is designed to run at 18 MHz (CCLK) maximum. However, if CCLK is 8 MHz or slower, the CLKLP SFR bit (AUXR1.7) can be set to ‘1’ to lower the power consumption further. On any reset, CLKLP is ‘0’ allowing highest performance access. This bit can then be set in software if CCLK is running at 8 MHz or slower.

8.9 Memory organization

The various P89LPC930/931 memory spaces are as follows:

- DATA

  128 bytes of internal data memory space (00h:7Fh) accessed via direct or indirect addressing, using instruction other than MOVX and MOVC. All or part of the Stack may be in this area.

- IDATA

  Indirect Data. 256 bytes of internal data memory space (00h:FFh) accessed via indirect addressing using instructions other than MOVX and MOVC. All or part of the Stack may be in this area. This area includes the DATA area and the 128 bytes immediately above it.

- SFR

  Special Function Registers. Selected CPU registers and peripheral control and status registers, accessible only via direct addressing.

- CODE

  64 kB of Code memory space, accessed as part of program execution and via the MOVC instruction. The P89LPC930/931 has 4 kB/ 8 kB of on-chip Code memory.

8.10 Interrupts

The P89LPC930/931 uses a four priority level interrupt structure. This allows great flexibility in controlling the handling of the many interrupt sources. The P89LPC930/931 supports 13 interrupt sources: external interrupts 0 and 1, timers 0 and 1, serial port Tx, serial port Rx, combined serial port Rx/Tx, brownout detect, watchdog/real-time clock, I^2C, keyboard, and comparators 1 and 2, and SPI.

Each interrupt source can be individually enabled or disabled by setting or clearing a bit in the interrupt enable registers IEN0 or IEN1. The IEN0 register also contains a global disable bit, EA, which disables all interrupts.

Each interrupt source can be individually programmed to one of four priority levels by setting or clearing bits in the interrupt priority registers IP0, IP0H, IP1, and IP1H. An interrupt service routine in progress can be interrupted by a higher priority interrupt, but not by another interrupt of the same or lower priority. The highest priority interrupt service cannot be interrupted by any other interrupt source. If two requests of different priority levels are pending at the start of an instruction, the request of higher priority level is serviced.

If requests of the same priority level are pending at the start of an instruction, an internal polling sequence determines which request is serviced. This is called the arbitration ranking. Note that the arbitration ranking is only used to resolve pending requests of the same priority level.

8.10.1 External interrupt inputs

The P89LPC930/931 has two external interrupt inputs as well as the Keypad Interrupt function. The two interrupt inputs are identical to those present on the standard 80C51 microcontrollers.

These external interrupts can be programmed to be level-triggered or edge-triggered by setting or clearing bit IT1 or IT0 in Register TCON.

In edge-triggered mode if successive samples of the $\overline{\text{INTn}}$ pin show a HIGH in one cycle and a LOW in the next cycle, the interrupt request flag IEn in TCON is set, causing an interrupt request.

If an external interrupt is enabled when the P89LPC930/931 is put into Power-down or Idle mode, the interrupt will cause the processor to wake-up and resume operation. Refer to Section 8.13 “Power reduction modes” for details.

8.11.1 Port configurations

All but three I/O port pins on the P89LPC930/931 may be configured by software to one of four types on a bit-by-bit basis. These are: quasi-bidirectional (standard 80C51 port outputs), push-pull, open drain, and input-only. Two configuration registers for each port select the output type for each port pin.

P1.5 ($\overline{RST}$) can only be an input and cannot be configured.

P1.2 (SCL/T0) and P1.3 (SDA/$\overline{INT0}$) may only be configured to be either input-only or open-drain.

8.11.2 Quasi-bidirectional output configuration

Quasi-bidirectional outputs can be used as both an input and output without the need to reconfigure the port. This is possible because when the port outputs a logic HIGH, it is weakly driven, allowing an external device to pull the pin LOW. When the pin is driven LOW, it is driven strongly and able to sink a fairly large current. These features are somewhat similar to an open-drain output except that there are three pull-up transistors in the quasi-bidirectional output that serve different purposes.

The P89LPC930/931 is a 3 V device, but the pins are 5 V-tolerant. In quasi-bidirectional mode, if a user applies 5 V on the pin, there will be a current flowing from the pin to V_{DD}, causing extra power consumption. Therefore, applying 5 V in quasi-bidirectional mode is discouraged.

A quasi-bidirectional port pin has a Schmitt-triggered input that also has a glitch suppression circuit.

8.11.3 Open-drain output configuration

The open-drain output configuration turns off all pull-ups and only drives the pull-down transistor of the port driver when the port latch contains a logic ‘0’. To be used as a logic output, a port configured in this manner must have an external pull-up, typically a resistor tied to V_{DD}.

An open-drain port pin has a Schmitt-triggered input that also has a glitch suppression circuit.

8.11.4 Input-only configuration

The input-only port configuration has no output drivers. It is a Schmitt-triggered input that also has a glitch suppression circuit.

8.11.5 Push-pull output configuration

The push-pull output configuration has the same pull-down structure as both the open-drain and the quasi-bidirectional output modes, but provides a continuous strong pull-up when the port latch contains a logic ‘1’. The push-pull mode may be used when more source current is needed from a port output. A push-pull port pin has a Schmitt-triggered input that also has a glitch suppression circuit.

8.11.6 Port 0 analog functions

The P89LPC930/931 incorporates two Analog Comparators. In order to give the best analog function performance and to minimize power consumption, pins that are being used for analog functions must have the digital outputs and digital inputs disabled.

8.13.1 Idle mode

Idle mode leaves peripherals running in order to allow them to activate the processor when an interrupt is generated. Any enabled interrupt source or reset may terminate Idle mode.

8.13.2 Power-down mode

The Power-down mode stops the oscillator in order to minimize power consumption. The P89LPC930/931 exits Power-down mode via any reset, or certain interrupts. In Power-down mode, the power supply voltage may be reduced to the RAM keep-alive voltage V_{RAM}. This retains the RAM contents at the point where Power-down mode was entered. SFR contents are not guaranteed after V_{DD} has been lowered to V_{RAM}, therefore it is highly recommended to wake up the processor via reset in this case. V_{DD} must be raised to within the operating range before the Power-down mode is exited.

Some chip functions continue to operate and draw power during Power-down mode, increasing the total power used during Power-down. These include: Brownout detect, Watchdog Timer, Comparators (note that Comparators can be powered-down separately), and Real-Time Clock (RTC)/System Timer. The internal RC oscillator is disabled unless both the RC oscillator has been selected as the system clock **and** the RTC is enabled.

8.13.3 Total Power-down mode

This is the same as Power-down mode except that the brownout detection circuitry and the voltage comparators are also disabled to conserve additional power. The internal RC oscillator is disabled unless both the RC oscillator has been selected as the system clock **and** the RTC is enabled. If the internal RC oscillator is used to clock the RTC during Power-down, there will be high power consumption. Please use an external low frequency clock to achieve low power with the Real-Time Clock running during Power-down.

8.14 Reset

The P1.5/$\overline{RST}$ pin can function as either an active-LOW reset input or as a digital input, P1.5. The RPE (Reset Pin Enable) bit in UCFG1, when set to ‘1’, enables the external reset input function on P1.5. When cleared, P1.5 may be used as an input pin.

Remark: During a power-up sequence, the RPE selection is overridden and this pin will always function as a reset input. **An external circuit connected to this pin should not hold this pin LOW during a power-on sequence as this will keep the device in reset.** After power-up this input will function either as an external reset input or as a digital input as defined by the RPE bit. Only a power-up reset will temporarily override the selection defined by RPE bit. Other sources of reset will not override the RPE bit.

Remark: During a power cycle, V_{DD} must fall below V_{POR} (see Table 7 “DC electrical characteristics” on page 42) before power is reapplied, in order to ensure a power-on reset.

Reset can be triggered from the following sources:

8.15.3 Mode 2

Mode 2 configures the Timer register as an 8-bit Counter with automatic reload. Mode 2 operation is the same for Timer 0 and Timer 1.

8.15.4 Mode 3

When Timer 1 is in Mode 3 it is stopped. Timer 0 in Mode 3 forms two separate 8-bit counters and is provided for applications that require an extra 8-bit timer. When Timer 1 is in Mode 3 it can still be used by the serial port as a baud rate generator.

8.15.5 Mode 6

In this mode, the corresponding timer can be changed to a PWM with a full period of 256 timer clocks.

8.15.6 Timer overflow toggle output

Timers 0 and 1 can be configured to automatically toggle a port output whenever a timer overflow occurs. The same device pins that are used for the T0 and T1 count inputs are also used for the timer toggle outputs. The port outputs will be a logic ‘1’ prior to the first timer overflow when this mode is turned on.

8.16 Real-Time clock/system timer

The P89LPC930/931 has a simple Real-Time clock that allows a user to continue running an accurate timer while the rest of the device is powered-down. The Real-Time clock can be a wake-up or an interrupt source. The Real-Time clock is a 23-bit down counter comprised of a 7-bit prescaler and a 16-bit loadable down counter. When it reaches all ‘0’s, the counter will be reloaded again and the RTCF flag will be set. The clock source for this counter can be either the CPU clock (CCLK) or the XTAL oscillator, provided that the XTAL oscillator is not being used as the CPU clock. If the XTAL oscillator is used as the CPU clock, then the RTC will use CCLK as its clock source. Only power-on reset will reset the Real-Time clock and its associated SFRs to the default state.

8.17 UART

The P89LPC930/931 has an enhanced UART that is compatible with the conventional 80C51 UART except that Timer 2 overflow cannot be used as a baud rate source. The P89LPC930/931 does include an independent Baud Rate Generator. The baud rate can be selected from the oscillator (divided by a constant), Timer 1 overflow, or the independent Baud Rate Generator. In addition to the baud rate generation, enhancements over the standard 80C51 UART include Framing Error detection, automatic address recognition, selectable double buffering and several interrupt options. The UART can be operated in 4 modes: shift register, 8-bit UART, 9-bit UART, and CPU clock/32 or CPU clock/16.

8.17.1 Mode 0

Serial data enters and exits through RxD. TxD outputs the shift clock. 8 bits are transmitted or received, LSB first. The baud rate is fixed at $^{1}/_{16}$ of the CPU clock frequency.

8.17.7 Break detect

Break detect is reported in the status register (SSTAT). A break is detected when 11 consecutive bits are sensed LOW. The break detect can be used to reset the device and force the device into ISP mode.

8.17.8 Double buffering

The UART has a transmit double buffer that allows buffering of the next character to be written to SBUF while the first character is being transmitted. Double buffering allows transmission of a string of characters with only one stop bit between any two characters, as long as the next character is written between the start bit and the stop bit of the previous character.

Double buffering can be disabled. If disabled (DBMOD, i.e., SSTAT.7 = ‘0’), the UART is compatible with the conventional 80C51 UART. If enabled, the UART allows writing to SnBUF while the previous data is being shifted out. Double buffering is only allowed in Modes 1, 2 and 3. When operated in Mode 0, double buffering must be disabled (DBMOD = ‘0’).

8.17.9 Transmit interrupts with double buffering enabled (Modes 1, 2 and 3)

Unlike the conventional UART, in double buffering mode, the Tx interrupt is generated when the double buffer is ready to receive new data.

8.17.10 The 9th bit (bit 8) in double buffering (Modes 1, 2 and 3)

If double buffering is disabled TB8 can be written before or after SBUF is written, as long as TB8 is updated some time before that bit is shifted out. TB8 must not be changed until the bit is shifted out, as indicated by the Tx interrupt.

If double buffering is enabled, TB8 **must** be updated before SBUF is written, as TB8 will be double-buffered together with SBUF data.

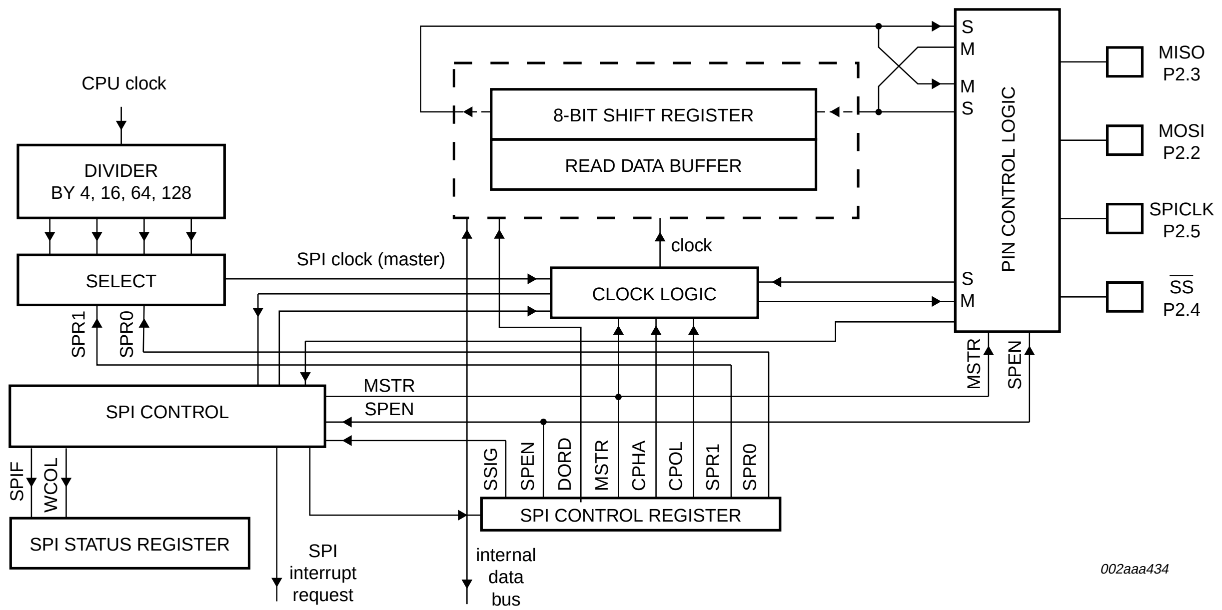


Fig 9. SPI block diagram.

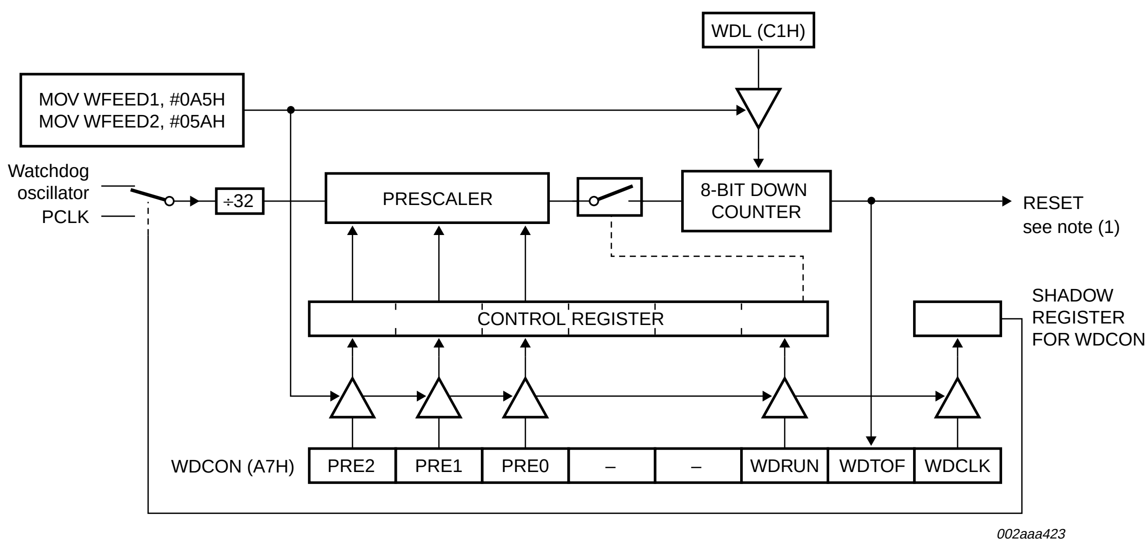
The SPI interface has four pins: SPICLK, MOSI, MISO, and $\overline{SS}$:

- SPICLK, MOSI and MISO are typically tied together between two or more SPI devices. Data flows from master to slave on MOSI (Master Out Slave In) pin and flows from slave to master on MISO (Master In Slave Out) pin. The SPICLK signal is output in the master mode and is input in the slave mode. If the SPI system is disabled, i.e. SPEN (SPCTL.6) = 0 (reset value), these pins are configured for port functions.
- $\overline{SS}$ is the optional slave select pin. In a typical configuration, an SPI master asserts one of its port pins to select one SPI device as the current slave. An SPI slave device uses its SS pin to determine whether it is selected.

Typical connections are shown in Figures 10, 11, and 12.

8.22 Watchdog timer

The watchdog timer causes a system reset when it underflows as a result of a failure to feed the timer prior to the timer reaching its terminal count. It consists of a programmable 12-bit prescaler, and an 8-bit down counter. The down counter is decremented by a tap taken from the prescaler. The clock source for the prescaler is either the PCLK or the nominal 400 kHz Watchdog oscillator. The watchdog timer can only be reset by a power-on reset. When the Watchdog feature is disabled, it can be used as an interval timer and may generate an interrupt. Figure 14 shows the watchdog timer in Watchdog mode. Feeding the watchdog requires a two-byte sequence. If PCLK is selected as the Watchdog clock and the CPU is powered-down, the watchdog is disabled. The watchdog timer has a time-out period that ranges from a few µs to a few seconds. Please refer to the *P89LPC930/931 User's Manual* for more details.



(1) Watchdog reset can also be caused by an invalid feed sequence, or by writing to WDCON not immediately followed by a feed sequence.

Fig 14. Watchdog timer in Watchdog mode (WDTE = '1').

8.23 Additional features

8.23.1 Software reset

The SRST bit in AUXR1 gives software the opportunity to reset the processor completely, as if an external reset or Watchdog reset had occurred. Care should be taken when writing to AUXR1 to avoid accidental software resets.

8.23.2 Dual data pointers

The dual Data Pointers (DPTR) provides two different Data Pointers to specify the address used with certain instructions. The DPS bit in the AUXR1 register selects one of the two Data Pointers. Bit 2 of AUXR1 is permanently wired as a logic '0' so that the DPS bit may be toggled (thereby switching Data Pointers) simply by incrementing the AUXR1 register, without the possibility of inadvertently altering other bits in the register.

the Boot Vector and Boot Status Bit. After programming the Flash, the status byte should be programmed to zero in order to allow execution of the user's application code beginning at address 0000H.

In-System Programming (ISP): In-System Programming is performed without removing the microcontroller from the system. The In-System Programming facility consists of a series of internal hardware resources coupled with internal firmware to facilitate remote programming of the P89LPC930/931 through the serial port. This firmware is provided by Philips and embedded within each P89LPC930/931 device. The Philips In-System Programming facility has made in-system programming in an embedded application possible with a minimum of additional expense in components and circuit board area. The ISP function uses five pins (V_{DD}, V_{SS}, TxD, RxD, and RST). Only a small connector needs to be available to interface your application to an external circuit in order to use this feature.

In-Application Programming (IAP): Several In-Application Programming (IAP) calls are available for use by an application program to permit selective erasing, reading, and programming of Flash sectors, pages, security bits, configuration bytes, and device id. All calls are made through a common interface, PGM_MTP. The programming functions are selected by setting up the microcontroller's registers before making a call to PGM_MTP at FF00H.

8.25 User configuration bytes

A number of user-configurable features of the P89LPC930/931 must be defined at power-up and therefore cannot be set by the program after start of execution. These features are configured through the use of the Flash byte UCFG1. Please see the *P89LPC930/931 User's Manual* for additional details.

8.26 User sector security bytes

There are eight User Sector Security Bytes, each corresponding to one sector. Please see the *P89LPC930/931 User's Manual* for additional details.

11. Dynamic characteristics

Table 8: AC characteristics

V_{DD} = 2.4 V to 3.6 V unless otherwise specified.
T_{amb} = −40 °C to +85 °C for industrial, unless otherwise specified.[1]

Symbol	Parameter	Conditions	Variable clock		f_{osc} = 12 MHz		Unit
			Min	Max	Min	Max	
f_{RCOSC}	internal RC oscillator frequency		7.189	7.557	7.189	7.557	MHz
f_{WDOSC}	internal watchdog oscillator frequency		320	520	320	520	kHz
f_{osc}	oscillator frequency		0	12	-	-	MHz
t_{CLCL}	clock cycle	see Figure 20	83	-	-	-	ns
f_{CLKP}	CLKLP active frequency		0	8	-	-	MHz
Glitch filter							
	glitch rejection, P1.5/$\overline{RST}$ pin		-	50	-	50	ns
	signal acceptance, P1.5/$\overline{RST}$ pin		125	-	125	-	ns
	glitch rejection, any pin except P1.5/$\overline{RST}$		-	15	-	15	ns
	signal acceptance, any pin except P1.5/$\overline{RST}$		50	-	50	-	ns
External clock							
t_{CHCX}	HIGH time	see Figure 20	33	$t_{CLCL} - t_{CLCX}$	33	-	ns
t_{CLCX}	LOW time	see Figure 20	33	$t_{CLCL} - t_{CHCX}$	33	-	ns
t_{CLCH}	rise time	see Figure 20	-	8	-	8	ns
t_{CHCL}	fall time	see Figure 20	-	8	-	8	ns
Shift register (UART mode 0)							
t_{XLXL}	serial port clock cycle time		16 t_{CLCL}	-	1333	-	ns
t_{QVXH}	output data set-up to clock rising edge		13 t_{CLCL}	-	1083	-	ns
t_{XHQX}	output data hold after clock rising edge		-	t_{CLCL} + 20	-	103	ns
t_{XHDX}	input data hold after clock rising edge		-	0	-	0	ns
t_{DVXH}	input data valid to clock rising edge		150	-	150	-	ns
SPI interface							
f_{SPI}	Operating frequency						
	2.0 MHz (Slave)		0	$^{CCLK}/_{6}$	0	2.0	MHz
	3.0 MHz (Master)		-	$^{CCLK}/_{4}$	-	-	MHz
t_{SPICYC}	Cycle time	see Figures 15, 16, 17, 18					
	2.0 MHz (Slave)		$^{6}/_{CCLK}$	-	500	-	ns
	3.0 MHz (Master)		$^{4}/_{CCLK}$	-	-	-	ns
$t_{SPILEAD}$	Enable lead time (Slave)	see Figures 17, 18					
	2.0 MHz		250	-	250	-	ns

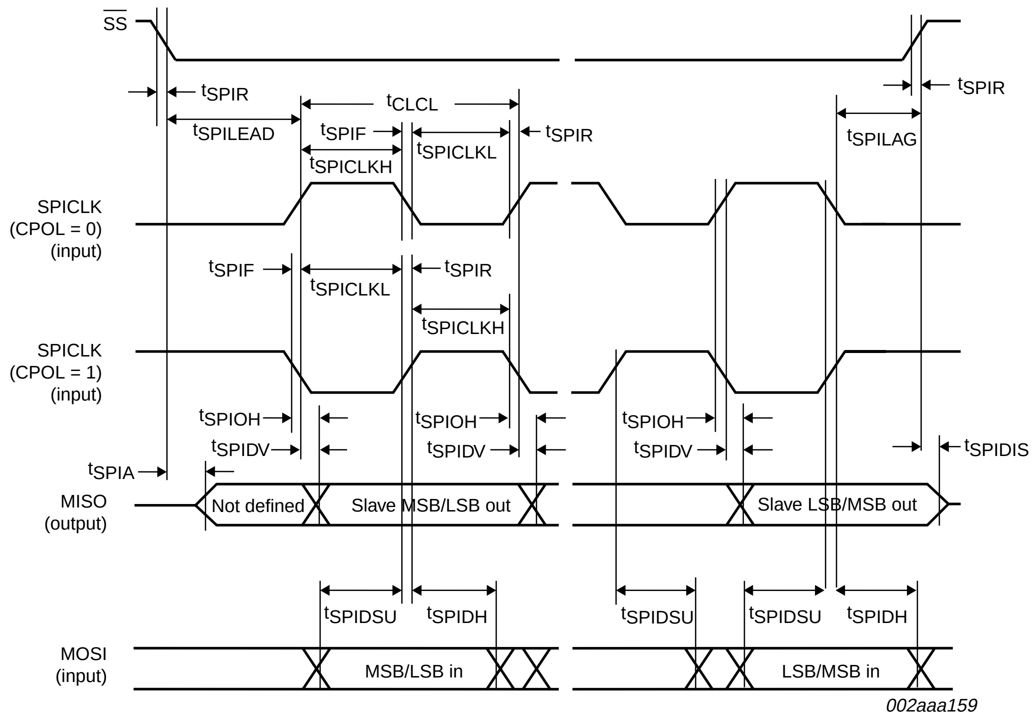


Fig 18. SPI slave timing (CPHA = 1).

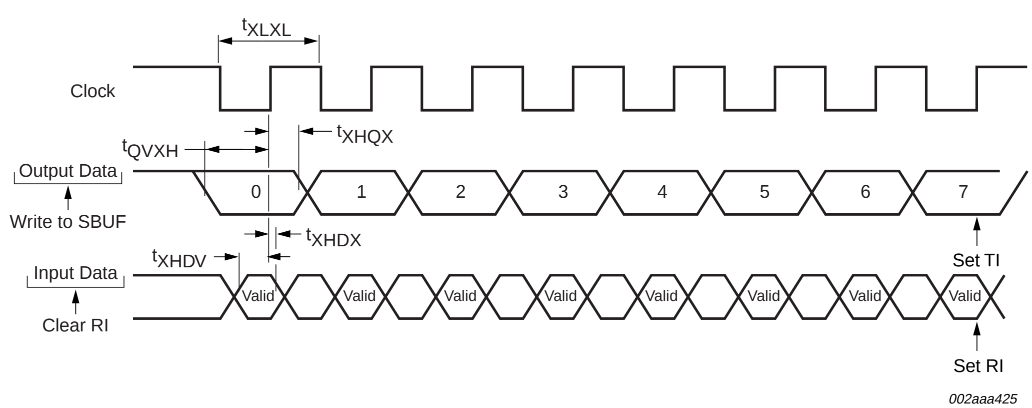


Fig 19. Shift register mode timing.

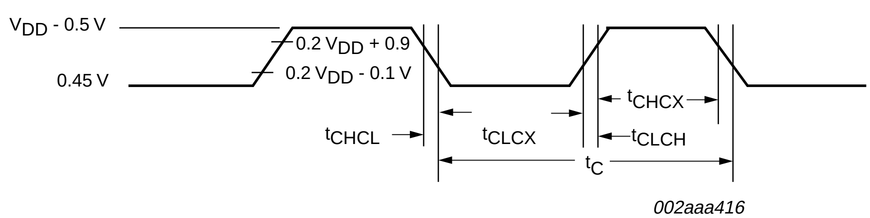


Fig 20. External clock timing.

Table 10: AC characteristics, ISP entry mode

V_{DD} = 2.4 V to 3.6 V, unless otherwise specified.
T_{amb} = –40 °C to +85 °C for industrial, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{VR}	$\overline{RST}$ delay from V_{DD} active		50	-	-	µs
t_{RH}	$\overline{RST}$ HIGH time		1	-	32	µs
t_{RL}	$\overline{RST}$ LOW time		1	-	-	µs

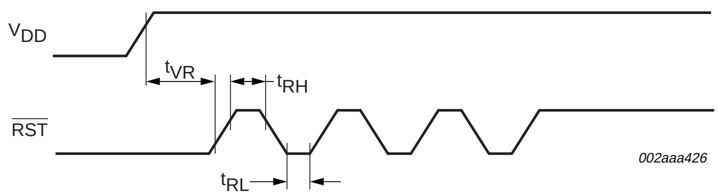


Fig 21. ISP entry waveform.

12. Comparator electrical characteristics

Table 11: Comparator electrical characteristics

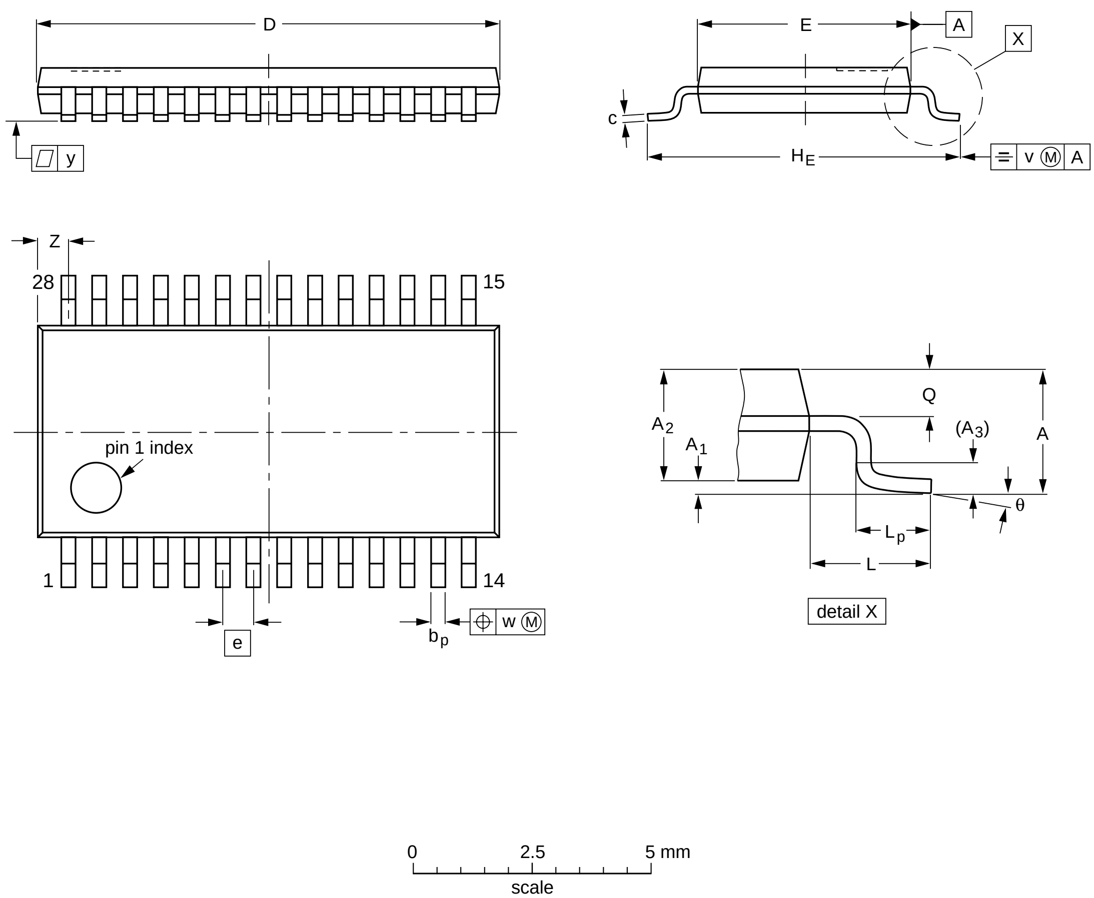
V_{DD} = 2.4 V to 3.6 V, unless otherwise specified.
T_{amb} = –40 °C to +85 °C for industrial, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IO}	offset voltage comparator inputs		-	-	±20	mV
V_{CR}	common mode range comparator inputs		0	-	V_{DD} – 0.3	V
CMRR	common mode rejection ratio	[1]	-	-	–50	dB
	response time		-	250	500	ns
	comparator enable to output valid		-	-	10	µs
I_{IL}	input leakage current, comparator	$0 < V_{IN} < V_{DD}$	-	-	±10	µA

[1] This parameter is characterized, but not tested in production.

13. Package outline

TSSOP28: plastic thin shrink small outline package; 28 leads; body width 4.4 mm **SOT361-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	9.8 9.6	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.8 0.5	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT361-1		MO-153				~~99-12-27~~ 03-02-19

Fig 22. SOT361-1 (TSSOP28).

14. Revision history

Table 12: Revision history

Rev	Date	CPCN	Description
05	20041215	-	**Product data (9397 750 14472)** Modification: • Added 18 MHz information.
04	20040106	-	**Product data (9397 750 12284); ECN 853-2406 01-A15015 dated 16 December 2003**
03	20031006	-	**Product data (9397 750 12122); ECN 853-2406 30390 dated 30 September 2003**
02	20030526	-	**Objective data (9397 750 11536)**
01	20030514	-	**Preliminary data (9397 750 11386)**