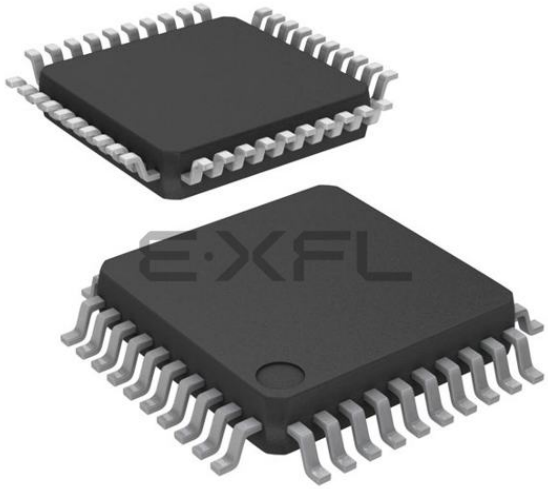
# Renesas Electronics America Inc - R5F10RBAGFP#50 Datasheet



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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | RL78 |
| Core Size | 16-Bit |
| Speed | 24MHz |
| Connectivity | CSI, I²C, LINbus, UART/USART |
| Peripherals | DMA, LCD, LVD, POR, PWM, WDT |
| Number of I/O | 20 |
| Program Memory Size | 16KB (16K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 2K x 8 |
| RAM Size | 1K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.6V ~ 5.5V |
| Data Converters | A/D 4x8/10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 32-LQFP |
| Supplier Device Package | 32-LQFP (7x7) |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f10rbagfp-50 |

### 1.3.4 52-pin products

- 52-pin plastic LQFP (10 × 10)

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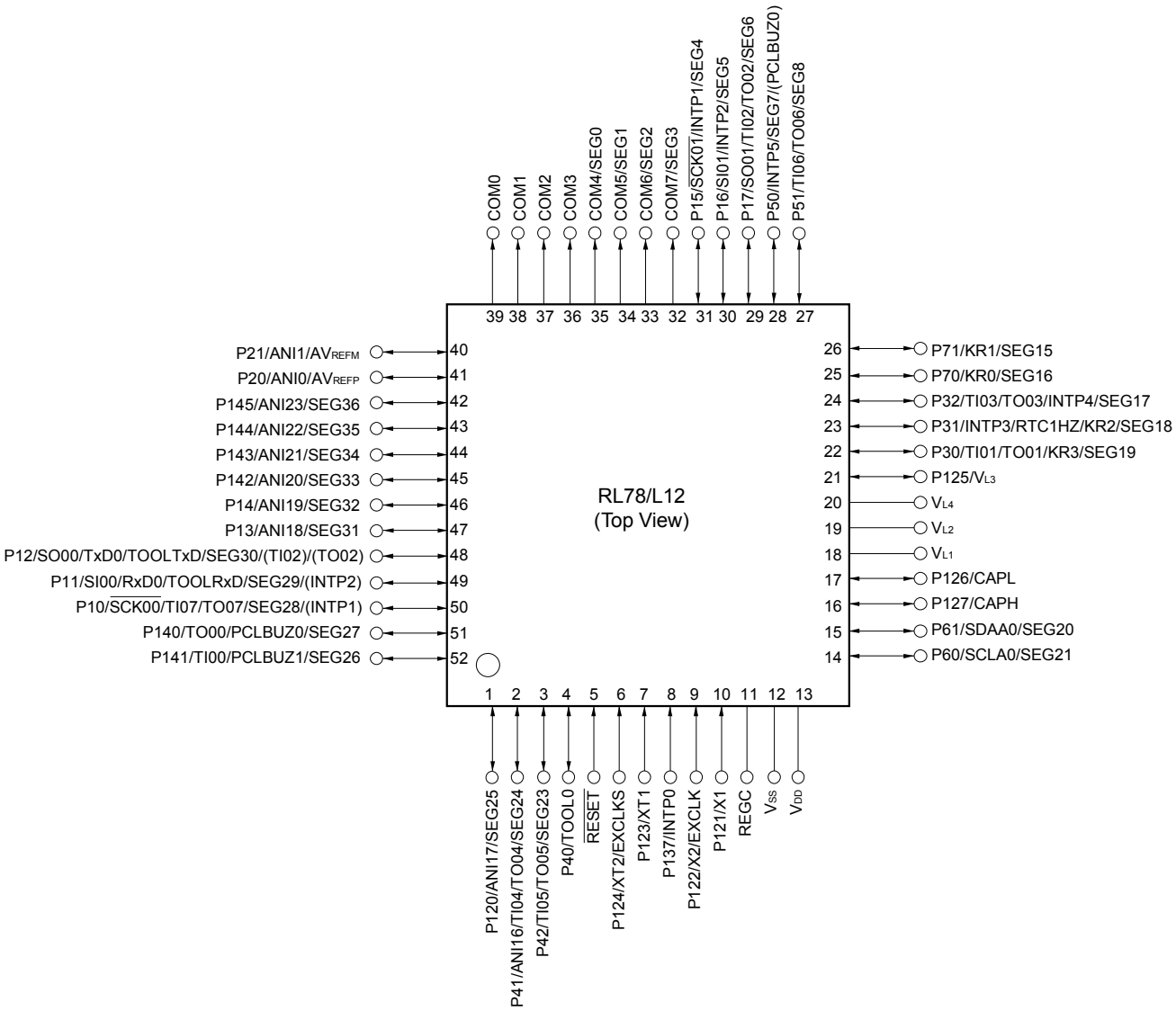


**Caution Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).**

**Remarks 1.** For pin identification, see **1.4 Pin Identification**.

**2.** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

- 64-pin plastic LQFP (fine pitch) (10 × 10)
- 64-pin plastic LQFP (12 × 12)

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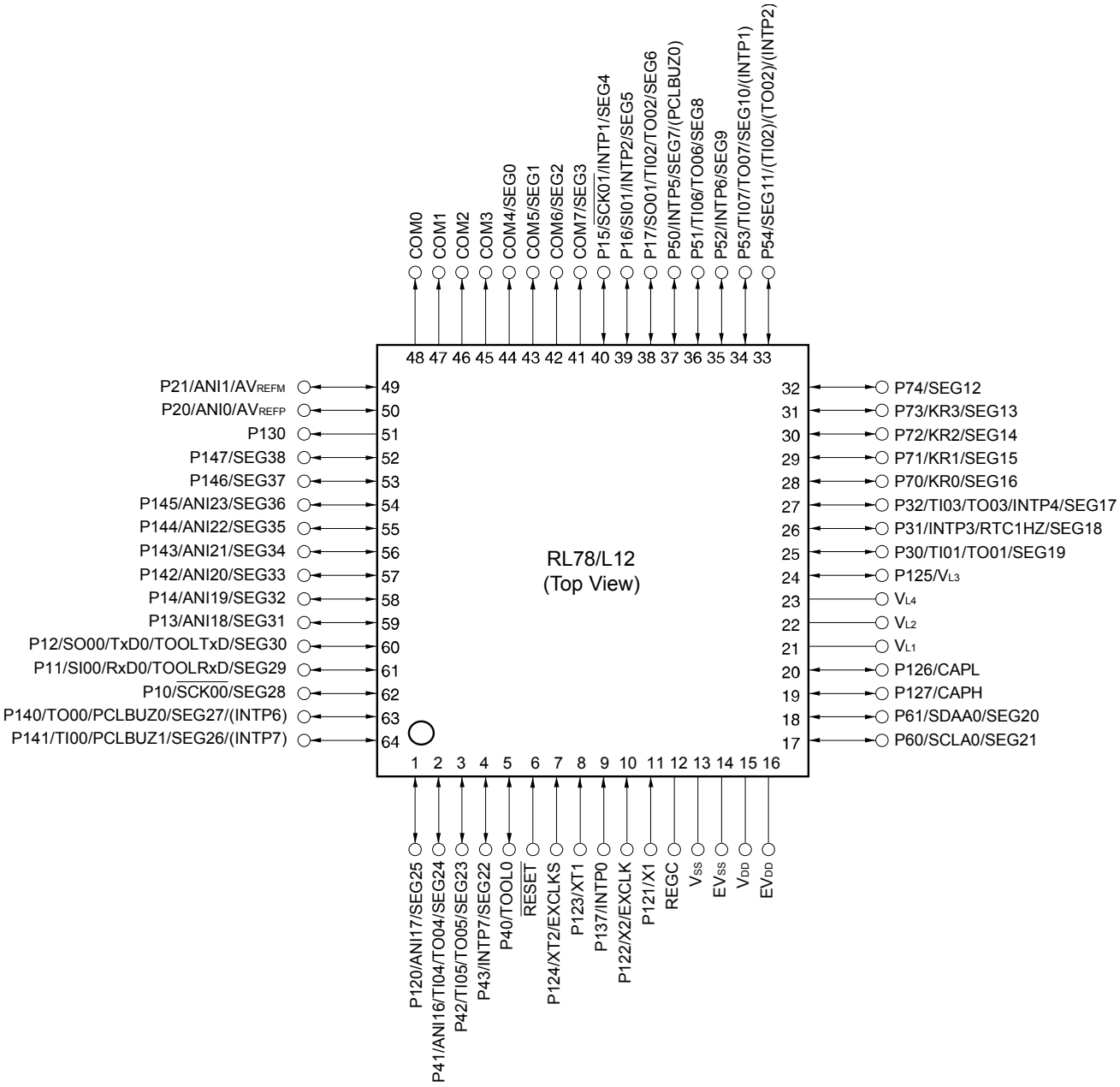



**Cautions 1. Make EVSS pin the same potential as VSS pin.**

**2. Make VDD pin the same potential as EVDD pin.**

**3. Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).**

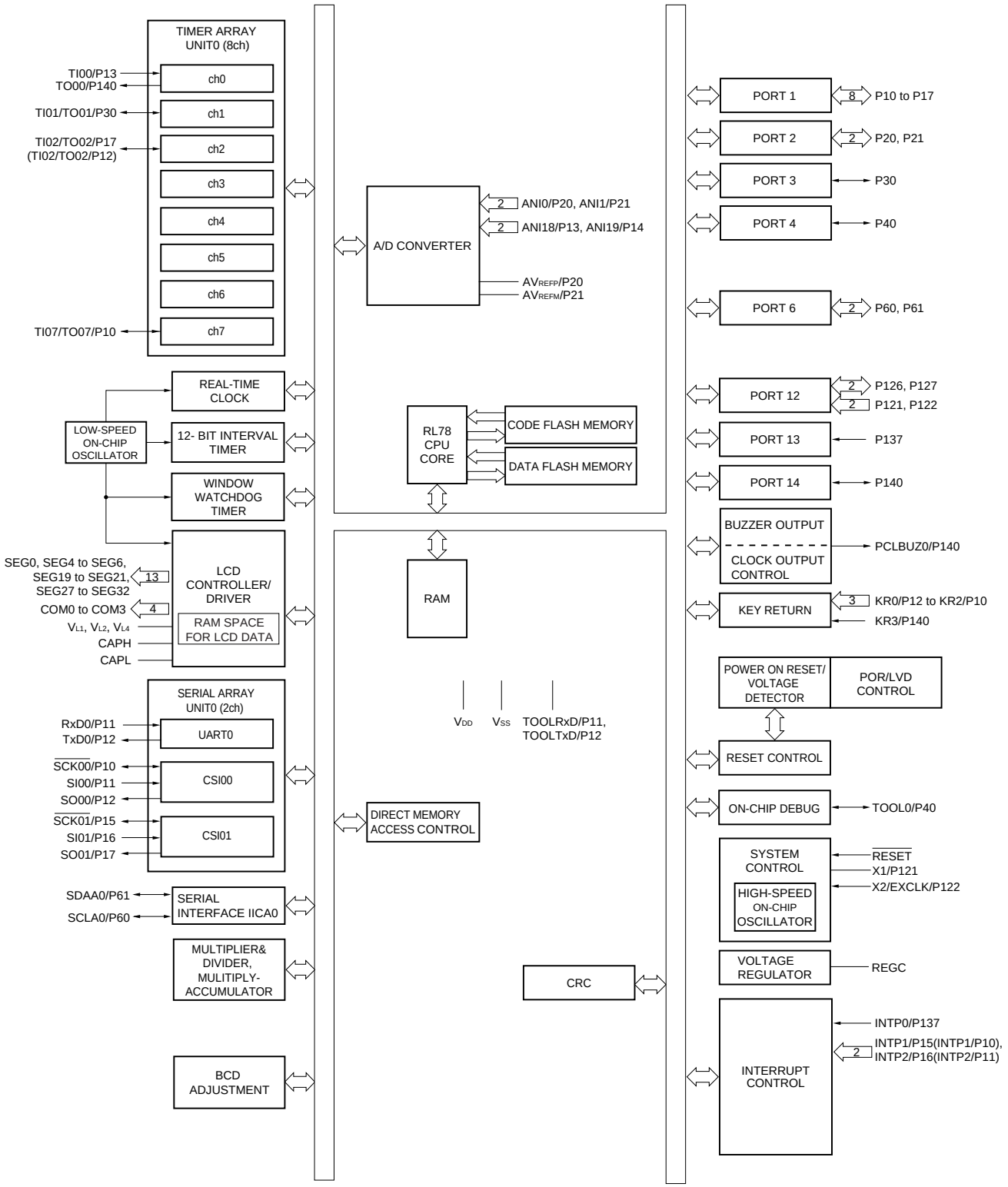
**Remarks 1.** For pin identification, see **1.4 Pin Identification.**

**2.** When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the VDD and EVDD pins and connect the VSS and EVSS pins to separate ground lines.

**3.** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

## 1.5 Block Diagram

### 1.5.1 32-pin products



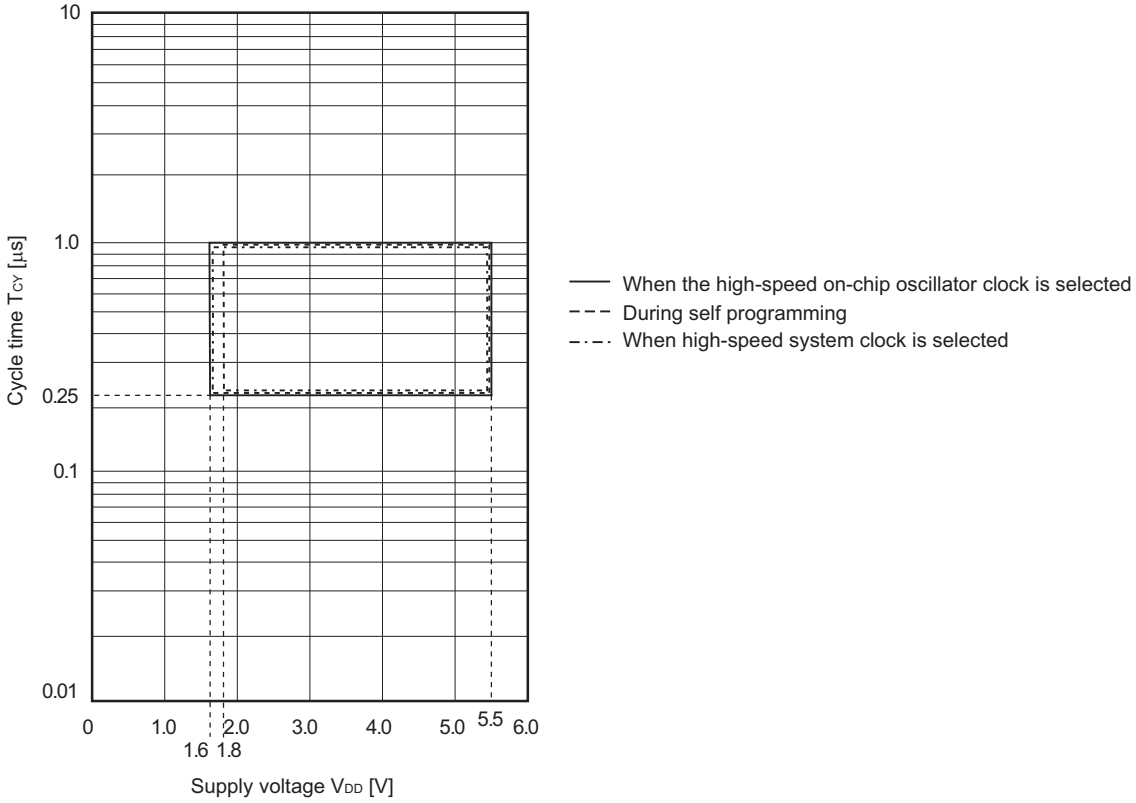

**Remark** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR)

**($T_A$ = –40 to +85°C, 1.6 V ≤ $EV_{DD}$ = $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS}$ = 0 V)** **(2/3)**

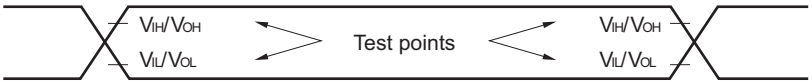
| Parameter | Symbol | Conditions | | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|
| Supply current Note 1 | $I_{DD2}$ Note 2 | HALT mode | HS (high-speed main) mode Note 7 | $f_{IH}$ = 24 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.44 | 1.28 | mA |
| | | | | | $V_{DD}$ = 3.0 V | | 0.44 | 1.28 | mA |
| | | | | $f_{IH}$ = 16 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.40 | 1.00 | mA |
| | | | | | $V_{DD}$ = 3.0 V | | 0.40 | 1.00 | mA |
| | | | LS (low-speed main) mode Note 7 | $f_{IH}$ = 8 MHz Note 4 | $V_{DD}$ = 3.0 V | | 260 | 530 | μA |
| | | | | | $V_{DD}$ = 2.0 V | | 260 | 530 | μA |
| | | | LV (low-voltage main) mode Note 7 | $f_{IH}$ = 4 MHz Note 4 | $V_{DD}$ = 3.0 V | | 420 | 640 | μA |
| | | | | | $V_{DD}$ = 2.0 V | | 420 | 640 | μA |
| | | | HS (high-speed main) mode Note 7 | $f_{MX}$ = 20 MHz Note 3, $V_{DD}$ = 5.0 V | Square wave input | | 0.28 | 1.00 | mA |
| | | | | | Resonator connection | | 0.45 | 1.17 | mA |
| | | | | $f_{MX}$ = 20 MHz Note 3, $V_{DD}$ = 3.0 V | Square wave input | | 0.28 | 1.00 | mA |
| | | | | | Resonator connection | | 0.45 | 1.17 | mA |
| | | | | $f_{MX}$ = 10 MHz Note 3, $V_{DD}$ = 5.0 V | Square wave input | | 0.19 | 0.60 | mA |
| | | | | | Resonator connection | | 0.26 | 0.67 | mA |
| | | | | $f_{MX}$ = 10 MHz Note 3, $V_{DD}$ = 3.0 V | Square wave input | | 0.19 | 0.60 | mA |
| | | | | | Resonator connection | | 0.26 | 0.67 | mA |
| | | | LS (low-speed main) mode Note 7 | $f_{MX}$ = 8 MHz Note 3, $V_{DD}$ = 3.0 V | Square wave input | | 95 | 330 | μA |
| | | | | | Resonator connection | | 145 | 380 | μA |
| | | | | $f_{MX}$ = 8 MHz Note 3, $V_{DD}$ = 2.0 V | Square wave input | | 95 | 330 | μA |
| | | | | | Resonator connection | | 145 | 380 | μA |
| | | | Subsystem clock operation | $f_{SUB}$ = 32.768 kHz Note 5 $T_A$ = –40°C | Square wave input | | 0.31 | 0.57 | μA |
| | | | | | Resonator connection | | 0.50 | 0.76 | μA |
| | | | | $f_{SUB}$ = 32.768 kHz Note 5 $T_A$ = +25°C | Square wave input | | 0.37 | 0.57 | μA |
| | | | | | Resonator connection | | 0.56 | 0.76 | μA |
| | | | | $f_{SUB}$ = 32.768 kHz Note 5 $T_A$ = +50°C | Square wave input | | 0.46 | 1.17 | μA |
| | | | | | Resonator connection | | 0.65 | 1.36 | μA |
| | | | | $f_{SUB}$ = 32.768 kHz Note 5 $T_A$ = +70°C | Square wave input | | 0.57 | 1.97 | μA |
| | | | | | Resonator connection | | 0.76 | 2.16 | μA |
| | | | | $f_{SUB}$ = 32.768 kHz Note 5 $T_A$ = +85°C | Square wave input | | 0.85 | 3.37 | μA |
| | | | | | Resonator connection | | 1.04 | 3.56 | μA |
| | $I_{DD3}$ Note 6 | STOP mode Note 8 | $T_A$ = –40°C | | | | 0.17 | 0.50 | μA |
| | | | $T_A$ = +25°C | | | | 0.23 | 0.50 | μA |
| | | | $T_A$ = +50°C | | | | 0.32 | 1.10 | μA |
| | | | $T_A$ = +70°C | | | | 0.43 | 1.90 | μA |
| | | | $T_A$ = +85°C | | | | 0.71 | 3.30 | μA |

(**Notes** and **Remarks** are listed on the next page.)

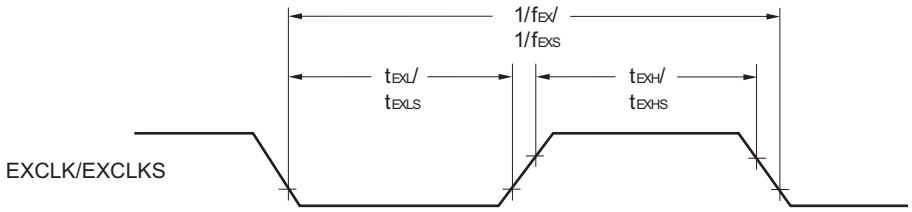
$T_{CY}$ vs $V_{DD}$ (LV (low-voltage main) mode)




**AC Timing Test Points**




**External System Clock Timing**



### (2) $I^2C$ fast mode

**($T_A$ = –40 to +85°C, 1.6 V ≤ $EV_{DD}$ = $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | | HS (high-speed main) Mode | | LS (low-speed main) Mode | | LV (low-voltage main) Mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | MIN. | MIN. | MAX. | MIN. | |
| SCLA0 clock frequency | $f_{SCL}$ | Fast mode: $f_{CLK}$ ≥ 3.5 MHz | 2.7 V ≤ $EV_{DD}$ ≤ 5.5 V | 0 | 400 | 0 | 400 | 0 | 400 | kHz |
| | | | 2.4 V ≤ $EV_{DD}$ ≤ 5.5 V | 0 | 400 | 0 | 400 | 0 | 400 | |
| | | | 1.8 V ≤ $EV_{DD}$ ≤ 5.5 V | | | 0 | 400 | 0 | 400 | |
| Setup time of restart condition | $t_{SU:STA}$ | 2.7 V ≤ $EV_{DD}$ ≤ 5.5 V | | 0.6 | | 0.6 | | 0.6 | | μs |
| | | 2.4 V ≤ $EV_{DD}$ ≤ 5.5 V | | 0.6 | | 0.6 | | 0.6 | | |
| | | 1.8 V ≤ $EV_{DD}$ ≤ 5.5 V | | | | 0.6 | | 0.6 | | |
| Hold time [Note 1] | $t_{HD:STA}$ | 2.7 V ≤ $EV_{DD}$ ≤ 5.5 V | | 0.6 | | 0.6 | | 0.6 | | μs |
| | | 2.4 V ≤ $EV_{DD}$ ≤ 5.5 V | | 0.6 | | 0.6 | | 0.6 | | |
| | | 1.8 V ≤ $EV_{DD}$ ≤ 5.5 V | | | | 0.6 | | 0.6 | | |
| Hold time when SCLA0 = “L” | $t_{LOW}$ | 2.7 V ≤ $EV_{DD}$ ≤ 5.5 V | | 1.3 | | 1.3 | | 1.3 | | μs |
| | | 2.4 V ≤ $EV_{DD}$ ≤ 5.5 V | | 1.3 | | 1.3 | | 1.3 | | |
| | | 1.8 V ≤ $EV_{DD}$ ≤ 5.5 V | | | | 1.3 | | 1.3 | | |
| Hold time when SCLA0 = “H” | $t_{HIGH}$ | 2.7 V ≤ $EV_{DD}$ ≤ 5.5 V | | 0.6 | | 0.6 | | 0.6 | | μs |
| | | 2.4 V ≤ $EV_{DD}$ ≤ 5.5 V | | 0.6 | | 0.6 | | 0.6 | | |
| | | 1.8 V ≤ $EV_{DD}$ ≤ 5.5 V | | | | 0.6 | | 0.6 | | |
| Data setup time (reception) | $t_{SU:DAT}$ | 2.7 V ≤ $EV_{DD}$ ≤ 5.5 V | | 100 | | 100 | | 100 | | ns |
| | | 2.4 V ≤ $EV_{DD}$ ≤ 5.5 V | | 100 | | 100 | | 100 | | |
| | | 1.8 V ≤ $EV_{DD}$ ≤ 5.5 V | | | | 100 | | 100 | | |
| Data hold time (transmission)[Note 2] | $t_{HD:DAT}$ | 2.7 V ≤ $EV_{DD}$ ≤ 5.5 V | | 0 | 0.9 | 0 | 0.9 | 0 | 0.9 | μs |
| | | 2.4 V ≤ $EV_{DD}$ ≤ 5.5 V | | 0 | 0.9 | 0 | 0.9 | 0 | 0.9 | |
| | | 1.8 V ≤ $EV_{DD}$ ≤ 5.5 V | | | | 0 | 0.9 | 0 | 0.9 | |
| Setup time of stop condition | $t_{SU:STO}$ | 2.7 V ≤ $EV_{DD}$ ≤ 5.5 V | | 0.6 | | 0.6 | | 0.6 | | μs |
| | | 2.4 V ≤ $EV_{DD}$ ≤ 5.5 V | | 0.6 | | 0.6 | | 0.6 | | |
| | | 1.8 V ≤ $EV_{DD}$ ≤ 5.5 V | | | | 0.6 | | 0.6 | | |
| Bus-free time | $t_{BUF}$ | 2.7 V ≤ $EV_{DD}$ ≤ 5.5 V | | 1.3 | | 1.3 | | 1.3 | | μs |
| | | 2.4 V ≤ $EV_{DD}$ ≤ 5.5 V | | 1.3 | | 1.3 | | 1.3 | | |
| | | 1.8 V ≤ $EV_{DD}$ ≤ 5.5 V | | | | 1.3 | | 1.3 | | |

**Notes 1.** The first clock pulse is generated after this period when the start/restart condition is detected.

**2.** The maximum value (MAX.) of $t_{HD:DAT}$ is during normal transfer and a wait state is inserted in the $\overline{ACK}$ (acknowledge) timing.

**Remark** The maximum value of Cb (communication line capacitance) and the value of Rb (communication line pull-up resistor) at that time in each mode are as follows.

Fast mode: $C_b$ = 320 pF, $R_b$ = 1.1 kΩ

## 2.7.2 Internal voltage boosting method

**(1) 1/3 bias method**

**($T_A$ = –40 to +85°C, 1.8 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| LCD output voltage variation range | $V_{L1}$ | C1 to C4[Note 1] = 0.47 μF | VLCD = 04H | 0.90 | 1.00 | 1.08 | V |
| | | | VLCD = 05H | 0.95 | 1.05 | 1.13 | V |
| | | | VLCD = 06H | 1.00 | 1.10 | 1.18 | V |
| | | | VLCD = 07H | 1.05 | 1.15 | 1.23 | V |
| | | | VLCD = 08H | 1.10 | 1.20 | 1.28 | V |
| | | | VLCD = 09H | 1.15 | 1.25 | 1.33 | V |
| | | | VLCD = 0AH | 1.20 | 1.30 | 1.38 | V |
| | | | VLCD = 0BH | 1.25 | 1.35 | 1.43 | V |
| | | | VLCD = 0CH | 1.30 | 1.40 | 1.48 | V |
| | | | VLCD = 0DH | 1.35 | 1.45 | 1.53 | V |
| | | | VLCD = 0EH | 1.40 | 1.50 | 1.58 | V |
| | | | VLCD = 0FH | 1.45 | 1.55 | 1.63 | V |
| | | | VLCD = 10H | 1.50 | 1.60 | 1.68 | V |
| | | | VLCD = 11H | 1.55 | 1.65 | 1.73 | V |
| | | | VLCD = 12H | 1.60 | 1.70 | 1.78 | V |
| | | | VLCD = 13H | 1.65 | 1.75 | 1.83 | V |
| Doubler output voltage | $V_{L2}$ | C1 to C4[Note 1] = 0.47 μF | | 2 $V_{L1}$ – 0.1 | 2 $V_{L1}$ | 2 $V_{L1}$ | V |
| Tripler output voltage | $V_{L4}$ | C1 to C4[Note 1] = 0.47 μF | | 3 $V_{L1}$ – 0.15 | 3 $V_{L1}$ | 3 $V_{L1}$ | V |
| Reference voltage setup time[Note 2] | $t_{VWAIT1}$ | | | 5 | | | ms |
| Voltage boost wait time[Note 3] | $t_{VWAIT2}$ | C1 to C4[Note 1] = 0.47 μF | | 500 | | | ms |

**Notes 1.** This is a capacitor that is connected between voltage pins used to drive the LCD.
C1: A capacitor connected between CAPH and CAPL
C2: A capacitor connected between $V_{L1}$ and GND
C3: A capacitor connected between $V_{L2}$ and GND
C4: A capacitor connected between $V_{L4}$ and GND
C1 = C2 = C3 = C4 = 0.47 μF±30%

**2.** This is the time required to wait from when the reference voltage is specified by using the VLCD register (or when the internal voltage boosting method is selected [by setting the MDSET1 and MDSET0 bits of the LCDM0 register to 01B] if the default value reference voltage is used) until voltage boosting starts (VLCON = 1).

**3.** This is the wait time from when voltage boosting is started (VLCON = 1) until display is enabled (LCDON = 1).

**Absolute Maximum Ratings ($T_A$ = 25°C) (2/3)**

| Parameter | Symbols | Conditions | | Ratings | Unit |
|---|---|---|---|---|---|
| LCD voltage | $V_{L1}$ | $V_{L1}$ voltage[Note 1] | | –0.3 to +2.8 and –0.3 to $V_{L4}$ + 0.3 | V |
| | $V_{L2}$ | $V_{L2}$ voltage[Note 1] | | –0.3 to $V_{L4}$ + 0.3[Note 2] | V |
| | $V_{L3}$ | $V_{L3}$ voltage[Note 1] | | –0.3 to $V_{L4}$ + 0.3[Note 2] | V |
| | $V_{L4}$ | $V_{L4}$ voltage[Note 1] | | –0.3 to +6.5 | V |
| | $V_{LCAP}$ | CAPL, CAPH voltage[Note 1] | | –0.3 to $V_{L4}$ + 0.3[Note 2] | V |
| | $V_{LOUT}$ | COM0 to COM7, SEG0 to SEG38, output voltage | External resistance division method | –0.3 to $V_{DD}$ + 0.3[Note 2] | V |
| | | | Capacitor split method | –0.3 to $V_{DD}$ + 0.3[Note 2] | |
| | | | Internal voltage boosting method | –0.3 to $V_{L4}$ + 0.3[Note 2] | |

**Notes 1.** This value only indicates the absolute maximum ratings when applying voltage to the $V_{L1}$, $V_{L2}$, $V_{L3}$, and $V_{L4}$ pins; it does not mean that applying voltage to these pins is recommended. When using the internal voltage boosting method or capacitance split method, connect these pins to $V_{SS}$ via a capacitor (0.47 $\mu$F ± 30%) and connect a capacitor (0.47 $\mu$F ± 30%) between the CAPL and CAPH pins.

**2.** Must be 6.5 V or lower.

**Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.**

**Remark** $V_{SS}$ : Reference voltage

## 3.3 DC Characteristics

### 3.3.1 Pin characteristics

**($T_A$ = –40 to +105°C, 2.4 V ≤ $EV_{DD}$ = $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS}$ = 0 V) (1/5)**

| Items | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Output current, high[Note 1] | $I_{OH1}$ | Per pin for P10 to P17, P30 to P32, P40 to P43, P50 to P54, P70 to P74, P120, P125 to P127, P130, P140 to P147 | | | | -3.0 [Note 2] | mA |
| | | Total of P10 to P14, P40 to P43, P120, P130, P140 to P147 (When duty = 70% [Note 3]) | 4.0 V ≤ $EV_{DD}$ ≤ 5.5 V | | | -30.0 | mA |
| | | | 2.7 V ≤ $EV_{DD}$ < 4.0 V | | | –8.0 | mA |
| | | | 2.4 V ≤ $EV_{DD}$ < 2.7 V | | | –4.0 | mA |
| | | Total of P15 to P17, P30 to P32, P50 to P54, P70 to P74, P125 to P127 (When duty = 70% [Note 3]) | 4.0 V ≤ $EV_{DD}$ ≤ 5.5 V | | | -30.0 | mA |
| | | | 2.7 V ≤ $EV_{DD}$ < 4.0 V | | | –15.0 | mA |
| | | | 2.4 V ≤ $EV_{DD}$ < 2.7 V | | | –8.0 | mA |
| | | Total of all pins (When duty = 70% [Note 3]) | | | | -60.0 | mA |
| | $I_{OH2}$ | P20, P21 | Per pin | | | –0.1 | mA |
| | | | Total of all pins | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | | | –0.2 | mA |

**Notes 1.** Value of current at which the device operation is guaranteed even if the current flows from the $V_{DD}$ and $EV_{DD}$ pins to an output pin.

**2.** Do not exceed the total current value.

**3.** Specification under conditions where the duty factor ≤ 70%.
The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = ($I_{OH}$ × 0.7)/(n × 0.01)

<Example> Where n = 80% and $I_{OH}$ = –30.0 mA

Total output current of pins = (–30.0 × 0.7)/(80 × 0.01) ≅ –26.25 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

**Caution P10, P12, P15, and P17 do not output high level in N-ch open-drain mode.**

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

**($T_A$ = –40 to +105°C, 2.4 V ≤ $EV_{DD}$ = $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS}$ = 0 V) (2/5)**

| Items | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Output current, low Note 1 | $I_{OL1}$ | Per pin for P10 to P17, P30 to P32, P40 to P43, P50 to P54, P70 to P74, P120, P125 to P127, P130, P140 to P147 | | | | 8.5 Note 2 | mA |
| | | Per pin for P60, P61 | | | | 15.0 Note 2 | mA |
| | | Total of P10 to P14, P40 to P43, P120, P130, P140 to P147 (When duty = 70% Note 3) | 4.0 V ≤ $EV_{DD}$ ≤ 5.5 V | | | 40.0 | mA |
| | | | 2.7 V ≤ $EV_{DD}$ < 4.0 V | | | 15.0 | mA |
| | | | 2.4 V ≤ $EV_{DD}$ < 2.7 V | | | 9.0 | mA |
| | | Total of P15 to P17, P30 to P32, P50 to P54, P60, P61, P70 to P74, P125 to P127 (When duty = 70% Note 3) | 4.0 V ≤ $EV_{DD}$ ≤ 5.5 V | | | 40.0 | mA |
| | | | 2.7 V ≤ $EV_{DD}$ < 4.0 V | | | 35.0 | mA |
| | | | 2,4 V ≤ $EV_{DD}$ < 2.7 V | | | 20.0 | mA |
| | | Total of all pins (When duty = 70% Note 3) | | | | 80.0 | mA |
| | $I_{OL2}$ | P20, P21 | Per pin | | | 0.4 | mA |
| | | | Total of all pins | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | | | 0.8 | mA |

**Notes 1.** Value of current at which the device operation is guaranteed even if the current flows from the $V_{DD}$ and $EV_{DD}$ pins to an output pin.

**2.** Do not exceed the total current value.

**3.** Specification under conditions where the duty factor ≤ 70%.
The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = ($I_{OL}$ × 0.7)/(n × 0.01)

<Example> Where n = 80% and $I_{OL}$ = 40.0 mA

Total output current of pins = (40.0 × 0.7)/(80 × 0.01) ≅ 35.0 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

**($T_A$ = –40 to +105°C, 2.4 V ≤ $EV_{DD}$ = $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS}$ = 0 V) (3/5)**

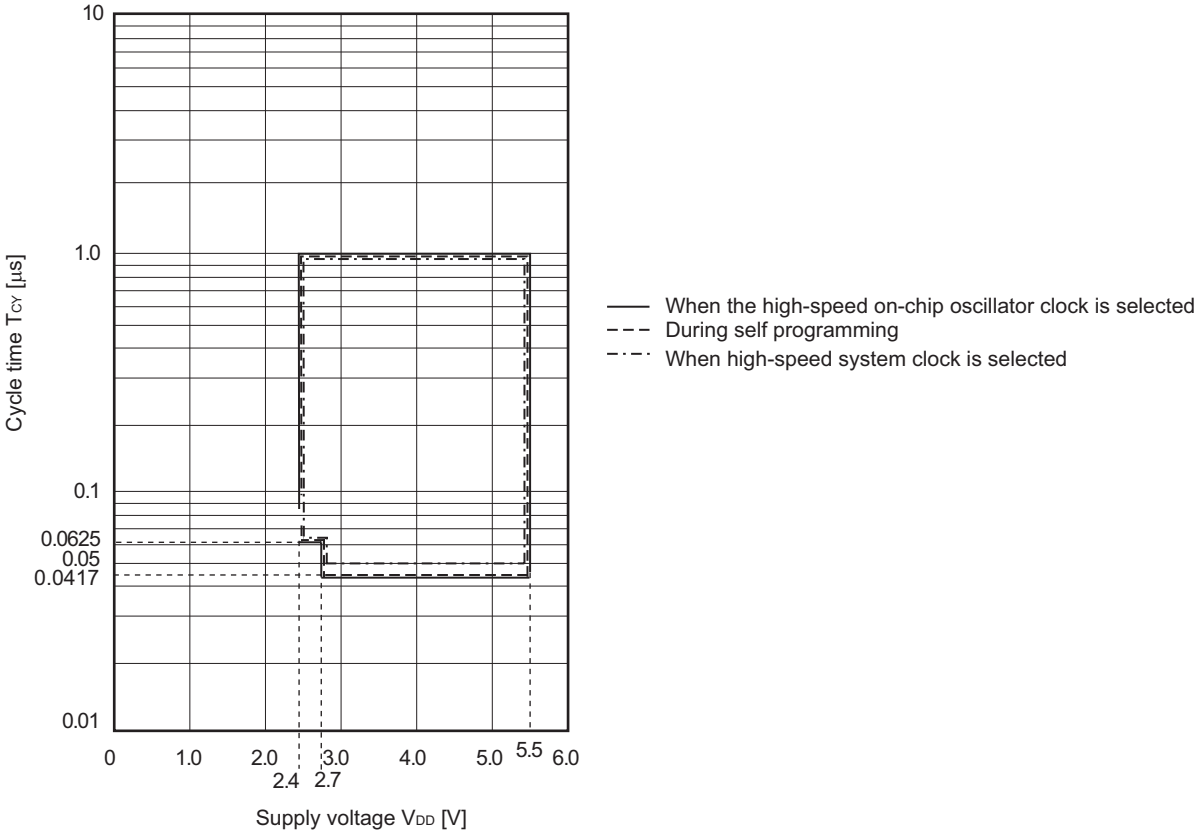
| Items | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Input voltage, high | $V_{IH1}$ | P10 to P17, P30 to P32, P40 to P43, P50 to P54, P70 to P74, P120, P125 to P127, P140 to P147 | Normal input buffer | 0.8$EV_{DD}$ | | $EV_{DD}$ | V |
| | $V_{IH2}$ | P10, P11, P15, P16 | TTL input buffer 4.0 V ≤ $EV_{DD}$ ≤ 5.5 V | 2.2 | | $EV_{DD}$ | V |
| | | | TTL input buffer 3.3 V ≤ $EV_{DD}$ < 4.0 V | 2.0 | | $EV_{DD}$ | V |
| | | | TTL input buffer 2.4 V ≤ $EV_{DD}$ < 3.3 V | 1.50 | | $EV_{DD}$ | V |
| | $V_{IH3}$ | P20, P21 | | 0.7$V_{DD}$ | | $V_{DD}$ | V |
| | $V_{IH4}$ | P60, P61 | | 0.7$EV_{DD}$ | | $EV_{DD}$ | V |
| | $V_{IH5}$ | P121 to P124, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$ | | 0.8$V_{DD}$ | | $V_{DD}$ | V |
| Input voltage, low | $V_{IL1}$ | P10 to P17, P30 to P32, P40 to P43, P50 to P54, P70 to P74, P120, P125 to P127, P140 to P147 | Normal input buffer | 0 | | 0.2$EV_{DD}$ | V |
| | $V_{IL2}$ | P10, P11, P15, P16 | TTL input buffer 4.0 V ≤ $EV_{DD}$ ≤ 5.5 V | 0 | | 0.8 | V |
| | | | TTL input buffer 3.3 V ≤ $EV_{DD}$ < 4.0 V | 0 | | 0.5 | V |
| | | | TTL input buffer 2.4 V ≤ $EV_{DD}$ < 3.3 V | 0 | | 0.32 | V |
| | $V_{IL3}$ | P20, P21 | | 0 | | 0.3$V_{DD}$ | V |
| | $V_{IL4}$ | P60, P61 | | 0 | | 0.3$EV_{DD}$ | V |
| | $V_{IL5}$ | P121 to P124, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$ | | 0 | | 0.2$V_{DD}$ | V |

**Caution The maximum value of $V_{IH}$ of pins P10, P12, P15, and P17 is $EV_{DD}$, even in the N-ch open-drain mode.**

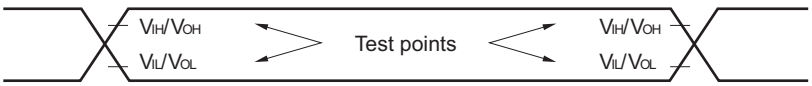
**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

**Minimum Instruction Execution Time during Main System Clock Operation**

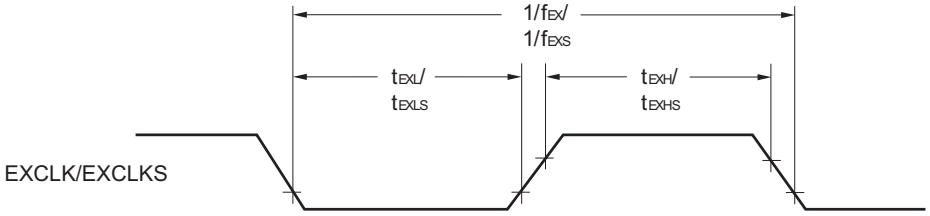
$T_{CY}$ vs $V_{DD}$ (HS (high-speed main) mode)




**AC Timing Test Points**

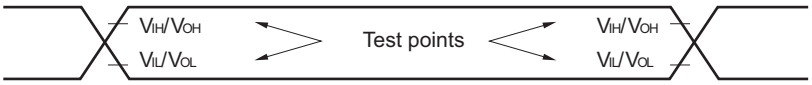



**External System Clock Timing**



## 3.5 Peripheral Functions Characteristics

**AC Timing Test Points**




### 3.5.1 Serial array unit

**(1) During communication at same potential (UART mode)**

**($T_A$ = –40 to +105°C, 2.4 V ≤ $EV_{DD}$ = $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | Unit |
|---|---|---|---|---|---|
| | | | MIN. | MAX. | |
| Transfer rate Note 1 | | | | $f_{MCK}$/12 | bps |
| | | Theoretical value of the maximum transfer rate $f_{MCK}$ = $f_{CLK}$ Note 2 | | 2.0 | Mbps |

**Notes 1.** Transfer rate in the SNOOZE mode is 4800 bps only.

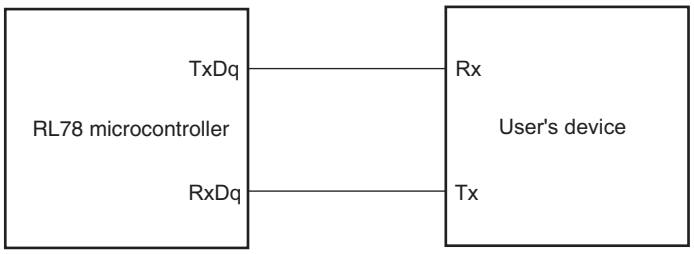
**2.** The maximum operating frequencies of the CPU/peripheral hardware clock ($f_{CLK}$) are:

HS (high-speed main) mode: 24 MHz (2.7 V ≤ $V_{DD}$ ≤ 5.5 V)

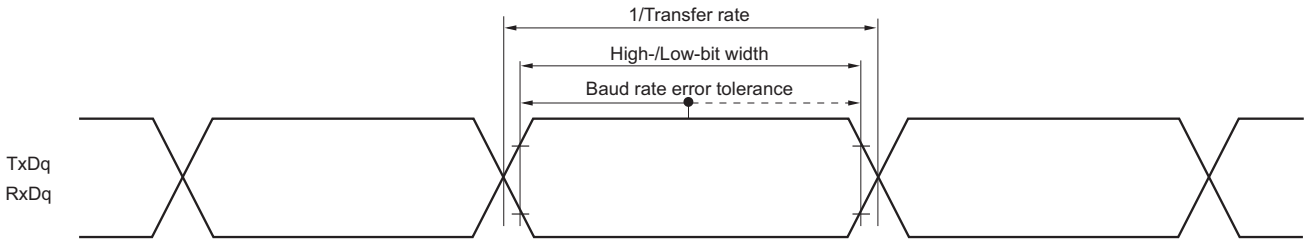
16 MHz (2.4 V ≤ $V_{DD}$ ≤ 5.5 V)

**Caution Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).**

**UART mode connection diagram (during communication at same potential)**




**UART mode bit width (during communication at same potential) (reference)**




**Remarks 1.** q: UART number (q = 0), g: PIM and POM number (g = 1)

**2.** $f_{MCK}$: Serial array unit operation clock frequency

(Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 01))

**(2) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output)**

**($T_A$ = –40 to +105°C, 2.4 V ≤ $EV_{DD}$ = $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | | HS (high-speed main) Mode | | Unit |
|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | |
| SCKp cycle time | $t_{KCY1}$ | 2.7 V ≤ $EV_{DD}$ ≤ 5.5 V | | 334 Note 1 | | ns |
| | | 2.4 V ≤ $EV_{DD}$ ≤ 5.5 V | | 500 Note 1 | | ns |
| SCKp high-/low-level width | $t_{KH1}$, $t_{KL1}$ | 4.0 V ≤ $EV_{DD}$ ≤ 5.5 V | | $t_{KCY1}$/2 – 24 | | ns |
| | | 2.7 V ≤ $EV_{DD}$ ≤ 5.5 V | | $t_{KCY1}$/2 – 36 | | ns |
| | | 2.4 V ≤ $EV_{DD}$ ≤ 5.5 V | | $t_{KCY1}$/2 – 76 | | ns |
| SIp setup time (to SCKp↑) Note 2 | $t_{SIK1}$ | 2.7 V ≤ $EV_{DD}$ ≤ 5.5 V | | 66 | | ns |
| | | 2.4 V ≤ $EV_{DD}$ ≤ 5.5 V | | 113 | | ns |
| SIp hold time (from SCKp↑) Note 3 | $t_{KSI1}$ | 2.4 V ≤ $EV_{DD}$ ≤ 5.5 V | | 38 | | ns |
| Delay time from SCKp↓ to SOp output Note 4 | $t_{KSO1}$ | C = 30 pF Note 5 | 2.4 V ≤ $EV_{DD}$ ≤ 5.5 V | | 50 | ns |

**Notes 1.** Set a cycle of 4/$f_{MCK}$ or longer.

**2.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**3.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**4.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**5.** C is the load capacitance of the SCKp and SOp output lines.

**Caution Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).**

**Remarks 1.** p: CSI number (p = 00, 01), m: Unit number (m = 0), n: Channel number (n = 0, 1), g: PIM and POM numbers (g = 1)

**2.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 01))

**(4) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (2/2)**

**($T_A$ = –40 to +105°C, 2.4 V ≤ $EV_{DD}$ = $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | | | HS (high-speed main) Mode | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | MIN. | MAX. | |
| Transfer rate | | Transmission | 4.0 V ≤ $EV_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V | | | **Note 1** | bps |
| | | | | Theoretical value of the maximum transfer rate $C_b$ = 50 pF, $R_b$ = 1.4 kΩ, $V_b$ = 2.7 V | | 2.0 Note 2 | Mbps |
| | | | 2.7 V ≤ $EV_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V | | | **Note 3** | bps |
| | | | | Theoretical value of the maximum transfer rate $C_b$ = 50 pF, $R_b$ = 2.7 kΩ, $V_b$ = 2.3 V | | 1.2 Note 4 | Mbps |
| | | | 2.4 V ≤ $EV_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V | | | **Note 5** | bps |
| | | | | Theoretical value of the maximum transfer rate $C_b$ = 50 pF, $R_b$ = 5.5 kΩ, $V_b$ = 1.6 V | | 0.43 Note 6 | Mbps |

**Notes 1.** The smaller maximum transfer rate derived by using $f_{MCK}$/6 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 4.0 V ≤ $EV_{DD}$ ≤ 5.5 V and 2.7 V ≤ $V_b$ ≤ 4.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

**2.** This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to Note 1 above to calculate the maximum transfer rate under conditions of the customer.

**3.** The smaller maximum transfer rate derived by using $f_{MCK}$/6 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 2.7 V ≤ $EV_{DD}$ < 4.0 V and 2.3 V ≤ $V_b$ ≤ 2.7 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

**4.** This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to Note 3 above to calculate the maximum transfer rate under conditions of the customer.

**(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (slave mode, SCKp... external clock input)**
**($T_A$ = –40 to +105°C, 2.4 V ≤ $EV_{DD}$ = $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | | HS (high-speed main) Mode | | Unit |
|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | |
| SCKp cycle time Note 1 | $t_{KCY2}$ | 4.0 V ≤ $EV_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V | 20 MHz < $f_{MCK}$ ≤ 24 MHz | 24/$f_{MCK}$ | | ns |
| | | | 8 MHz < $f_{MCK}$ ≤ 20 MHz | 20/$f_{MCK}$ | | ns |
| | | | 4 MHz < $f_{MCK}$ ≤ 8 MHz | 16/$f_{MCK}$ | | ns |
| | | | $f_{MCK}$ ≤ 4 MHz | 12/$f_{MCK}$ | | ns |
| | | 2.7 V ≤ $EV_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V | 20 MHz < $f_{MCK}$ ≤ 24 MHz | 32/$f_{MCK}$ | | ns |
| | | | 16 MHz < $f_{MCK}$ ≤ 20 MHz | 28/$f_{MCK}$ | | ns |
| | | | 8 MHz < $f_{MCK}$ ≤ 16 MHz | 24/$f_{MCK}$ | | ns |
| | | | 4 MHz < $f_{MCK}$ ≤ 8 MHz | 16/$f_{MCK}$ | | ns |
| | | | $f_{MCK}$ ≤ 4 MHz | 12/$f_{MCK}$ | | ns |
| | | 2.4 V ≤ $EV_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V | 20 MHz < $f_{MCK}$ ≤ 24 MHz | 72/$f_{MCK}$ | | ns |
| | | | 16 MHz < $f_{MCK}$ ≤ 20 MHz | 64/$f_{MCK}$ | | ns |
| | | | 8 MHz < $f_{MCK}$ ≤ 16 MHz | 52/$f_{MCK}$ | | ns |
| | | | 4 MHz < $f_{MCK}$ ≤ 8 MHz | 32/$f_{MCK}$ | | ns |
| | | | $f_{MCK}$ ≤ 4 MHz | 20/$f_{MCK}$ | | ns |
| SCKp high-/low-level width | $t_{KH2}$, $t_{KL2}$ | 4.0 V ≤ $EV_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V | | $t_{KCY2}$/2 – 24 | | ns |
| | | 2.7 V ≤ $EV_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V | | $t_{KCY2}$/2 – 36 | | ns |
| | | 2.4 V ≤ $EV_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V | | $t_{KCY2}$/2 – 100 | | ns |
| SIp setup time (to SCKp↑) Note2 | $t_{SIK2}$ | 4.0 V ≤ $EV_{DD}$ < 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V | | 1/$f_{MCK}$ + 40 | | ns |
| | | 2.7 V ≤ $EV_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V | | 1/$f_{MCK}$ + 40 | | ns |
| | | 2.4 V ≤ $EV_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V | | 1/$f_{MCK}$ + 60 | | ns |
| SIp hold time (from SCKp↑) Note 3 | $t_{KSI2}$ | 4.0 V ≤ $EV_{DD}$ < 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V | | 1/$f_{MCK}$ + 62 | | ns |
| | | 2.7 V ≤ $EV_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V | | 1/$f_{MCK}$ + 62 | | ns |
| | | 2.4 V ≤ $EV_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V | | 1/$f_{MCK}$ + 62 | | ns |
| Delay time from SCKp↓ to SOp output Note 4 | $t_{KSO2}$ | 4.0 V ≤ $EV_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | | | 2/$f_{MCK}$ + 240 | ns |
| | | 2.7 V ≤ $EV_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | | | 2/$f_{MCK}$ + 428 | ns |
| | | 2.4 V ≤ $EV_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | | | 2/$f_{MCK}$ + 1146 | ns |

(**Notes**, **Caution** and **Remarks** are listed on the page after the next page.)

## 3.6.2 Temperature sensor/internal reference voltage characteristics

**($T_A$ = –40 to +105°C, 2.4 V ≤ $EV_{DD}$ = $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS}$ = 0 V, HS (high-speed main) mode)**

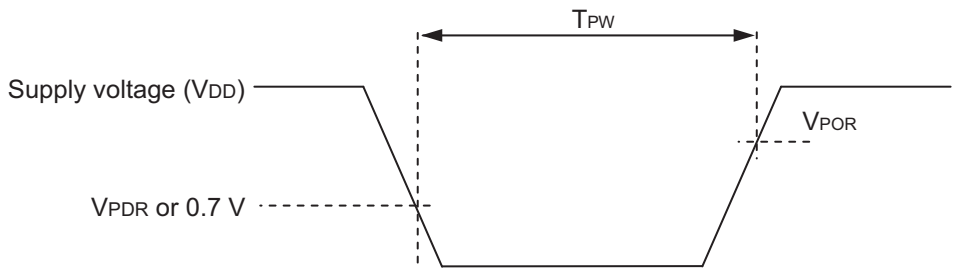
| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Temperature sensor output voltage | $V_{TMPS25}$ | Setting ADS register = 80H, $T_A$ = +25°C | | 1.05 | | V |
| Internal reference voltage | $V_{BGR}$ | Setting ADS register = 81H | 1.38 | 1.45 | 1.5 | V |
| Temperature coefficient | $F_{VTMPS}$ | Temperature sensor that depends on the temperature | | –3.6 | | mV/°C |
| Operation stabilization wait time | $t_{AMP}$ | | 5 | | | μs |

## 3.6.3 POR circuit characteristics

**($T_A$ = –40 to +105°C, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Detection voltage | $V_{POR}$ | Power supply rise time | 1.45 | 1.51 | 1.57 | V |
| | $V_{PDR}$ | Power supply fall time | 1.44 | 1.50 | 1.56 | V |
| Minimum pulse width | $T_{PW}$ | | 300 | | | μs |

**Note** Minimum time required for a POR reset when $V_{DD}$ exceeds below $V_{PDR}$. This is also the minimum time required for a POR reset from when $V_{DD}$ exceeds below 0.7 V to when $V_{DD}$ exceeds $V_{POR}$ while STOP mode is entered or the main system clock is stopped through setting bit 0 (HIOSTOP) and bit 7 (MSTOP) in the clock operation status control register (CSC).



**(2) 1/4 bias method**

**($T_A$ = –40 to +105°C, 2.4 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| LCD output voltage variation range | $V_{L1}$ Note 4 | C1 to C5 Note 1 = 0.47 μF | VLCD = 04H | 0.90 | 1.00 | 1.08 | V |
| | | | VLCD = 05H | 0.95 | 1.05 | 1.13 | V |
| | | | VLCD = 06H | 1.00 | 1.10 | 1.18 | V |
| | | | VLCD = 07H | 1.05 | 1.15 | 1.23 | V |
| | | | VLCD = 08H | 1.10 | 1.20 | 1.28 | V |
| | | | VLCD = 09H | 1.15 | 1.25 | 1.33 | V |
| | | | VLCD = 0AH | 1.20 | 1.30 | 1.38 | V |
| | | | VLCD = 0BH | 1.25 | 1.35 | 1.43 | V |
| | | | VLCD = 0CH | 1.30 | 1.40 | 1.48 | V |
| | | | VLCD = 0DH | 1.35 | 1.45 | 1.53 | V |
| | | | VLCD = 0EH | 1.40 | 1.50 | 1.58 | V |
| | | | VLCD = 0FH | 1.45 | 1.55 | 1.63 | V |
| | | | VLCD = 10H | 1.50 | 1.60 | 1.68 | V |
| | | | VLCD = 11H | 1.55 | 1.65 | 1.73 | V |
| | | | VLCD = 12H | 1.60 | 1.70 | 1.78 | V |
| | | | VLCD = 13H | 1.65 | 1.75 | 1.83 | V |
| Doubler output voltage | $V_{L2}$ | C1 to C5 Note 1 = 0.47 μF | | 2 $V_{L1}$ – 0.08 | 2 $V_{L1}$ | 2 $V_{L1}$ | V |
| Tripler output voltage | $V_{L3}$ | C1 to C5 Note 1 = 0.47 μF | | 3 $V_{L1}$ – 0.12 | 3 $V_{L1}$ | 3 $V_{L1}$ | V |
| Quadruply output voltage | $V_{L4}$ Note 4 | C1 to C5 Note 1 = 0.47 μF | | 4 $V_{L1}$ – 0.16 | 4 $V_{L1}$ | 4 $V_{L1}$ | V |
| Reference voltage setup time Note 2 | $t_{VWAIT1}$ | | | 5 | | | ms |
| Voltage boost wait time Note 3 | $t_{VWAIT2}$ | C1 to C5 Note 1 = 0.47 μF | | 500 | | | ms |

**Notes 1.** This is a capacitor that is connected between voltage pins used to drive the LCD.
C1: A capacitor connected between CAPH and CAPL
C2: A capacitor connected between $V_{L1}$ and GND
C3: A capacitor connected between $V_{L2}$ and GND
C4: A capacitor connected between $V_{L3}$ and GND
C5: A capacitor connected between $V_{L4}$ and GND
C1 = C2 = C3 = C4 = C5 = 0.47 μF±30%

**2.** This is the time required to wait from when the reference voltage is specified by using the VLCD register (or when the internal voltage boosting method is selected [by setting the MDSET1 and MDSET0 bits of the LCDM0 register to 01B] if the default value reference voltage is used) until voltage boosting starts (VLCON = 1).

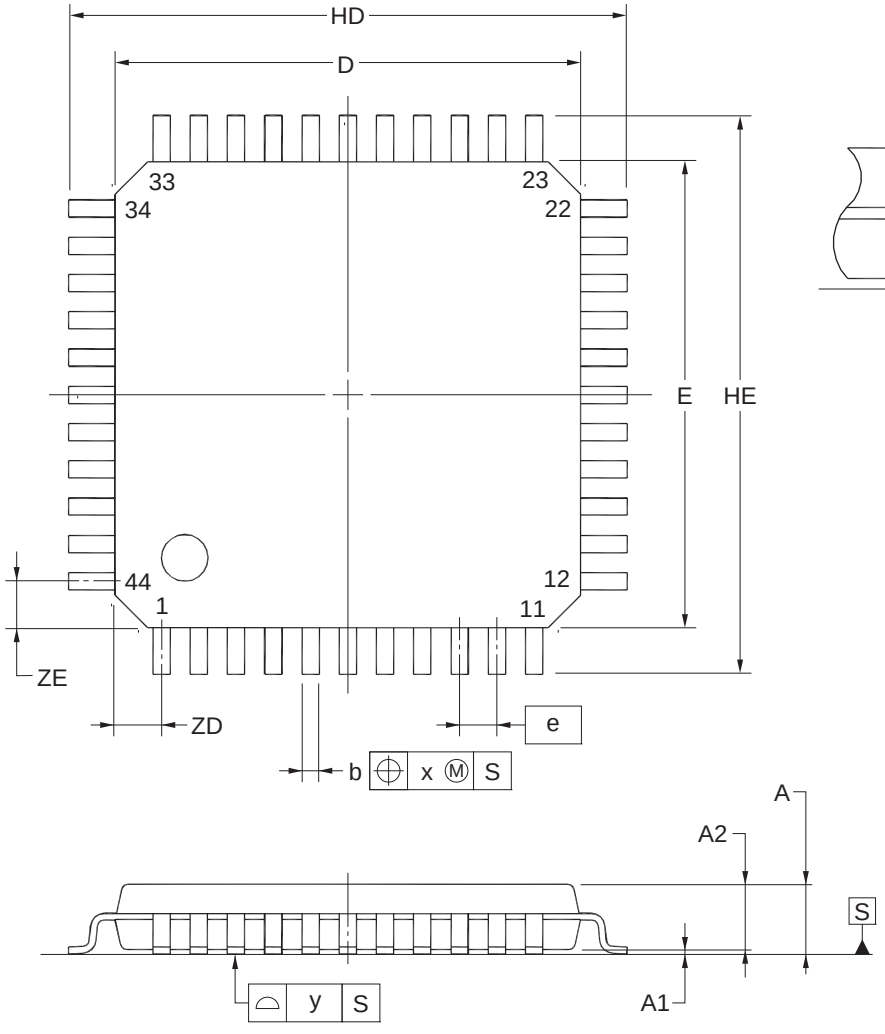
**3.** This is the wait time from when voltage boosting is started (VLCON = 1) until display is enabled (LCDON = 1).

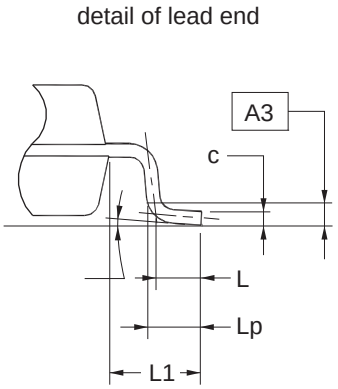
**4.** $V_{L4}$ must be 5.5 V or lower.

## 4.2 44-pin Products

R5F10RF8AFP, R5F10RFAAFP, R5F10RFCAFP
R5F10RF8GFP, R5F10RFAGFP, R5F10RFCGFP

| JEITA Package Code | RENESAS Code | Previous Code | MASS (TYP.) [g] |
|---|---|---|---|
| P-LQFP44-10x10-0.80 | PLQP0044GC-A | P44GB-80-UES-2 | 0.36 |




(UNIT:mm)

| ITEM | DIMENSIONS |
|---|---|
| D | 10.00±0.20 |
| E | 10.00±0.20 |
| HD | 12.00±0.20 |
| HE | 12.00±0.20 |
| A | 1.60 MAX. |
| A1 | 0.10±0.05 |
| A2 | 1.40±0.05 |
| A3 | 0.25 |
| b | $0.37^{+0.08}_{0.07}$ |
| c | $0.145^{+0.055}_{0.045}$ |
| L | 0.50 |
| Lp | 0.60±0.15 |
| L1 | 1.00±0.20 |
| | $3^{\circ}{}^{+5^{\circ}}_{3^{\circ}}$ |
| e | 0.80 |
| x | 0.20 |
| y | 0.10 |
| ZD | 1.00 |
| ZE | 1.00 |

**NOTE**
Each lead centerline is located within 0.20 mm of its true position at maximum material condition.

The mark "<R>" shows major revised points. The revised points can be easily searched by copying an "<R>" in the PDF file and specifying it in the "Find what:" field.



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