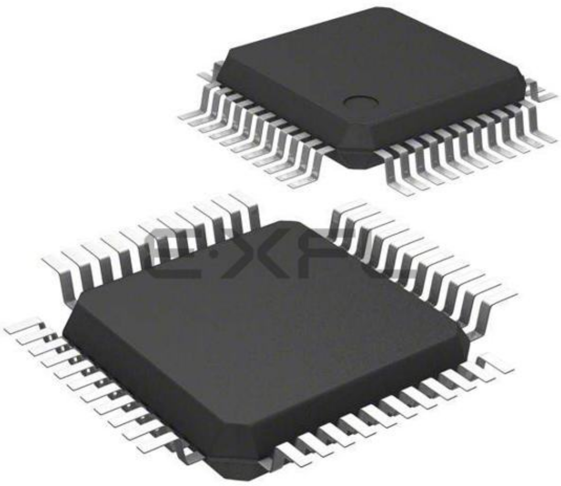

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

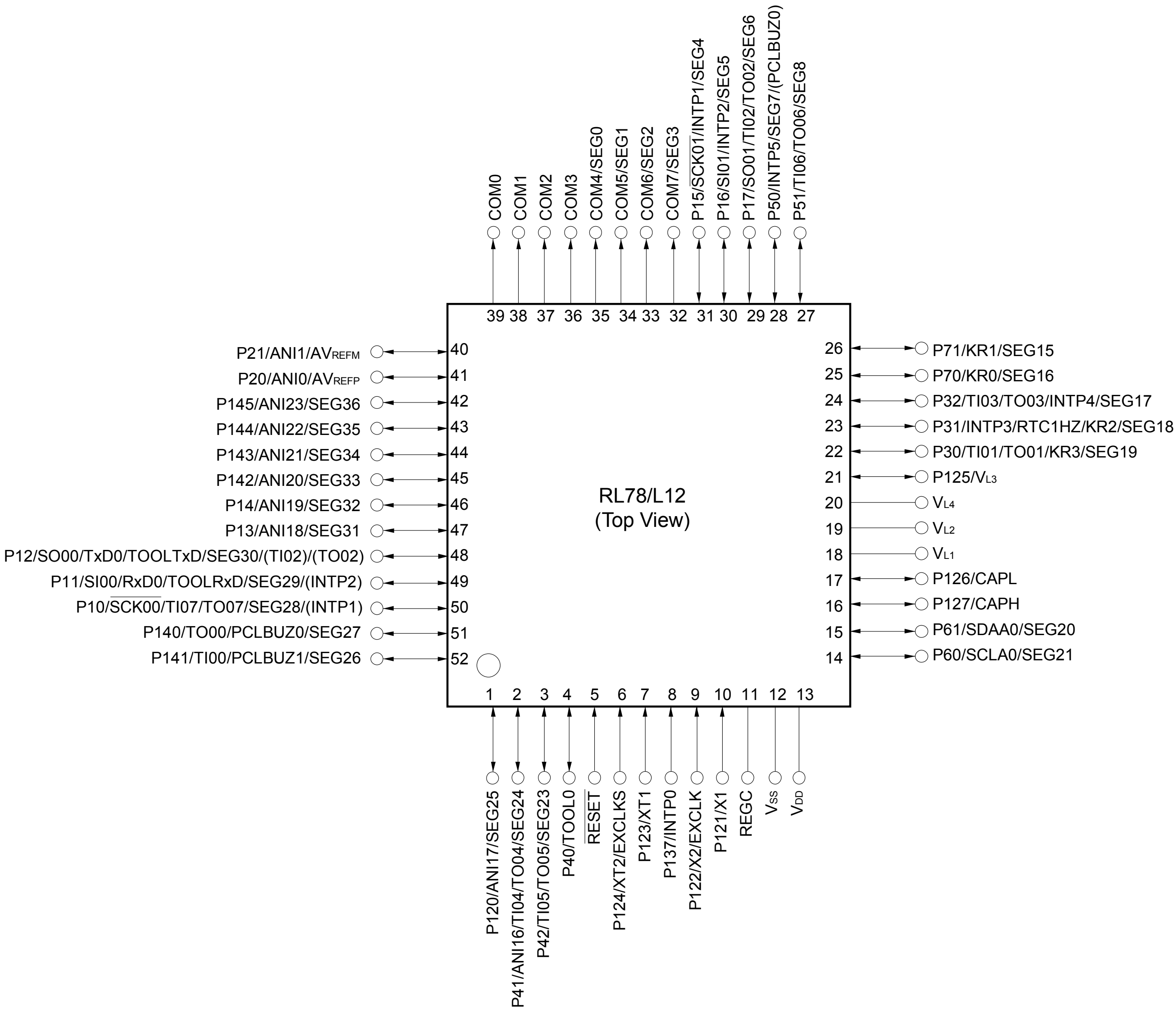
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	RL78
Core Size	16-Bit
Speed	24MHz
Connectivity	CSI, I²C, LINbus, UART/USART
Peripherals	DMA, LCD, LVD, POR, PWM, WDT
Number of I/O	29
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	1.5K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 7x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LQFP
Supplier Device Package	44-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f10rfcgfp-v0

1.3.4 52-pin products

- 52-pin plastic LQFP (10 × 10)

<R>



Caution Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).

Remarks 1. For pin identification, see **1.4 Pin Identification**.

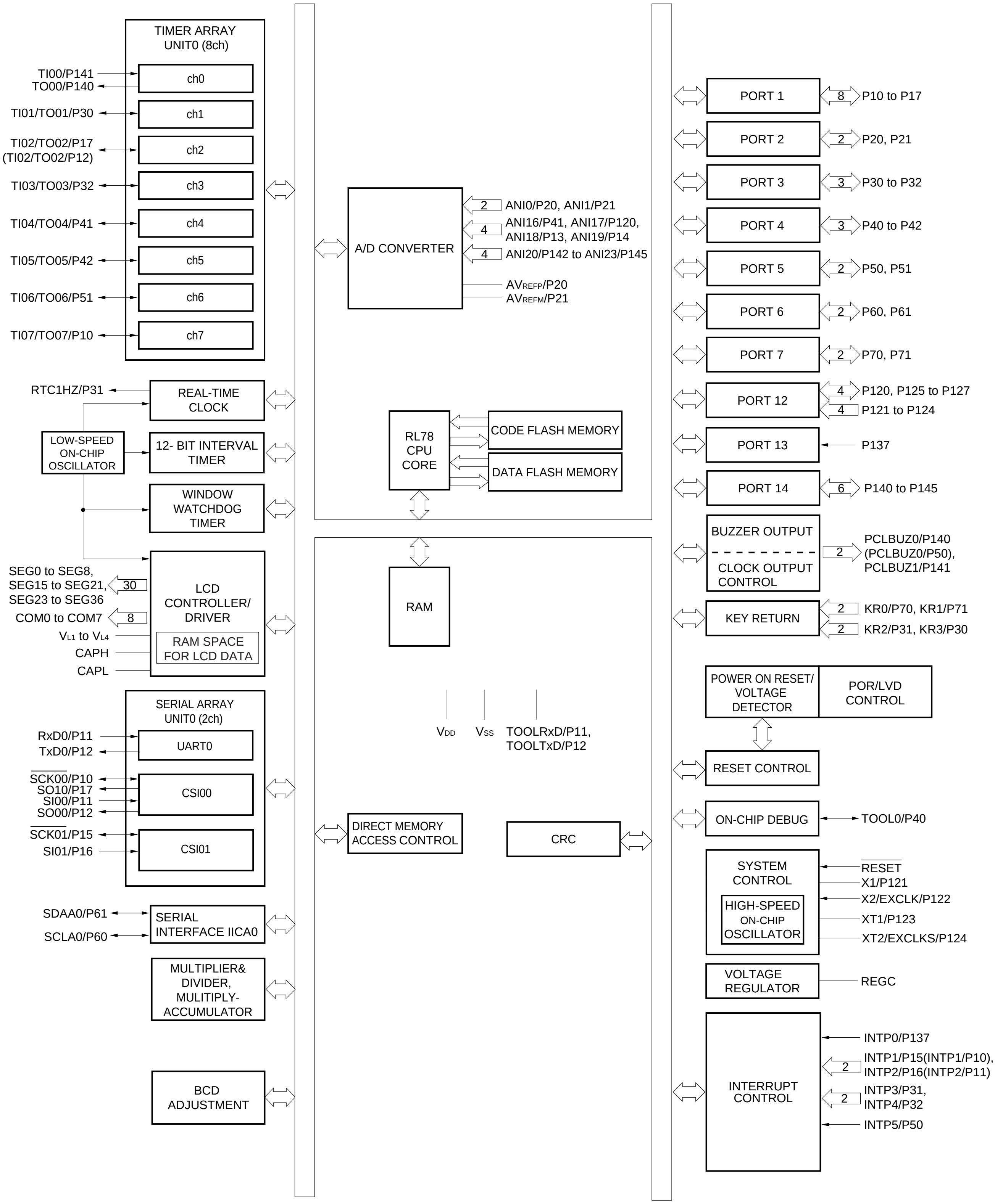
2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

1.4 Pin Identification

ANI0, ANI1, ANI16 to ANI23:	Analog Input
AV_{REFM}:	Analog Reference Voltage Minus
AV_{REFP}:	Analog Reference Voltage Plus
CAPH, CAPL:	Capacitor for LCD
COM0 to COM7,	
EV_{DD}:	Power Supply for Port
EV_{SS}:	Ground for Port
EXCLK:	External Clock Input (Main System Clock)
EXCLKS:	External Clock Input (Subsystem Clock)
INTP0 to INTP7:	Interrupt Request From Peripheral
KR0 to KR3:	Key Return
P10 to P17:	Port 1
P20, P21:	Port 2
P30 to P32:	Port 3
P40 to P43:	Port 4
P50 to P54:	Port 5
P60, P61:	Port 6
P70 to P74:	Port 7
P120 to P127:	Port 12

P130, P137:	Port 13
P140 to P147:	Port 14
PCLBUZ0, PCLBUZ1:	Programmable Clock Output/Buzzer Output
REGC:	Regulator Capacitance
$\overline{\text{RESET}}$:	Reset
RTC1HZ:	Real-time Clock Correction Clock (1 Hz) Output
RxD0:	Receive Data
$\overline{\text{SCK00}}$, $\overline{\text{SCK01}}$:	Serial Clock Input/Output
SCLA0:	Serial Clock Input/Output
SDAA0:	Serial Data Input/Output
SEG0 to SEG38:	LCD Segment Output
SI00, SI01:	Serial Data Input
SO00, SO01:	Serial Data Output
TI00 to TI07:	Timer Input
TO00 to TO07:	Timer Output
TOOL0:	Data Input/Output for Tool
TOOLRxD, TOOLTxD:	Data Input/Output for External Device
TxD0:	Transmit Data
V_{DD}:	Power Supply
V_{L1} to V_{L4}:	LCD Power Supply
V_{SS}:	Ground
X1, X2:	Crystal Oscillator (Main System Clock)
XT1, XT2:	Crystal Oscillator (Subsystem Clock)

1.5.4 52-pin products



Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR)

Absolute Maximum Ratings (T_A = 25°C) **(2/3)**

Parameter	Symbols	Conditions		Ratings	Unit
LCD voltage	V_{L1}	V_{L1} voltage Note 1		–0.3 to +2.8 and –0.3 to V_{L4} + 0.3	V
	V_{L2}	V_{L2} voltage Note 1		–0.3 to V_{L4} + 0.3 Note 2	V
	V_{L3}	V_{L3} voltage Note 1		–0.3 to V_{L4} + 0.3 Note 2	V
	V_{L4}	V_{L4} voltage Note 1		–0.3 to +6.5	V
	V_{LCAP}	CAPL, CAPH voltage Note 1		–0.3 to V_{L4} + 0.3 Note 2	V
	V_{LOUT}	COM0 to COM7, SEG0 to SEG38, output voltage	External resistance division method	–0.3 to V_{DD} + 0.3 Note 2	V
			Capacitor split method	–0.3 to V_{DD} + 0.3 Note 2	
			Internal voltage boosting method	–0.3 to V_{L4} + 0.3 Note 2	

Notes 1. This value only indicates the absolute maximum ratings when applying voltage to the V_{L1}, V_{L2}, V_{L3}, and V_{L4} pins; it does not mean that applying voltage to these pins is recommended. When using the internal voltage boosting method or capacitance split method, connect these pins to V_{SS} via a capacitor (0.47 μF ± 30%) and connect a capacitor (0.47 μF ± 30%) between the CAPL and CAPH pins.

2. Must be 6.5 V or lower.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark V_{SS} : Reference voltage

2.3 DC Characteristics

2.3.1 Pin characteristics

(T_A = –40 to +85°C, 1.6 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V) (1/5)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, high[Note 1]	I_{OH1}	Per pin for P10 to P17, P30 to P32, P40 to P43, P50 to P54, P70 to P74, P120, P125 to P127, P130, P140 to P147				–10.0 Note 2	mA
		Total of P10 to P14, P40 to P43, P120, P130, P140 to P147 (When duty = 70% [Note 3])	4.0 V ≤ EV_{DD} ≤ 5.5 V			–40.0	mA
			2.7 V ≤ EV_{DD} < 4.0 V			–8.0	mA
			1.8 V ≤ EV_{DD} < 2.7 V			–4.0	mA
			1.6 V ≤ EV_{DD} < 1.8 V			–2.0	mA
		Total of P15 to P17, P30 to P32, P50 to P54, P70 to P74, P125 to P127 (When duty = 70% [Note 3])	4.0 V ≤ EV_{DD} ≤ 5.5 V			–60.0	mA
			2.7 V ≤ EV_{DD} < 4.0 V			–15.0	mA
			1.8 V ≤ EV_{DD} < 2.7 V			–8.0	mA
			1.6 V ≤ EV_{DD} < 1.8 V			–4.0	mA
		Total of all pins (When duty = 70%[Note 3])				–100.0	mA
	I_{OH2}	P20, P21	Per pin			–0.1	mA
			Total of all pins 1.6 V ≤ V_{DD} ≤ 5.5 V			–0.2	mA

Notes 1. Value of current at which the device operation is guaranteed even if the current flows from the V_{DD} and EV_{DD} pins to an output pin.

2. Do not exceed the total current value.

3. Specification under conditions where the duty factor ≤ 70%.

The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (I_{OH} × 0.7)/(n × 0.01)

<Example> Where n = 80% and I_{OH} = –40.0 mA

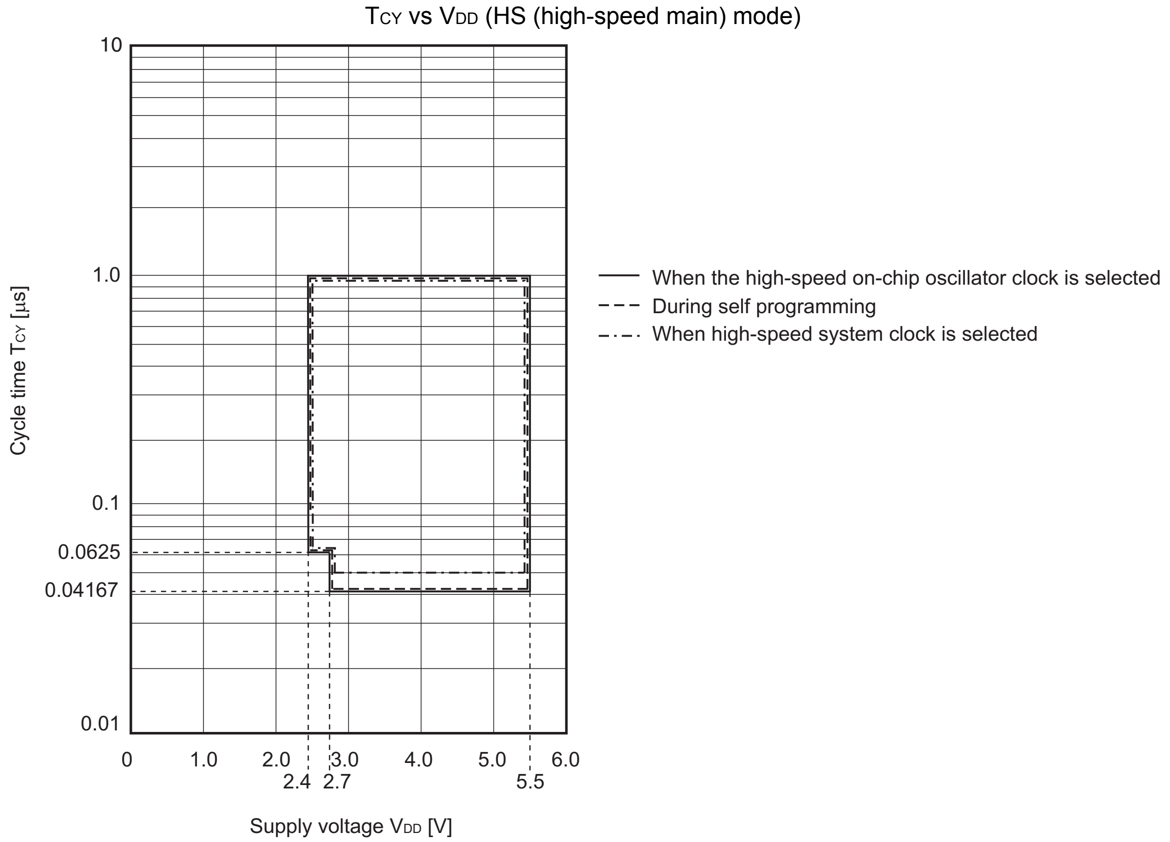
Total output current of pins = (–40.0 × 0.7)/(80 × 0.01) ≅ –35.0 mA

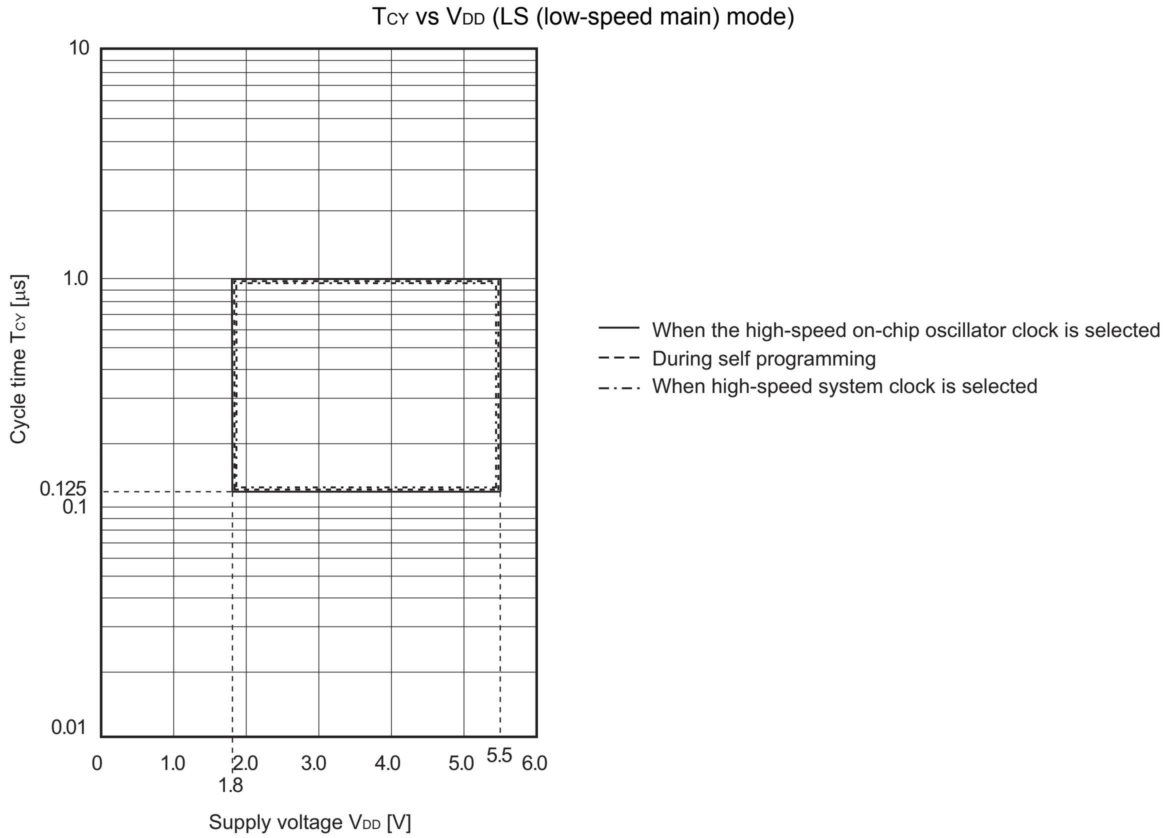
However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

Caution P10, P12, P15, and P17 do not output high level in N-ch open-drain mode.

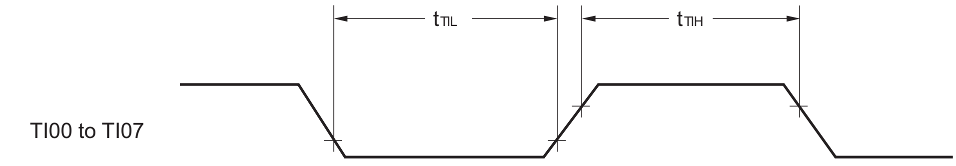
Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

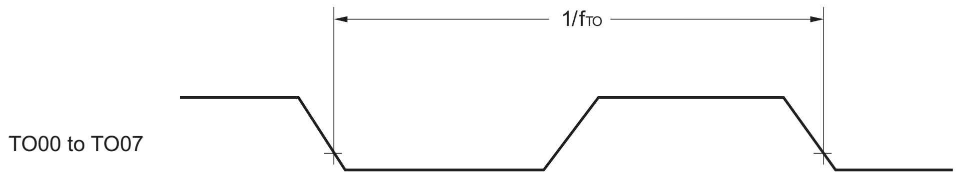
Minimum Instruction Execution Time during Main System Clock Operation



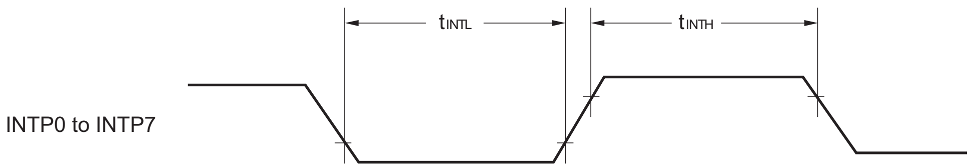


TI/TO Timing

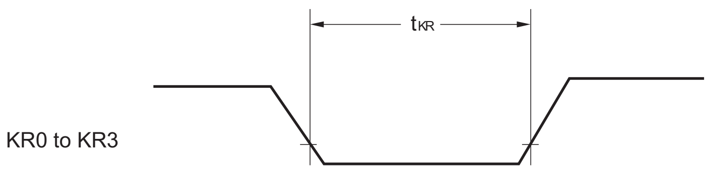




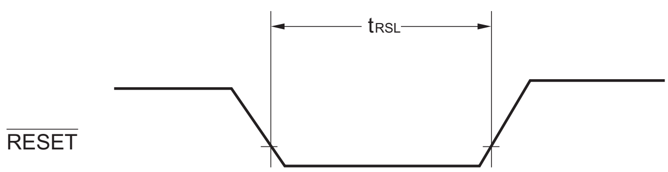
Interrupt Request Input Timing



Key Interrupt Input Timing



$\overline{\text{RESET}}$ Input Timing



(2) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output)
(T_A = –40 to +85°C, 1.6 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode MIN.	HS (high-speed main) Mode MAX.	LS (low-speed main) Mode MIN.	LS (low-speed main) Mode MAX.	LV (low-voltage main) Mode MIN.	LV (low-voltage main) Mode MAX.	Unit
SCKp cycle time	t_{KCY1}	2.7 V ≤ EV_{DD} ≤ 5.5 V	167 Note 1		500 Note 1		1000 Note 1		ns
		2.4 V ≤ EV_{DD} ≤ 5.5 V	250 Note 1		500 Note 1		1000 Note 1		ns
		1.8 V ≤ EV_{DD} ≤ 5.5 V			500 Note 1		1000 Note 1		ns
		1.6 V ≤ EV_{DD} ≤ 5.5 V					1000 Note 1		ns
SCKp high-/low-level width	t_{KH1}, t_{KL1}	4.0 V ≤ EV_{DD} ≤ 5.5 V	$t_{KCY1}/2 - 12$		$t_{KCY1}/2 - 50$		$t_{KCY1}/2 - 50$		ns
		2.7 V ≤ EV_{DD} ≤ 5.5 V	$t_{KCY1}/2 - 18$		$t_{KCY1}/2 - 50$		$t_{KCY1}/2 - 50$		ns
		2.4 V ≤ EV_{DD} ≤ 5.5 V	$t_{KCY1}/2 - 38$		$t_{KCY1}/2 - 50$		$t_{KCY1}/2 - 50$		ns
		1.8 V ≤ EV_{DD} ≤ 5.5 V			$t_{KCY1}/2 - 50$		$t_{KCY1}/2 - 50$		ns
		1.6 V ≤ EV_{DD} ≤ 5.5 V					$t_{KCY1}/2 - 100$		ns
SIp setup time (to SCKp↑) Note 2	t_{SIK1}	2.7 V ≤ EV_{DD} ≤ 5.5 V	44		110		110		ns
		2.4 V ≤ EV_{DD} ≤ 5.5 V	75		110		110		ns
		1.8 V ≤ EV_{DD} ≤ 5.5 V			110		110		ns
		1.6 V ≤ EV_{DD} ≤ 5.5 V					220		ns
SIp hold time (from SCKp↑) Note 3	t_{KSI1}	2.4 V ≤ EV_{DD} ≤ 5.5 V	19		19		19		ns
		1.8 V ≤ EV_{DD} ≤ 5.5 V			19		19		
		1.6 V ≤ EV_{DD} ≤ 5.5 V					19		
Delay time from SCKp↓ to SOp output Note 4	t_{KSO1}	C = 30 pF Note 5, 2.4 V ≤ EV_{DD} ≤ 5.5 V		25		25		25	ns
		C = 30 pF Note 5, 1.8 V ≤ EV_{DD} ≤ 5.5 V				25		25	
		C = 30 pF Note 5, 1.6 V ≤ EV_{DD} ≤ 5.5 V						25	

Notes
1. For CSI00, set a cycle of 2/f_{MCK} or longer. For CSI01, set a cycle of 4/f_{MCK} or longer.
2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
4. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
5. C is the load capacitance of the SCKp and SOp output lines.

Caution **Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).**

(**Remarks** are listed on the next page.)

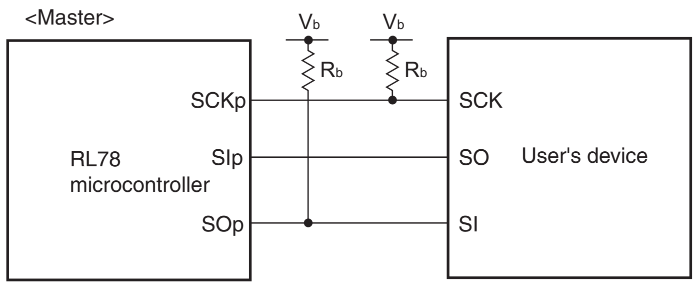
(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output) (2/3)
(T_A = –40 to +85°C, 1.8 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SIp setup time (to SCKp↑) Note 1	t_{SIK1}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	81		479		479		ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	177		479		479		ns
		2.4 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ	479		479		479		ns
		1.8 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 3, C_b = 30 pF, R_b = 5.5 kΩ			479		479		ns
SIp hold time (from SCKp↑) Note 1	t_{KSI1}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	19		19		19		ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	19		19		19		ns
		2.4 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ	19		19		19		ns
		1.8 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 3, C_b = 30 pF, R_b = 5.5 kΩ			19		19		ns
Delay time from SCKp↓ to SOp output Note 1	t_{KSO1}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		100		100		100	ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		195		195		195	ns
		2.4 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		483		483		483	ns
		1.8 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 3, C_b = 30 pF, R_b = 5.5 kΩ				483		483	ns
SIp setup time (to SCKp↓) Note 2	t_{SIK1}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	44		110		110		ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	44		110		110		ns
		2.4 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	110		110		110		ns
		1.8 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 3, C_b = 30 pF, R_b = 5.5 kΩ			110		110		ns

Notes
1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.
2. When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
3. Use it with EV_{DD} ≥ V_b.

Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance (32-pin to 52-pin products)/EV_{DD} tolerance (64-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

CSI mode connection diagram (during communication at different potential)



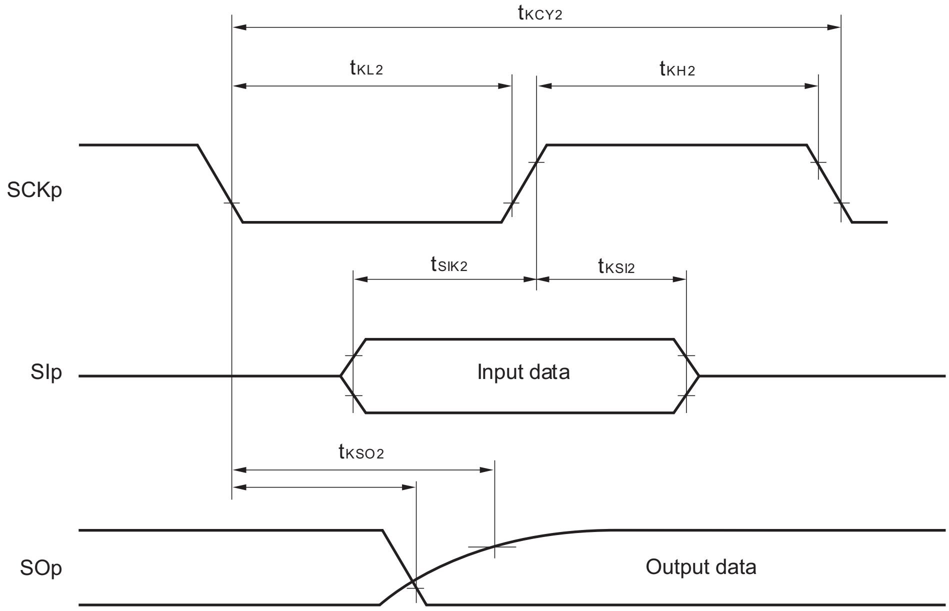
Remarks 1. R_b[Ω]:Communication line (SCKp, SOp) pull-up resistance, C_b[F]: Communication line (SCKp, SOp) load capacitance, V_b[V]: Communication line voltage

2. p: CSI number (p = 00, 01), m: Unit number (m = 0), n: Channel number (n = 0, 1), g: PIM and POM number (g = 1)

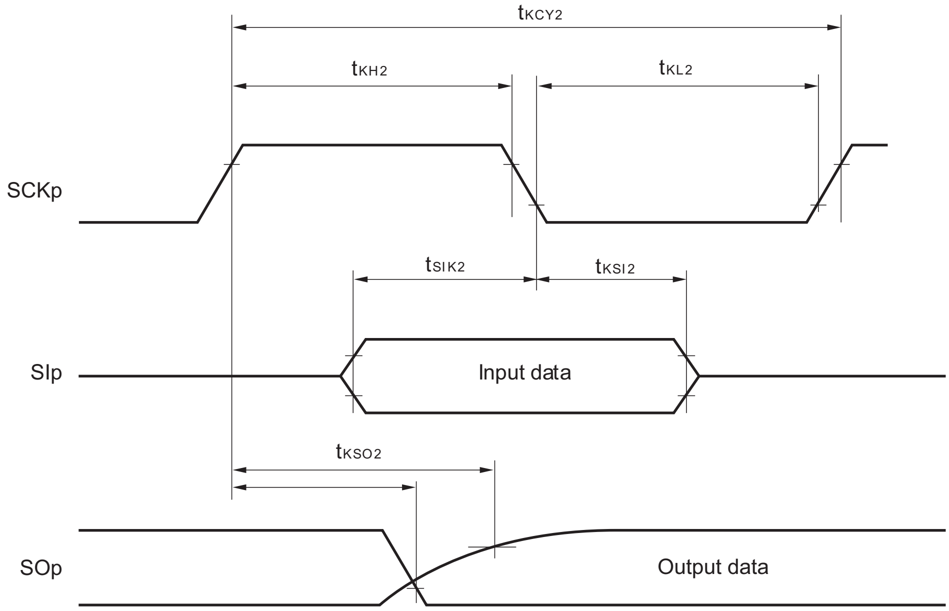
3. f_{MCK}: Serial array unit operation clock frequency

(Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 01)

CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remark p: CSI number (p = 00, 01), m: Unit number (m = 0), n: Channel number (n = 0, 1),
g: PIM and POM number (g = 1)

Notes 1. The first clock pulse is generated after this period when the start/restart condition is detected.

2. The maximum value (MAX.) of $t_{HD:DAT}$ is during normal transfer and a wait state is inserted in the $\overline{ACK}$ (acknowledge) timing.

Remark The maximum value of Cb (communication line capacitance) and the value of Rb (communication line pull-up resistor) at that time in each mode are as follows.

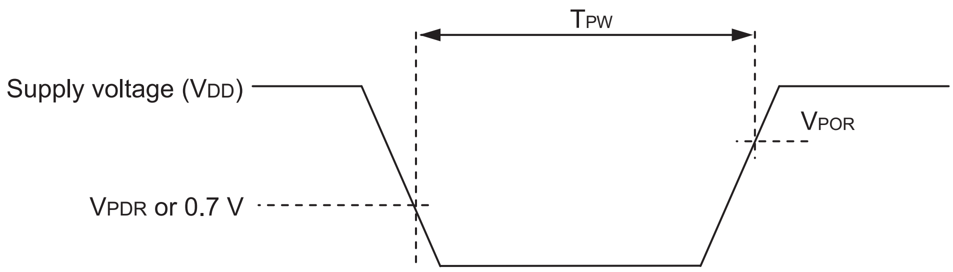
Standard mode: C_b = 400 pF, R_b = 2.7 kΩ

2.6.3 POR circuit characteristics

(T_A = –40 to +85°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V_{POR}	Power supply rise time	1.47	1.51	1.55	V
	V_{PDR}	Power supply fall time	1.46	1.50	1.54	V
Minimum pulse width[Note]	T_{PW}		300			μs

Note Minimum time required for a POR reset when V_{DD} exceeds below V_{PDR}. This is also the minimum time required for a POR reset from when V_{DD} exceeds below 0.7 V to when V_{DD} exceeds V_{POR} while STOP mode is entered or the main system clock is stopped through setting bit 0 (HIOSTOP) and bit 7 (MSTOP) in the clock operation status control register (CSC).



(2) 1/4 bias method

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
LCD output voltage variation range	V_{L1} Note 4	C1 to C5 Note 1 = 0.47 μF	VLCD = 04H	0.90	1.00	1.08	V
			VLCD = 05H	0.95	1.05	1.13	V
			VLCD = 06H	1.00	1.10	1.18	V
			VLCD = 07H	1.05	1.15	1.23	V
			VLCD = 08H	1.10	1.20	1.28	V
			VLCD = 09H	1.15	1.25	1.33	V
			VLCD = 0AH	1.20	1.30	1.38	V
			VLCD = 0BH	1.25	1.35	1.43	V
			VLCD = 0CH	1.30	1.40	1.48	V
			VLCD = 0DH	1.35	1.45	1.53	V
			VLCD = 0EH	1.40	1.50	1.58	V
			VLCD = 0FH	1.45	1.55	1.63	V
			VLCD = 10H	1.50	1.60	1.68	V
			VLCD = 11H	1.55	1.65	1.73	V
			VLCD = 12H	1.60	1.70	1.78	V
			VLCD = 13H	1.65	1.75	1.83	V
Doubler output voltage	V_{L2}	C1 to C5 Note 1 = 0.47 μF		2 V_{L1} – 0.08	2 V_{L1}	2 V_{L1}	V
Tripler output voltage	V_{L3}	C1 to C5 Note 1 = 0.47 μF		3 V_{L1} – 0.12	3 V_{L1}	3 V_{L1}	V
Quadruply output voltage	V_{L4} Note 4	C1 to C5 Note 1 = 0.47 μF		4 V_{L1} – 0.16	4 V_{L1}	4 V_{L1}	V
Reference voltage setup time Note 2	t_{VWAIT1}			5			ms
Voltage boost wait time Note 3	t_{VWAIT2}	C1 to C5 Note 1 = 0.47 μF		500			ms

Notes 1. This is a capacitor that is connected between voltage pins used to drive the LCD.
C1: A capacitor connected between CAPH and CAPL
C2: A capacitor connected between V_{L1} and GND
C3: A capacitor connected between V_{L2} and GND
C4: A capacitor connected between V_{L3} and GND
C5: A capacitor connected between V_{L4} and GND
C1 = C2 = C3 = C4 = C5 = 0.47 μF±30%

2. This is the time required to wait from when the reference voltage is specified by using the VLCD register (or when the internal voltage boosting method is selected [by setting the MDSET1 and MDSET0 bits of the LCDM0 register to 01B] if the default value reference voltage is used) until voltage boosting starts (VLCON = 1).

3. This is the wait time from when voltage boosting is started (VLCON = 1) until display is enabled (LCDON = 1).

4. V_{L4} must be 5.5 V or lower.

2.7.3 Capacitor split method

1/3 bias method

(T_A = –40 to +85°C, 2.2 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
V_{L4} voltage	V_{L4}	C1 to C4 = 0.47 μF Note 2		V_{DD}		V
V_{L2} voltage	V_{L2}	C1 to C4 = 0.47 μF Note 2	2/3 V_{L4} – 0.1	2/3 V_{L4}	2/3 V_{L4} + 0.1	V
V_{L1} voltage	V_{L1}	C1 to C4 = 0.47 μF Note 2	1/3 V_{L4} – 0.1	1/3 V_{L4}	1/3 V_{L4} + 0.1	V
Capacitor split wait time Note 1	t_{VWAIT}		100			ms

Absolute Maximum Ratings (T_A = 25°C) **(3/3)**

Parameter	Symbols	Conditions		Ratings	Unit
Output current, high	I_{OH1}	Per pin	P10 to P17, P30 to P32, P40 to P43, P50 to P54, P70 to P74, P120, P125 to P127, P130, P140 to P147	–40	mA
		Total of all pins –170 mA	P10 to P14, P40 to P43, P120, P130, P140 to P147	–70	mA
			P15 to P17, P30 to P32, P50 to P54, P70 to P74, P125 to P127	–100	mA
	I_{OH2}	Per pin	P20, P21	–0.5	mA
		Total of all pins		–1	mA
Output current, low	I_{OL1}	Per pin	P10 to P17, P30 to P32, P40 to P43, P50 to P54, P60, P61, P70 to P74, P120, P125 to P127, P130, P140 to P147	40	mA
		Total of all pins 170 mA	P10 to P14, P40 to P43, P120, P130, P140 to P147	70	mA
			P15 to P17, P30 to P32, P50 to P54, P60, P61, P70 to P74, P125 to P127	100	mA
	I_{OL2}	Per pin	P20, P21	1	mA
		Total of all pins		2	mA
Operating ambient temperature	T_A	In normal operation mode		–40 to +105	°C
		In flash memory programming mode			
Storage temperature	T_{stg}			–65 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = –40 to +105°C, 2.4 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V) (2/3)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current Note 1	I_{DD2} Note 2	HALT mode	HS (high-speed main) mode Note 7	f_{IH} = 24 MHz Note 4	V_{DD} = 5.0 V		0.44	2.3	mA
					V_{DD} = 3.0 V		0.44	2.3	mA
				f_{IH} = 16 MHz Note 4	V_{DD} = 5.0 V		0.40	1.7	mA
					V_{DD} = 3.0 V		0.40	1.7	mA
			HS (high-speed main) mode Note 7	f_{MX} = 20 MHz Note 3, V_{DD} = 5.0 V	Square wave input		0.28	1.9	mA
					Resonator connection		0.45	2.0	mA
				f_{MX} = 20 MHz Note 3, V_{DD} = 3.0 V	Square wave input		0.28	1.9	mA
					Resonator connection		0.45	2.0	mA
				f_{MX} = 10 MHz Note 3, V_{DD} = 5.0 V	Square wave input		0.19	1.02	mA
					Resonator connection		0.26	1.10	mA
				f_{MX} = 10 MHz Note 3, V_{DD} = 3.0 V	Square wave input		0.19	1.02	mA
					Resonator connection		0.26	1.10	mA
			Subsystem clock operation	f_{SUB} = 32.768 kHz Note 5, T_A = –40°C	Square wave input		0.31	0.57	μA
					Resonator connection		0.50	0.76	μA
				f_{SUB} = 32.768 kHz Note 5, T_A = +25°C	Square wave input		0.37	0.57	μA
					Resonator connection		0.56	0.76	μA
				f_{SUB} = 32.768 kHz Note 5, T_A = +50°C	Square wave input		0.46	1.17	μA
					Resonator connection		0.65	1.36	μA
				f_{SUB} = 32.768 kHz Note 5, T_A = +70°C	Square wave input		0.57	1.97	μA
					Resonator connection		0.76	2.16	μA
				f_{SUB} = 32.768 kHz Note 5, T_A = +85°C	Square wave input		0.85	3.37	μA
					Resonator connection		1.04	3.56	μA
				f_{SUB} = 32.768 kHz Note 5, T_A = +105°C	Square wave input		3.04	15.37	μA
					Resonator connection		3.23	15.56	μA
	I_{DD3} Note 6	STOP mode Note 8	T_A = –40°C				0.17	0.50	μA
			T_A = +25°C				0.23	0.50	μA
			T_A = +50°C				0.32	1.10	μA
			T_A = +70°C				0.43	1.90	μA
			T_A = +85°C				0.71	3.30	μA
			T_A = +105°C				2.90	15.30	μA

(**Notes** and **Remarks** are listed on the next page.)

(2) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output)
(T_A = –40 to +105°C, 2.4 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		Unit
				MIN.	MAX.	
SCKp cycle time	t_{KCY1}	2.7 V ≤ EV_{DD} ≤ 5.5 V		334 Note 1		ns
		2.4 V ≤ EV_{DD} ≤ 5.5 V		500 Note 1		ns
SCKp high-/low-level width	t_{KH1}, t_{KL1}	4.0 V ≤ EV_{DD} ≤ 5.5 V		t_{KCY1}/2 – 24		ns
		2.7 V ≤ EV_{DD} ≤ 5.5 V		t_{KCY1}/2 – 36		ns
		2.4 V ≤ EV_{DD} ≤ 5.5 V		t_{KCY1}/2 – 76		ns
SIp setup time (to SCKp↑) Note 2	t_{SIK1}	2.7 V ≤ EV_{DD} ≤ 5.5 V		66		ns
		2.4 V ≤ EV_{DD} ≤ 5.5 V		113		ns
SIp hold time (from SCKp↑) Note 3	t_{KSI1}	2.4 V ≤ EV_{DD} ≤ 5.5 V		38		ns
Delay time from SCKp↓ to SOp output Note 4	t_{KSO1}	C = 30 pF Note 5	2.4 V ≤ EV_{DD} ≤ 5.5 V		50	ns

Notes 1. Set a cycle of 4/f_{MCK} or longer.

2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

4. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

5. C is the load capacitance of the SCKp and SOp output lines.

Caution Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remarks 1. p: CSI number (p = 00, 01), m: Unit number (m = 0), n: Channel number (n = 0, 1), g: PIM and POM numbers (g = 1)

2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 01))

(3) When reference voltage (+) = V_{DD} (ADREFP1 = 0, ADREFP0 = 0), reference voltage (–) = V_{SS} (ADREFM = 0), target pin : ANI0, ANI1, ANI16 to ANI23, internal reference voltage, and temperature sensor output voltage

(T_A = –40 to +105°C, 2.4 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V, Reference voltage (+) = V_{DD}, Reference voltage (–) = V_{SS})

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error[Note 1]	AINL	10-bit resolution	2.4 V ≤ V_{DD} ≤ 5.5 V		1.2	±7.0	LSB
Conversion time	t_{CONV}	10-bit resolution	3.6 V ≤ V_{DD} ≤ 5.5 V	2.125		39	μs
			2.7 V ≤ V_{DD} ≤ 5.5 V	3.1875		39	μs
			2.4 V ≤ V_{DD} ≤ 5.5 V	17		39	μs
		10-bit resolution Target pin: Internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode)	3.6 V ≤ V_{DD} ≤ 5.5 V	2.375		39	μs
			2.7 V ≤ V_{DD} ≤ 5.5 V	3.5625		39	μs
			2.4 V ≤ V_{DD} ≤ 5.5 V	17		39	μs
Zero-scale error[Notes 1, 2]	E_{ZS}	10-bit resolution	2.4 V ≤ V_{DD} ≤ 5.5 V			±0.60	%FSR
Full-scale error[Notes 1, 2]	E_{FS}	10-bit resolution	2.4 V ≤ V_{DD} ≤ 5.5 V			±0.60	%FSR
Integral linearity error[Note 1]	ILE	10-bit resolution	2.4 V ≤ V_{DD} ≤ 5.5 V			±4.0	LSB
Differential linearity error[Note 1]	DLE	10-bit resolution	2.4 V ≤ V_{DD} ≤ 5.5 V			±2.0	LSB
Analog input voltage	V_{AIN}	ANI0, ANI1		0		V_{DD}	V
		ANI16 to ANI23		0		EV_{DD}	V
		Internal reference voltage output (2.4 V ≤ V_{DD} ≤ 5.5 V, HS (high-speed main) mode)		V_{BGR}[Note 3]			V
		Temperature sensor output voltage (2.4 V ≤ V_{DD} ≤ 5.5 V, HS (high-speed main) mode)		V_{TMPS25}[Note 3]			V

Notes 1. Excludes quantization error (±1/2 LSB).

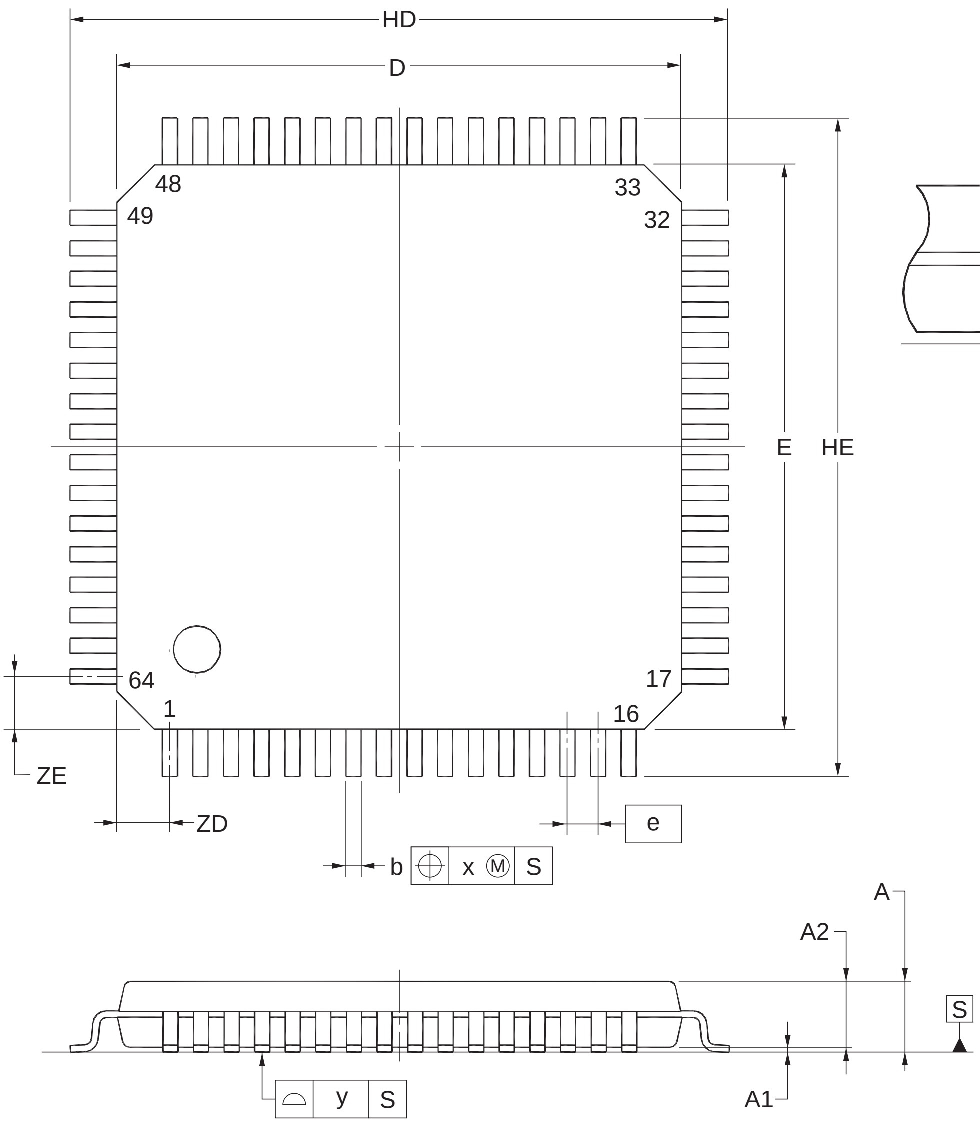
2. This value is indicated as a ratio (%FSR) to the full-scale value.

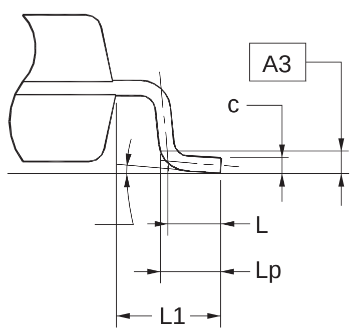
3. Refer to **3.6.2 Temperature sensor/internal reference voltage characteristics**.

4.5 64-pin Products

R5F10RLAAFA, R5F10RLCAFA
R5F10RLAGFA, R5F10RLCGFA

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LQFP64-12x12-0.65	PLQP0064JA-A	P64GK-65-UET-2	0.51





(UNIT:mm)

ITEM	DIMENSIONS
D	12.00±0.20
E	12.00±0.20
HD	14.00±0.20
HE	14.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
A3	0.25
b	$0.32^{+0.08}_{-0.07}$
c	$0.145^{+0.055}_{-0.045}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
e	0.65
x	0.13
y	0.10
ZD	1.125
ZE	1.125

NOTE
Each lead centerline is located within 0.13 mm of its true position at maximum material condition.

Rev.	Date	Description	
		Page	Summary
2.00	Jan 10, 2014	35	Modification of table in 2.4 AC Characteristics
		36	Addition of Minimum Instruction Execution Time during Main System Clock Operation
		37	Modification of AC Timing Test Points and External System Clock Timing
		39	Modification of AC Timing Test Points
		39	Modification of description, notes 1 and 2 in (1) During communication at same potential (UART mode)
		41, 42	Modification of description, remark 2 in (2) During communication at same potential (CSI mode)
		42, 43	Modification of description in (3) During communication at same potential (CSI mode)
		45	Modification of description, notes 1 and 3, and remark 3 in (4) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (1/2)
		46, 48	Modification of description, and remark 3 in (4) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (2/2)
		49, 50	Modification of table, and note 1, caution, and remark 3 in (5) Communication at different potential (2.5 V, 3 V) (CSI mode)
		51	Modification of table and note in (6) Communication at different potential (1.8 V, 2.5 V, 3 V) (1/3)
		52	Modification of table and notes 1 to 3 in (6) Communication at different potential (1.8 V, 2.5 V, 3 V) (2/3)
		53, 54	Modification of table, note 3, and remark 3 in (6) Communication at different potential (1.8 V, 2.5 V, 3 V) (3/3)
		56	Modification of table in (7) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (1/2)
		57	Modification of table in (7) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (2/2)
		59, 60	Addition of (1) I^2C standard mode
		61	Addition of (2) I^2C fast mode
		62	Addition of (3) I^2C fast mode plus
		63	Addition of table in 2.6.1 A/D converter characteristics
		63, 64	Modification of description and notes 3 to 5 in 2.6.1 (1)
		65	Modification of description, notes 3 and 4 in 2.6.1 (2)
		66	Modification of description, notes 3 and 4 in 2.6.1 (3)
		67	Modification of description, notes 3 and 4 in 2.6.1 (4)
		67	Modification of the table in 2.6.2 Temperature sensor/internal reference voltage characteristics
		68	Modification of the table and note in 2.6.3 POR circuit characteristics
		70	Modification of the table of LVD Detection Voltage of Interrupt & Reset Mode
		70	Modification from V_{DD} rise slope to Power supply voltage rising slope in 2.6.5 Supply voltage rise time
		75	Modification of description in 2.10 Dedicated Flash Memory Programmer Communication (UART)
		76	Modification of the figure in 2.11 Timing Specifications for Switching Flash Memory Programming Modes
		77 to 126	Addition of products for industrial applications (G: T_A = -40 to +105°C)
		127 to 133	Addition of product names for industrial applications (G: T_A = -40 to +105°C)
2.10	Sep 30, 2016	5	Modification of pin configuration in 1.3.1 32-pin products
		6	Modification of pin configuration in 1.3.2 44-pin products
		7	Modification of pin configuration in 1.3.3 48-pin products
		8	Modification of pin configuration in 1.3.4 52-pin products
		9, 10	Modification of pin configuration in 1.3.5 64-pin products
		17	Modification of description of main system clock in 1.6 Outline of Functions
		74	Modification of title of 2.8 RAM Data Retention Characteristics, Note, and figure
		74	Modification of table of 2.9 Flash Memory Programming Characteristics
		123	Modification of title of 3.8 RAM Data Retention Characteristics, Note, and figure
		123	Modification of table of 3.9 Flash Memory Programming Characteristics and addition of Note 4
		131	Modification of 4.5 64-pin Products