**What is "Embedded - Microcontrollers"?**

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details

Product Status	Obsolete
Core Processor	RL78
Core Size	16-Bit
Speed	24MHz
Connectivity	CSI, I²C, LINbus, UART/USART
Peripherals	DMA, LCD, LVD, POR, PWM, WDT
Number of I/O	33
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 9x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LFQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f10rgaafb-x0

1.5.2 44-pin products
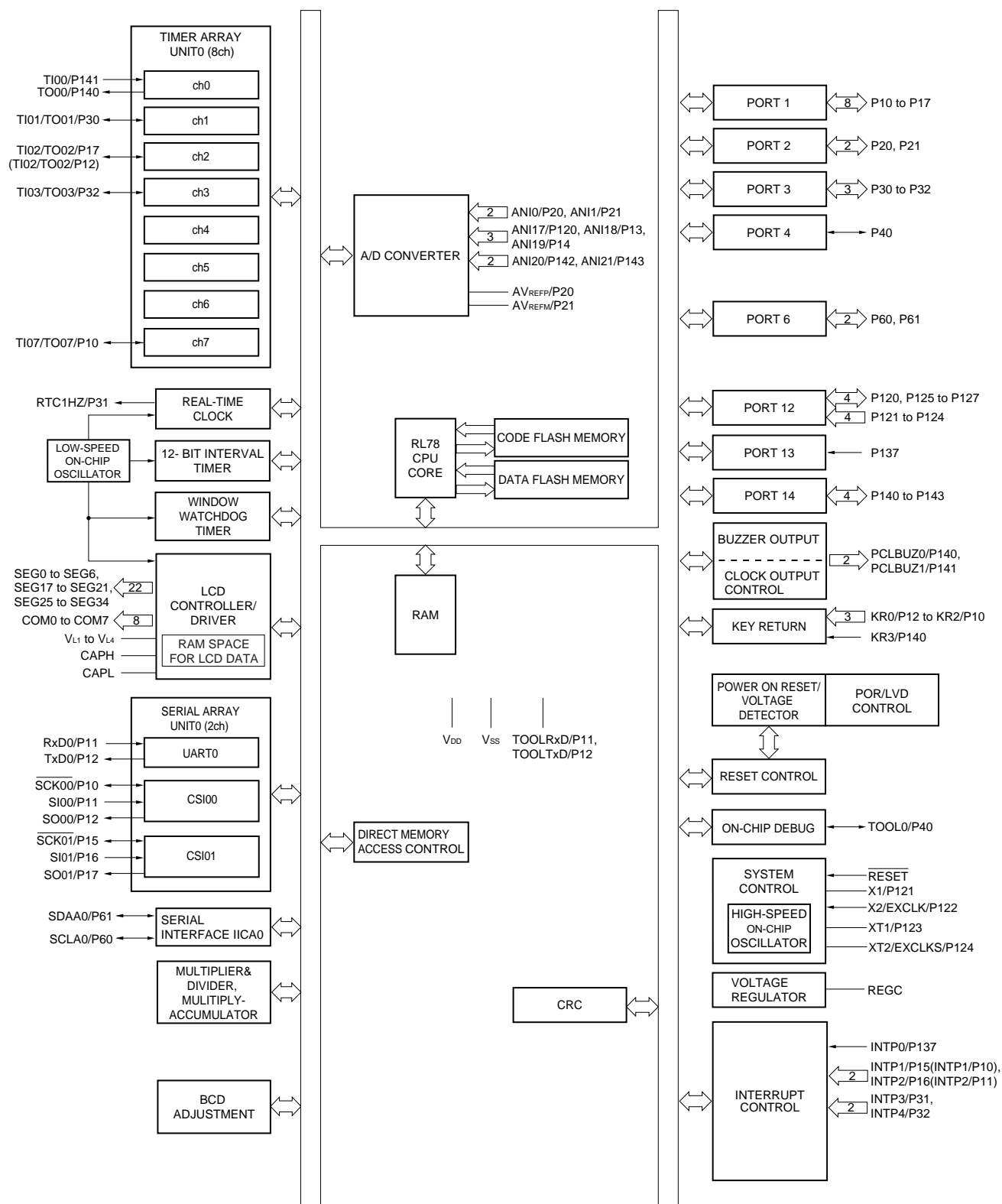
Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR)

2.3 DC Characteristics

2.3.1 Pin characteristics

(T_A = −40 to +85°C, 1.6 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)   **(1/5)**

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, high[Note 1]	I_{OH1}	Per pin for P10 to P17, P30 to P32, P40 to P43, P50 to P54, P70 to P74, P120, P125 to P127, P130, P140 to P147				−10.0 [Note 2]	mA
		Total of P10 to P14, P40 to P43, P120, P130, P140 to P147 (When duty = 70% [Note 3])	4.0 V ≤ EV_{DD} ≤ 5.5 V			−40.0	mA
			2.7 V ≤ EV_{DD} < 4.0 V			−8.0	mA
			1.8 V ≤ EV_{DD} < 2.7 V			−4.0	mA
			1.6 V ≤ EV_{DD} < 1.8 V			−2.0	mA
		Total of P15 to P17, P30 to P32, P50 to P54, P70 to P74, P125 to P127 (When duty = 70% [Note 3])	4.0 V ≤ EV_{DD} ≤ 5.5 V			−60.0	mA
			2.7 V ≤ EV_{DD} < 4.0 V			−15.0	mA
			1.8 V ≤ EV_{DD} < 2.7 V			−8.0	mA
			1.6 V ≤ EV_{DD} < 1.8 V			−4.0	mA
		Total of all pins (When duty = 70%[Note 3])				−100.0	mA
	I_{OH2}	P20, P21	Per pin			−0.1	mA
			Total of all pins	1.6 V ≤ V_{DD} ≤ 5.5 V			−0.2	mA

Notes 1. Value of current at which the device operation is guaranteed even if the current flows from the V_{DD} and EV_{DD} pins to an output pin.

2. Do not exceed the total current value.

3. Specification under conditions where the duty factor ≤ 70%.
The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (I_{OH} × 0.7)/(n × 0.01)

<Example> Where n = 80% and I_{OH} = −40.0 mA

Total output current of pins = (−40.0 × 0.7)/(80 × 0.01) ≅ −35.0 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

Caution   P10, P12, P15, and P17 do not output high level in N-ch open-drain mode.

Remark   Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

Notes 1. Total current flowing into V$_{DD}$ and EV$_{DD}$, including the input leakage current flowing when the level of the input pin is fixed to V$_{DD}$, EV$_{DD}$ or V$_{SS}$, EV$_{SS}$. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

2. During HALT instruction execution by flash memory.

3. When high-speed on-chip oscillator and subsystem clock are stopped.

4. When high-speed system clock and subsystem clock are stopped.

5. When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1). The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer, watchdog timer, and LCD controller/driver.

6. Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.

7. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

    HS (high-speed main) mode: 2.7 V ≤ V$_{DD}$ ≤ 5.5 V@1 MHz to 24 MHz

                                 2.4 V ≤ V$_{DD}$ ≤ 5.5 V@1 MHz to 16 MHz

    LS (low-speed main) mode: 1.8 V ≤ V$_{DD}$ ≤ 5.5 V@1 MHz to 8 MHz

    LV (low-voltage main) mode: 1.6 V ≤ V$_{DD}$ ≤ 5.5 V@1 MHz to 4 MHz

8. Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.

Remarks 1. f$_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

2. f$_{IH}$: High-speed on-chip oscillator clock frequency

3. f$_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)

4. Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is T$_A$ = 25°C

(5) Communication at different potential (2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output, corresponding CSI00 only)

(T$_A$ = –40 to +85°C, 2.7 V ≤ EV$_{DD}$ = V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS}$ = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t$_{KCY1}$	t$_{KCY1}$ ≥ 2/f$_{CLK}$	4.0 V ≤ EV$_{DD}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 20 pF, R$_b$ = 1.4 kΩ	200 **Note 1**		1150 **Note 1**		1150 **Note 1**		ns
			2.7 V ≤ EV$_{DD}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 20 pF, R$_b$ = 2.7 kΩ	300 **Note 1**		1150 **Note 1**		1150 **Note 1**		ns
SCKp high-level width	t$_{KH1}$	4.0 V ≤ EV$_{DD}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 20 pF, R$_b$ = 1.4 kΩ		t$_{KCY1}$/2 − 50		t$_{KCY1}$/2 − 50		t$_{KCY1}$/2 − 50		ns
		2.7 V ≤ EV$_{DD}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 20 pF, R$_b$ = 2.7 kΩ		t$_{KCY1}$/2 − 120		t$_{KCY1}$/2 − 120		t$_{KCY1}$/2 − 120		ns
SCKp low-level width	t$_{KL1}$	4.0 V ≤ EV$_{DD}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 20 pF, R$_b$ = 1.4 kΩ		t$_{KCY1}$/2 − 7		t$_{KCY1}$/2 − 50		t$_{KCY1}$/2 − 50		ns
		2.7 V ≤ EV$_{DD}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 20 pF, R$_b$ = 2.7 kΩ		t$_{KCY1}$/2 − 10		t$_{KCY1}$/2 − 50		t$_{KCY1}$/2 − 50		ns
SIp setup time (to SCKp↑) **Note 2**	t$_{SIK1}$	4.0 V ≤ EV$_{DD}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 20 pF, R$_b$ = 1.4 kΩ		58		479		479		ns
		2.7 V ≤ EV$_{DD}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 20 pF, R$_b$ = 2.7 kΩ		121		479		479		ns
SIp hold time (from SCKp↑) **Note 2**	t$_{KSI1}$	4.0 V ≤ EV$_{DD}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 20 pF, R$_b$ = 1.4 kΩ		10		10		10		ns
		2.7 V ≤ EV$_{DD}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 20 pF, R$_b$ = 2.7 kΩ		10		10		10		ns
Delay time from SCKp↓ to SOp output **Note 2**	t$_{KSO1}$	4.0 V ≤ EV$_{DD}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 20 pF, R$_b$ = 1.4 kΩ			60		60		60	ns
		2.7 V ≤ EV$_{DD}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 20 pF, R$_b$ = 2.7 kΩ			130		130		130	ns
SIp setup time (to SCKp↓) **Note 3**	t$_{SIK1}$	4.0 V ≤ EV$_{DD}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 20 pF, R$_b$ = 1.4 kΩ		23		110		110		ns
		2.7 V ≤ EV$_{DD}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 20 pF, R$_b$ = 2.7 kΩ		33		110		110		ns
SIp hold time (from SCKp↓) **Note 3**	t$_{KSI1}$	4.0 V ≤ EV$_{DD}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 20 pF, R$_b$ = 1.4 kΩ		10		10		10		ns
		2.7 V ≤ EV$_{DD}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 20 pF, R$_b$ = 2.7 kΩ		10		10		10		ns
Delay time from SCKp↑ to SOp output **Note 3**	t$_{KSO1}$	4.0 V ≤ EV$_{DD}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 20 pF, R$_b$ = 1.4 kΩ			10		10		10	ns
		2.7 V ≤ EV$_{DD}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 20 pF, R$_b$ = 2.7 kΩ			10		10		10	ns

(**Notes**, **Caution** and **Remarks** are listed on the next page.)

(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output) (1/3)
(T_A = –40 to +85°C, 1.8 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t_{KCY1}	t_{KCY1} ≥ 4/f_{CLK} 4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	300		1150		1150		ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	500		1150		1150		ns
		2.4 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ	1150		1150		1150		ns
		1.8 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V **Note**, C_b = 30 pF, R_b = 5.5 kΩ			1150		1150		ns
SCKp high-level width	t_{KH1}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	t_{KCY1}/2 − 75		t_{KCY1}/2 − 75		t_{KCY1}/2 − 75		ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	t_{KCY1}/2 − 170		t_{KCY1}/2 − 170		t_{KCY1}/2 − 170		ns
		2.4 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ	t_{KCY1}/2 − 458		t_{KCY1}/2 − 458		t_{KCY1}/2 − 458		ns
		1.8 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V **Note**, C_b = 30 pF, R_b = 5.5 kΩ			t_{KCY1}/2 − 458		t_{KCY1}/2 − 458		ns
SCKp low-level width	t_{KL1}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	t_{KCY1}/2 − 12		t_{KCY1}/2 − 50		t_{KCY1}/2 − 50		ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	t_{KCY1}/2 − 18		t_{KCY1}/2 − 50		t_{KCY1}/2 − 50		ns
		2.4 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ	t_{KCY1}/2 − 50		t_{KCY1}/2 − 50		t_{KCY1}/2 − 50		ns
		1.8 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V **Note**, C_b = 30 pF, R_b = 5.5 kΩ			t_{KCY1}/2 − 50		t_{KCY1}/2 − 50		ns

Note Use it with EV_{DD} ≥ V_b.

Caution **Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance (32-pin to 52-pin products)/EV_{DD} tolerance (64-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.**
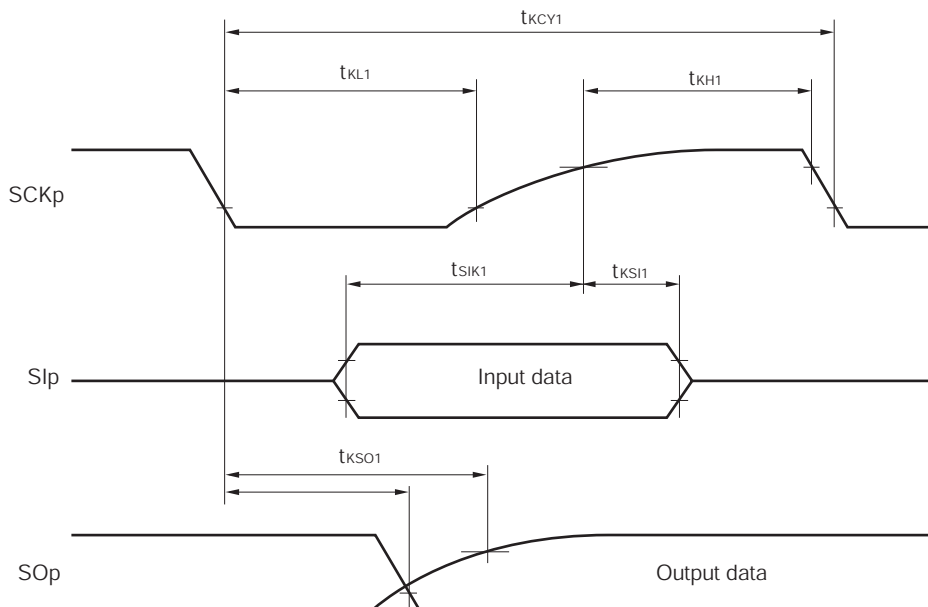
(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output) (3/3)
(T_A = –40 to +85°C, 1.8 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SIp hold time (from SCKp↓) [Note 2]	t_{KSI1}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	19		19		19		ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	19		19		19		ns
		2.4 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ	19		19		19		ns
		1.8 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V [Note 3], C_b = 30 pF, R_b = 5.5 kΩ			19		19		ns
Delay time from SCKp↑ to SOp output [Note 2]	t_{KSO1}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		25		25		25	ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		25		25		25	ns
		2.4 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ		25		25		25	ns
		1.8 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V [Note 3], C_b = 30 pF, R_b = 5.5 kΩ				25		25	ns

Notes   1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

2. When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

3. Use it with EV_{DD} ≥ V_b.

Caution   Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance (32-pin to 52-pin products)/EV_{DD} tolerance (64-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)

CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)
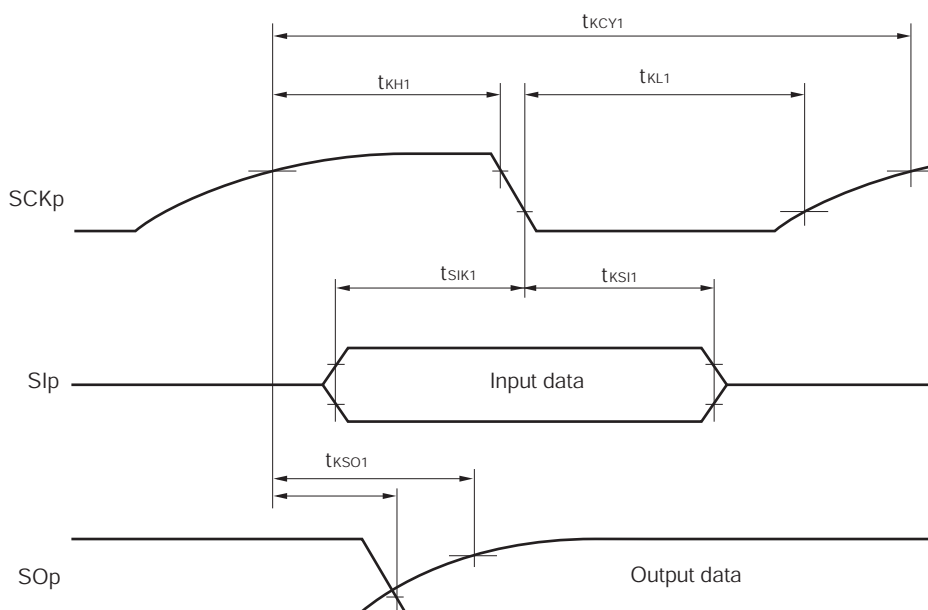
Remark p: CSI number (p = 00, 01), m: Unit number (m = 0), n: Channel number (n = 0, 1),
g: PIM and POM number (g = 1)

(7) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (slave mode, SCKp... external clock input)
(T$_A$ = −40 to +85°C, 1.8 V ≤ EV$_{DD}$ = V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS}$ = 0 V)   **(1/2)**

Parameter	Symbol	Conditions		HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time [Note 1]	t$_{KCY2}$	4.0 V ≤ EV$_{DD}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V	20 MHz < f$_{MCK}$ ≤ 24 MHz	12/f$_{MCK}$						ns
			8 MHz < f$_{MCK}$ ≤ 20 MHz	10/f$_{MCK}$						ns
			4 MHz < f$_{MCK}$ ≤ 8 MHz	8/f$_{MCK}$		16/f$_{MCK}$				ns
			f$_{MCK}$ ≤ 4 MHz	6/f$_{MCK}$		10/f$_{MCK}$		10/f$_{MCK}$		ns
		2.7 V ≤ EV$_{DD}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V	20 MHz < f$_{MCK}$ ≤ 24 MHz	16/f$_{MCK}$						ns
			16 MHz < f$_{MCK}$ ≤ 20 MHz	14/f$_{MCK}$						ns
			8 MHz < f$_{MCK}$ ≤ 16 MHz	12/f$_{MCK}$						ns
			4 MHz < f$_{MCK}$ ≤ 8 MHz	8/f$_{MCK}$		16/f$_{MCK}$				ns
			f$_{MCK}$ ≤ 4 MHz	6/f$_{MCK}$		10/f$_{MCK}$		10/f$_{MCK}$		ns
		2.4 V ≤ EV$_{DD}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V	20 MHz < f$_{MCK}$ ≤ 24 MHz	36/f$_{MCK}$						ns
			16 MHz < f$_{MCK}$ ≤ 20 MHz	32/f$_{MCK}$						ns
			8 MHz < f$_{MCK}$ ≤ 16 MHz	26/f$_{MCK}$						ns
			4 MHz < f$_{MCK}$ ≤ 8 MHz	16/f$_{MCK}$		16/f$_{MCK}$				ns
			f$_{MCK}$ ≤ 4 MHz	10/f$_{MCK}$		10/f$_{MCK}$		10/f$_{MCK}$		ns
		1.8 V ≤ EV$_{DD}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V [Note 2]	4 MHz < f$_{MCK}$ ≤ 8 MHz			16/f$_{MCK}$				ns
			f$_{MCK}$ ≤ 4 MHz			10/f$_{MCK}$		10/f$_{MCK}$		ns
SCKp high-/low-level width	t$_{KH2}$, t$_{KL2}$	4.0 V ≤ EV$_{DD}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V		t$_{KCY2}$/2 − 12		t$_{KCY2}$/2 − 50		t$_{KCY2}$/2 − 50		ns
		2.7 V ≤ EV$_{DD}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V		t$_{KCY2}$/2 − 18		t$_{KCY2}$/2 − 50		t$_{KCY2}$/2 − 50		ns
		2.4 V ≤ EV$_{DD}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V		t$_{KCY2}$/2 − 50		t$_{KCY2}$/2 − 50		t$_{KCY2}$/2 − 50		ns
		1.8 V ≤ EV$_{DD}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V [Note 2]				t$_{KCY2}$/2 − 50		t$_{KCY2}$/2 − 50		ns
SIp setup time (to SCKp↑) [Note 3]	t$_{SIK2}$	4.0 V ≤ EV$_{DD}$ < 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V		1/f$_{MCK}$ + 20		1/f$_{MCK}$ + 30		1/f$_{MCK}$ + 30		ns
		2.7 V ≤ EV$_{DD}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V		1/f$_{MCK}$ + 20		1/f$_{MCK}$ + 30		1/f$_{MCK}$ + 30		ns
		2.4 V ≤ EV$_{DD}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V		1/f$_{MCK}$ + 30		1/f$_{MCK}$ + 30		1/f$_{MCK}$ + 30		ns
		1.8 V ≤ EV$_{DD}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V [Note 2]				1/f$_{MCK}$ + 30		1/f$_{MCK}$ + 30		ns
SIp hold time (from SCKp↑) [Note 4]	t$_{KSI2}$	4.0 V ≤ EV$_{DD}$ < 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V		1/f$_{MCK}$ + 31		1/f$_{MCK}$ + 31		1/f$_{MCK}$ + 31		ns
		2.7 V ≤ EV$_{DD}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V		1/f$_{MCK}$ + 31		1/f$_{MCK}$ + 31		1/f$_{MCK}$ + 31		ns
		2.4 V ≤ EV$_{DD}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V		1/f$_{MCK}$ + 31		1/f$_{MCK}$ + 31		1/f$_{MCK}$ + 31		ns
		1.8 V ≤ EV$_{DD}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V [Note 2]				1/f$_{MCK}$ + 31		1/f$_{MCK}$ + 31		ns

(**Notes**, **Caution** and **Remarks** are listed on the next page.)

(2) When reference voltage (+) = AV_{REFP}/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (–) = AV_{REFM}/ANI1 (ADREFM = 1), target pin : ANI16 to ANI23

(T_A = –40 to +85°C, 1.6 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, 1.6 V ≤ AV_{REFP} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V, Reference voltage (+) = AV_{REFP}, Reference voltage (–) = AV_{REFM} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error[Note 1]	AINL	10-bit resolution AV_{REFP} = EV_{DD} = V_{DD} [Note 3]	1.8 V ≤ AV_{REFP} ≤ 5.5 V		1.2	±5.0	LSB
			1.6 V ≤ AV_{REFP} ≤ 5.5 V [Note 4]		1.2	±8.5	LSB
Conversion time	t_{CONV}	10-bit resolution AV_{REFP} = EV_{DD} = V_{DD} [Note 3]	3.6 V ≤ V_{DD} ≤ 5.5 V	2.125		39	μs
			2.7 V ≤ V_{DD} ≤ 5.5 V	3.1875		39	μs
			1.8 V ≤ V_{DD} ≤ 5.5 V	17		39	μs
			1.6 V ≤ V_{DD} ≤ 5.5 V	57		95	μs
Zero-scale error[Notes 1, 2]	E_{ZS}	10-bit resolution AV_{REFP} = EV_{DD} = V_{DD} [Note 3]	1.8 V ≤ AV_{REFP} ≤ 5.5 V			±0.35	%FSR
			1.6 V ≤ AV_{REFP} ≤ 5.5 V [Note 4]			±0.60	%FSR
Full-scale error[Notes 1, 2]	E_{FS}	10-bit resolution AV_{REFP} = EV_{DD} = V_{DD} [Note 3]	1.8 V ≤ AV_{REFP} ≤ 5.5 V			±0.35	%FSR
			1.6 V ≤ AV_{REFP} ≤ 5.5 V [Note 4]			±0.60	%FSR
Integral linearity error[Note 1]	ILE	10-bit resolution AV_{REFP} = EV_{DD} = V_{DD} [Note 3]	1.8 V ≤ AV_{REFP} ≤ 5.5 V			±3.5	LSB
			1.6 V ≤ AV_{REFP} ≤ 5.5 V [Note 4]			±6.0	LSB
Differential linearity error [Note 1]	DLE	10-bit resolution AV_{REFP} = EV_{DD} = V_{DD} [Note 3]	1.8 V ≤ AV_{REFP} ≤ 5.5 V			±2.0	LSB
			1.6 V ≤ AV_{REFP} ≤ 5.5 V [Note 4]			±2.5	LSB
Analog input voltage	V_{AIN}			0		AV_{REFP} and EV_{DD}	V

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. When AV_{REFP} < EV_{DD} = V_{DD}, the MAX. values are as follows.

Overall error: Add ±4.0 LSB to the MAX. value when AV_{REFP} = V_{DD}.

Zero-scale error/Full-scale error: Add ±0.20%FSR to the MAX. value when AV_{REFP} = V_{DD}.

Integral linearity error/Differential linearity error: Add ±2.0 LSB to the MAX. value when AV_{REFP} = V_{DD}.

4. When the conversion time is set to 57 μs (min.) and 95 μs (max.).

<R>
2.8 RAM Data Retention Characteristics

(T_A = –40 to +85°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.46[Note]		5.5	V

<R> **Note** This depends on the POR detection voltage. For a falling voltage, data in RAM are retained until the voltage reaches the level that triggers a POR reset but not once it reaches the level at which a POR reset is generated.

<R>
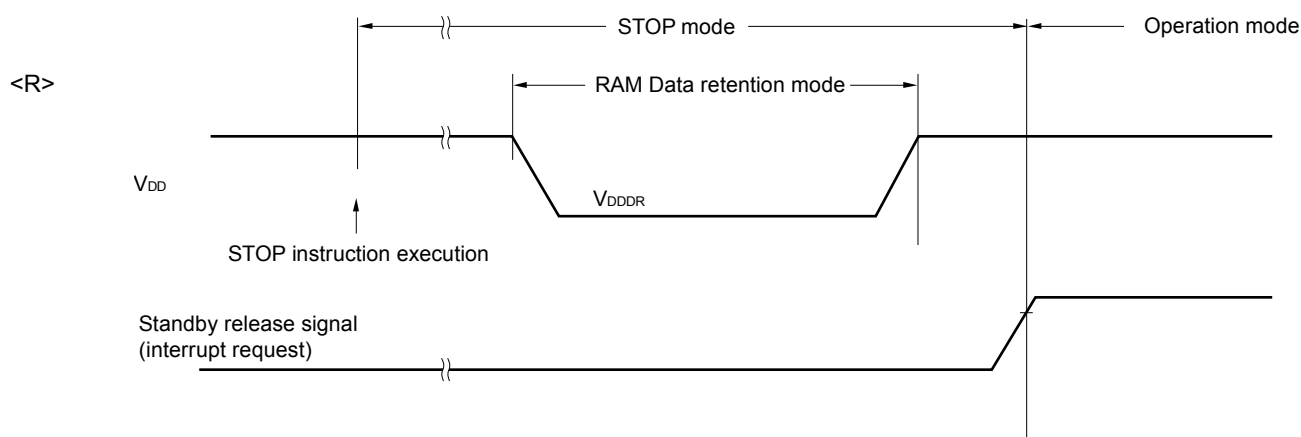
2.9 Flash Memory Programming Characteristics

(T_A = –40 to +85°C, 1.8 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
System clock frequency	f_{CLK}	1.8 V ≤ V_{DD} ≤ 5.5 V	1		24	MHz
<R> Number of code flash rewrites **Note 1, 2, 3**	C_{erwr}	Retained for 20 years T_A = 85°C	1,000			Times
<R> Number of data flash rewrites **Note 1, 2, 3**		Retained for 1 year T_A = 25°C		1,000,000		
<R>		Retained for 5 years T_A = 85°C	100,000			
<R>		Retained for 20 years T_A = 85°C	10,000			

Notes 1. 1 erase + 1 write after the erase is regarded as 1 rewrite.
     The retaining years are until next rewrite after the rewrite.
  2. When using flash memory programmer and Renesas Electronics self programming library
  3. This characteristic indicates the flash memory characteristic and based on Renesas Electronics reliability test.

Remark When updating data multiple times, use the flash memory as one for updating data.

2.10 Dedicated Flash Memory Programmer Communication (UART)

(T_A = –40 to +85°C, 1.8 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		During flash memory programming	115,200		1,000,000	bps

2.11 Timing Specifications for Switching Flash Memory Programming Modes

(T$_A$ = –40 to +85°C, 1.8 V ≤ EV$_{DD}$ = V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS}$ = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Time to complete the communication for the initial setting after the external reset is released	t$_{SUINIT}$	POR and LVD reset must be released before the external reset is released.			100	ms
Time to release the external reset after the TOOL0 pin is set to the low level	t$_{SU}$	POR and LVD reset must be released before the external reset is released.	10			μ s
Time to hold the TOOL0 pin at the low level after the external reset is released (excluding the processing time of the firmware to control the flash memory)	t$_{HD}$	POR and LVD reset must be released before the external reset is released.	1			ms
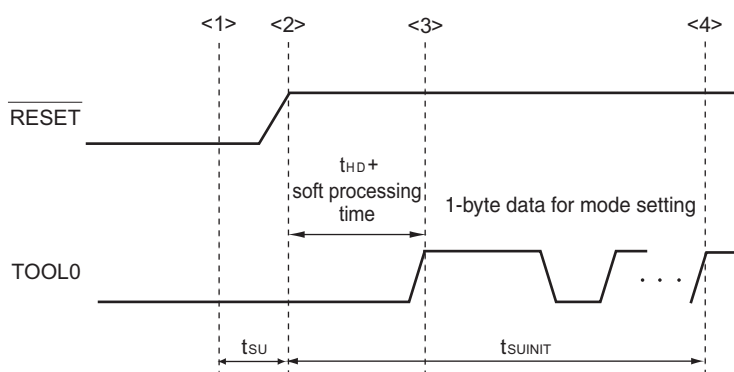
<1> The low level is input to the TOOL0 pin.

<2> The external reset is released (POR and LVD reset must be released before the external reset is released.).

<3> The TOOL0 pin is set to the high level.

<4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

Remark t$_{SUINIT}$: Communication for the initial setting must be completed within 100 ms after a reset is released during this period.

t$_{SU}$:   Time to release the external reset after the TOOL0 pin is set to the low level

t$_{HD}$:   Time to hold the TOOL0 pin at the low level after the external reset is released (excluding the processing time of the firmware to control the flash memory)

Notes 1. Total current flowing into V$_{DD}$ and EV$_{DD}$, including the input leakage current flowing when the level of the input pin is fixed to V$_{DD}$, EV$_{DD}$ or V$_{SS}$, EV$_{SS}$. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

2. During HALT instruction execution by flash memory.

3. When high-speed on-chip oscillator and subsystem clock are stopped.

4. When high-speed system clock and subsystem clock are stopped.

5. When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1). The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer, watchdog timer, and LCD controller/driver.

6. Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.

7. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

   HS (high-speed main) mode: 2.7 V ≤ V$_{DD}$ ≤ 5.5 V@1 MHz to 24 MHz

   2.4 V ≤ V$_{DD}$ ≤ 5.5 V@1 MHz to 16 MHz

8. Regarding the value for current operate the subsystem clock in STOP mode, refer to that in HALT mode.

Remarks 1. f$_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

2. f$_{IH}$: High-speed on-chip oscillator clock frequency

3. f$_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)

4. Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is T$_A$ = 25°C

3.4 AC Characteristics

3.4.1 Basic operation

(T$_A$ = –40 to +105°C, 2.4 V ≤ EV$_{DD}$ = V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS}$ = 0 V)

Items	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Instruction cycle (minimum instruction execution time)	T$_{CY}$	Main system clock (f$_{MAIN}$) operation	HS (high-speed main) mode	2.7 V ≤ V$_{DD}$ ≤ 5.5 V	0.04167		1	μs
				2.4 V ≤ V$_{DD}$ < 2.7 V	0.0625		1	μs
		Subsystem clock (f$_{SUB}$) operation		2.4 V ≤ V$_{DD}$ ≤ 5.5 V	28.5	30.5	31.3	μs
		In the self programming mode	HS (high-speed main) mode	2.7 V ≤ V$_{DD}$ ≤ 5.5 V	0.04167		1	μs
				2.4 V ≤ V$_{DD}$ < 2.7 V	0.0625		1	μs
External system clock frequency	f$_{EX}$	2.7 V ≤ V$_{DD}$ ≤ 5.5 V			1.0		20.0	MHz
		2.4 V ≤ V$_{DD}$ < 2.7 V			1.0		16.0	MHz
	f$_{EXS}$				32		35	kHz
External system clock input high-level width, low-level width	t$_{EXH}$, t$_{EXL}$	2.7 V ≤ V$_{DD}$ ≤ 5.5 V			24			ns
		2.4 V ≤ V$_{DD}$ < 2.7 V			30			ns
	t$_{EXHS}$, t$_{EXLS}$				13.7			μs
TI00 to TI07 input high-level width, low-level width	t$_{TIH}$, t$_{TIL}$				1/f$_{MCK}$+10			ns
TO00 to TO07 output frequency	f$_{TO}$	HS (high-speed main) mode	4.0 V ≤ EV$_{DD}$ ≤ 5.5 V				16	MHz
			2.7 V ≤ EV$_{DD}$ < 4.0 V				8	MHz
			2.4 V ≤ EV$_{DD}$ < 2.7 V				4	MHz
PCLBUZ0, PCLBUZ1 output frequency	f$_{PCL}$	HS (high-speed main) mode	4.0 V ≤ EV$_{DD}$ ≤ 5.5 V				16	MHz
			2.7 V ≤ EV$_{DD}$ < 4.0 V				8	MHz
			2.4 V ≤ EV$_{DD}$ < 2.7 V				4	MHz
Interrupt input high-level width, low-level width	t$_{INTH}$, t$_{INTL}$	INTP0	2.4 V ≤ V$_{DD}$ ≤ 5.5 V		1			μs
		INTP1 to INTP7	2.4 V ≤ EV$_{DD}$ ≤ 5.5 V		1			μs
Key interrupt input low-level width	t$_{KR}$	KR0 to KR3	2.4 V ≤ EV$_{DD}$ ≤ 5.5 V		250			ns
$\overline{\text{RESET}}$ low-level width	t$_{RSL}$				10			μs

Remark f$_{MCK}$: Timer array unit operation clock frequency

(Operation clock to be set by the CKS0n bit of timer mode register 0n (TMR0n).

n: Channel number (n = 0 to 7))

Minimum Instruction Execution Time during Main System Clock Operation

T_{CY} vs V_{DD} (HS (high-speed main) mode)

— When the high-speed on-chip oscillator clock is selected
- - - During self programming
-·-· When high-speed system clock is selected
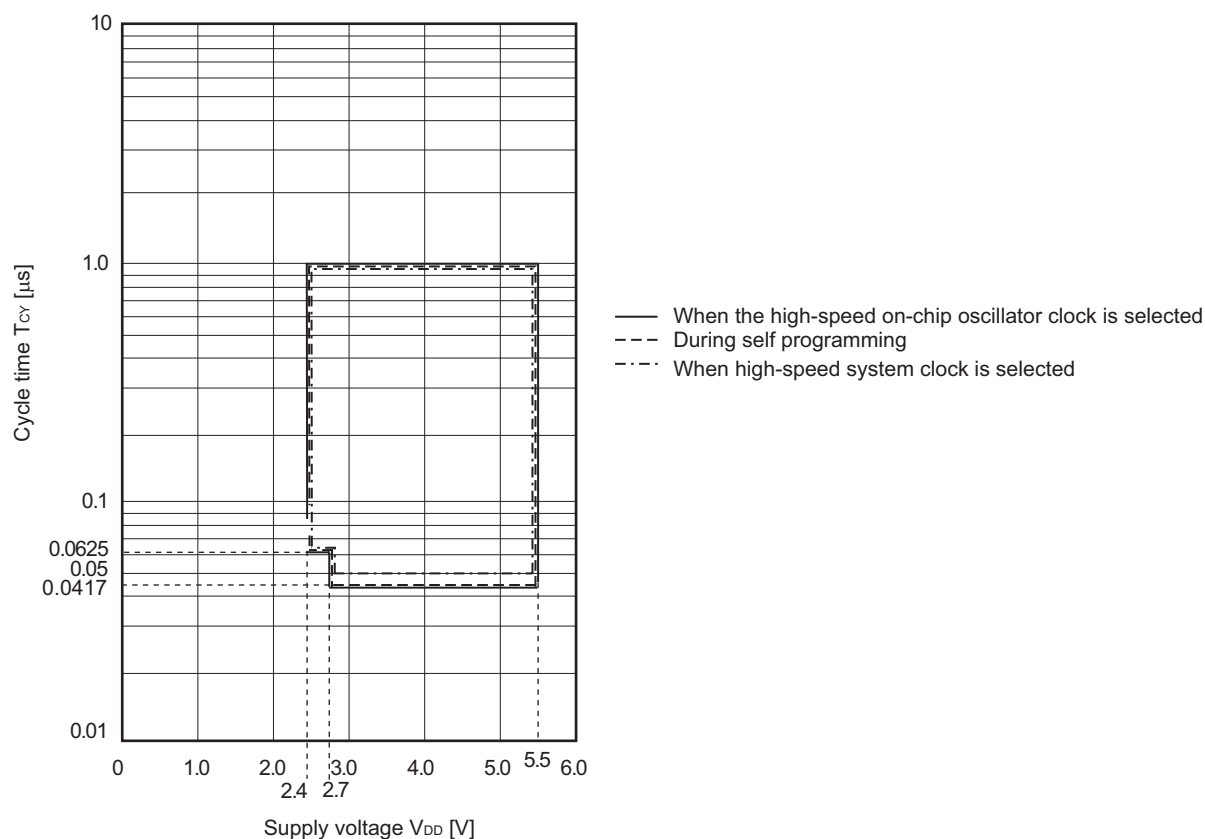
AC Timing Test Points
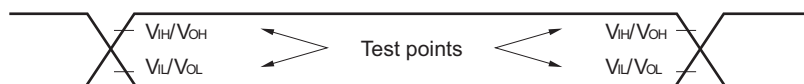
External System Clock Timing
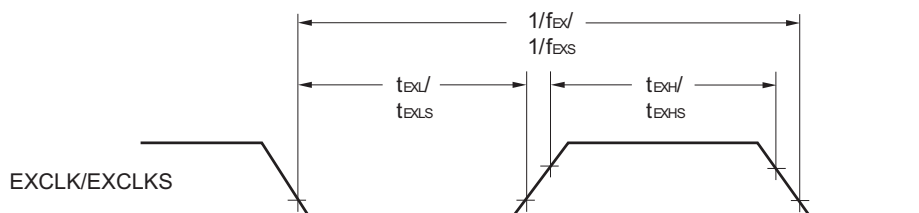
3.5 Peripheral Functions Characteristics

AC Timing Test Points
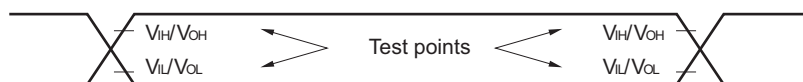
3.5.1 Serial array unit

(1) During communication at same potential (UART mode)

(T_A = –40 to +105°C, 2.4 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		Unit
				MIN.	MAX.	
Transfer rate [Note 1]					f_{MCK}/12	bps
		Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} [Note 2]			2.0	Mbps

Notes 1. Transfer rate in the SNOOZE mode is 4800 bps only.

2. The maximum operating frequencies of the CPU/peripheral hardware clock (f_{CLK}) are:

HS (high-speed main) mode: 24 MHz (2.7 V ≤ V_{DD} ≤ 5.5 V)

16 MHz (2.4 V ≤ V_{DD} ≤ 5.5 V)

Caution   Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using
port input mode register g (PIMg) and port output mode register g (POMg).

UART mode connection diagram (during communication at same potential)
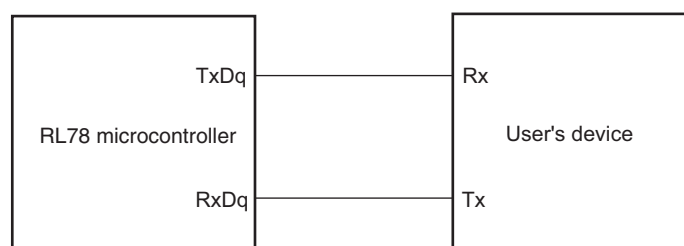
UART mode bit width (during communication at same potential) (reference)
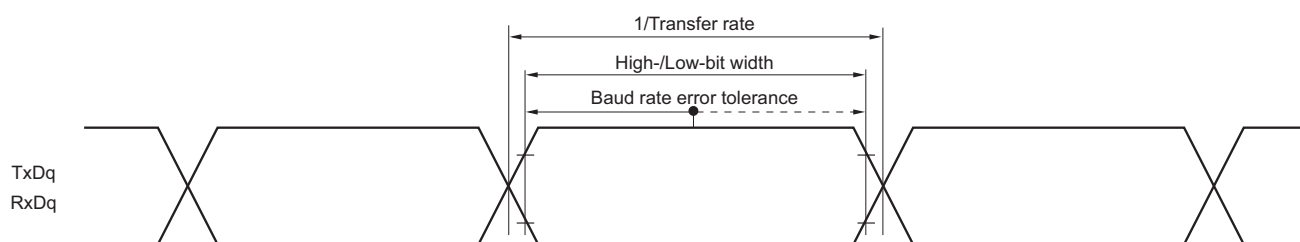
Remarks 1.   q: UART number (q = 0), g: PIM and POM number (g = 1)

2. f_{MCK}: Serial array unit operation clock frequency

(Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 01))

3.7.2 Internal voltage boosting method

(1) 1/3 bias method

(T$_A$ = –40 to +105°C, 2.4 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
LCD output voltage variation range	V$_{L1}$	C1 to C4[Note 1] = 0.47 μF	VLCD = 04H	0.90	1.00	1.08	V
			VLCD = 05H	0.95	1.05	1.13	V
			VLCD = 06H	1.00	1.10	1.18	V
			VLCD = 07H	1.05	1.15	1.23	V
			VLCD = 08H	1.10	1.20	1.28	V
			VLCD = 09H	1.15	1.25	1.33	V
			VLCD = 0AH	1.20	1.30	1.38	V
			VLCD = 0BH	1.25	1.35	1.43	V
			VLCD = 0CH	1.30	1.40	1.48	V
			VLCD = 0DH	1.35	1.45	1.53	V
			VLCD = 0EH	1.40	1.50	1.58	V
			VLCD = 0FH	1.45	1.55	1.63	V
			VLCD = 10H	1.50	1.60	1.68	V
			VLCD = 11H	1.55	1.65	1.73	V
			VLCD = 12H	1.60	1.70	1.78	V
			VLCD = 13H	1.65	1.75	1.83	V
Doubler output voltage	V$_{L2}$	C1 to C4[Note 1] = 0.47 μF		2 V$_{L1}$ −0.1	2 V$_{L1}$	2 V$_{L1}$	V
Tripler output voltage	V$_{L4}$	C1 to C4[Note 1] = 0.47 μF		3 V$_{L1}$ −0.15	3 V$_{L1}$	3 V$_{L1}$	V
Reference voltage setup time [Note 2]	t$_{VWAIT1}$			5			ms
Voltage boost wait time[Note 3]	t$_{VWAIT2}$	C1 to C4[Note 1] = 0.47 μF		500			ms

Notes 1. This is a capacitor that is connected between voltage pins used to drive the LCD.

C1: A capacitor connected between CAPH and CAPL

C2: A capacitor connected between V$_{L1}$ and GND

C3: A capacitor connected between V$_{L2}$ and GND

C4: A capacitor connected between V$_{L4}$ and GND

C1 = C2 = C3 = C4 = 0.47 μF±30%

2. This is the time required to wait from when the reference voltage is specified by using the VLCD register (or when the internal voltage boosting method is selected [by setting the MDSET1 and MDSET0 bits of the LCDM0 register to 01B] if the default value reference voltage is used) until voltage boosting starts (VLCON = 1).

3. This is the wait time from when voltage boosting is started (VLCON = 1) until display is enabled (LCDON = 1).

3.7.3 Capacitor split method

1/3 bias method

(T$_A$ = –40 to +105°C, 2.4 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
V$_{L4}$ voltage	V$_{L4}$	C1 to C4 = 0.47 μF[Note 2]		V$_{DD}$		V
V$_{L2}$ voltage	V$_{L2}$	C1 to C4 = 0.47 μF[Note 2]	2/3 V$_{L4}$ – 0.1	2/3 V$_{L4}$	2/3 V$_{L4}$ + 0.1	V
V$_{L1}$ voltage	V$_{L1}$	C1 to C4 = 0.47 μF[Note 2]	1/3 V$_{L4}$ – 0.1	1/3 V$_{L4}$	1/3 V$_{L4}$ + 0.1	V
Capacitor split wait time[Note 1]	t$_{VWAIT}$		100			ms

Notes 1. This is the wait time from when voltage bucking is started (VLCON = 1) until display is enabled (LCDON = 1).

2. This is a capacitor that is connected between voltage pins used to drive the LCD.

C1: A capacitor connected between CAPH and CAPL

C2: A capacitor connected between V$_{L1}$ and GND

C3: A capacitor connected between V$_{L2}$ and GND

C4: A capacitor connected between V$_{L4}$ and GND

C1 = C2 = C3 = C4 = 0.47 µF±30%

4.3 48-pin Products

R5F10RG8AFB, R5F10RGAAFB, R5F10RGCAFB
R5F10RG8GFB, R5F10RGAGFB, R5F10RGCGFB

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LFQFP48-7x7-0.50	PLQP0048KF-A	P48GA-50-8EU-1	0.16

detail of lead end

(UNIT:mm)

ITEM	DIMENSIONS
D	7.00±0.20
E	7.00±0.20
HD	9.00±0.20
HE	9.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
A3	0.25
b	0.22±0.05
c	$0.145^{+0.055}_{-0.045}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
	$3°^{+5°}_{-3°}$
e	0.50
x	0.08
y	0.08
ZD	0.75
ZE	0.75
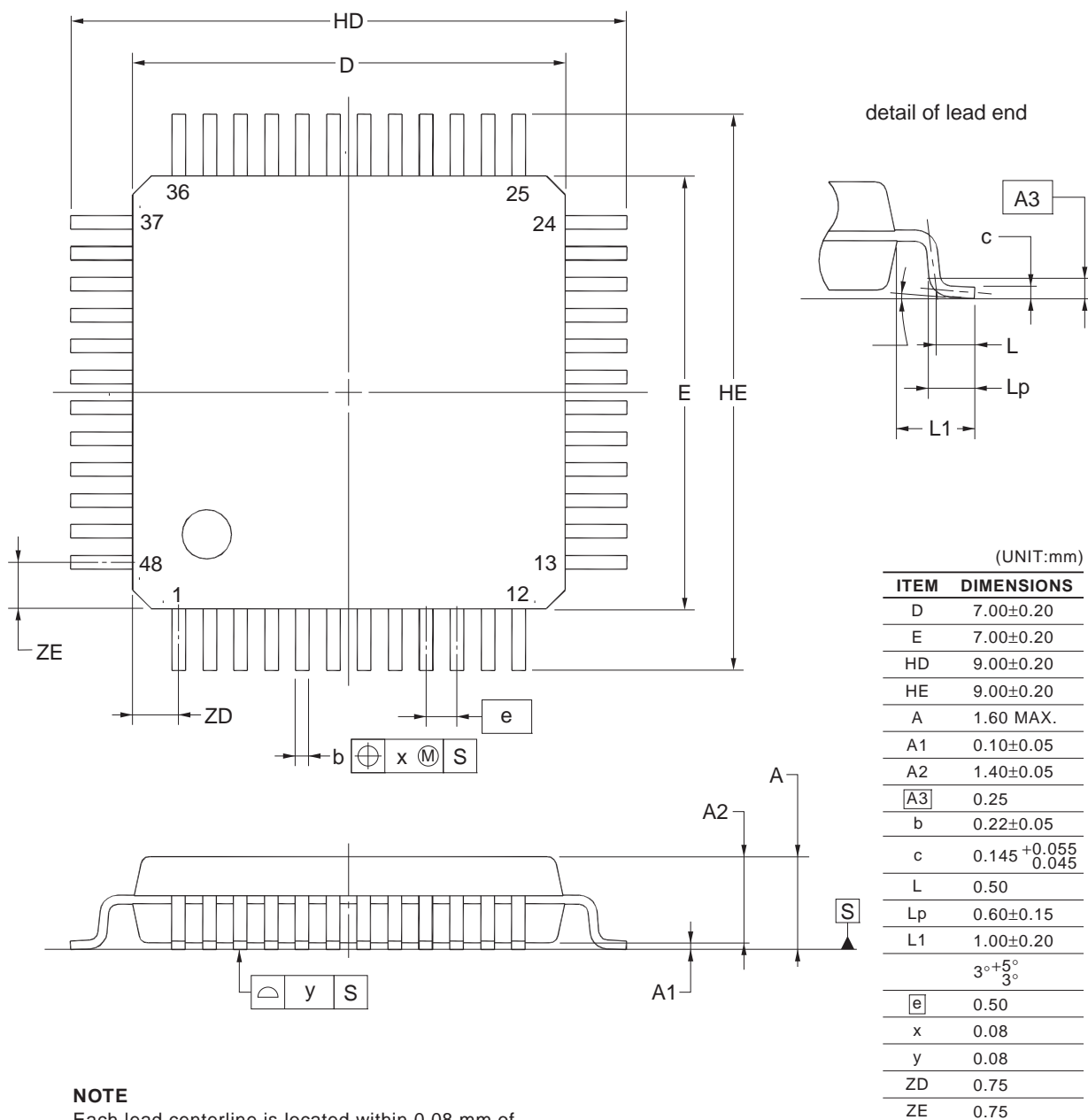
NOTE
Each lead centerline is located within 0.08 mm of
its true position at maximum material condition.

The mark "<R>" shows major revised points. The revised points can be easily searched by copying an "<R>" in the PDF file and specifying it in the "Find what:" field.

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