



Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Obsolete
Core Processor	RL78
Core Size	16-Bit
Speed	24MHz
Connectivity	CSI, I ² C, LINbus, UART/USART
Peripherals	DMA, LCD, LVD, POR, PWM, WDT
Number of I/O	33
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 9x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LFQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f10rgagfb-x0

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	Vih1	P10 to P17, P30 to P32, P40 to P43, P50 to P54, P70 to P74, P120, P125 to P127, P140 to P147	Normal input buffer	0.8EVDD		EVDD	V
	VIH2	P10, P11, P15, P16	, P15, P16 TTL input buffer $4.0 V \le EV_{DD} \le 5.5 V$ TTL input buffer $3.3 V \le EV_{DD} < 4.0 V$ TTL input buffer $1.6 V \le EV_{DD} < 3.3 V$			EVDD	V
						EVDD	V
						EVDD	V
	VIH3	P20, P21		0.7V _{DD}		VDD	V
	VIH4	P60, P61					V
	VIH5	P121 to P124, P137, EXCLK, EXCLK	S, RESET	0.8V _{DD}		VDD	V
Input voltage, Iow	VIL1	P10 to P17, P30 to P32, P40 to P43, P50 to P54, P70 to P74, P120, P125 to P127, P140 to P147	Normal input buffer	0		0.2EV _{DD}	V
	VIL2	P10, P11, P15, P16	TTL input buffer $4.0 \text{ V} \le \text{EV}_{\text{DD}} \le 5.5 \text{ V}$	0		0.8	V
			TTL input buffer $3.3 \text{ V} \leq \text{EV}_{\text{DD}} < 4.0 \text{ V}$	0		0.5	V
			TTL input buffer 1.6 V \leq EV _{DD} $<$ 3.3 V			0.32	V
	VIL3	P20, P21				0.3VDD	V
	VIL4	P60, P61		0		0.3EVDD	V
	VIL5	P121 to P124, P137, EXCLK, EXCLK	S, RESET	0		0.2V _{DD}	V

$(T_A = -40 \text{ to } +85^{\circ}C, 1.6 \text{ V} \le EV_{DD} = V_{DD} \le 5.5 \text{ V}, \text{ Vss} = EV_{SS} = 0 \text{ V})$



Caution The maximum value of VIH of P10, P12, P15, P17 is EVDD, even in the N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.



- Notes 1. Current flowing to VDD.
 - 2. When high speed on-chip oscillator and high-speed system clock are stopped.
 - 3. Current flowing only to the real-time clock (RTC) (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either IDD1 or IDD2, and IRTC, when the real-time clock operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, IFIL should be added. IDD2 subsystem clock operation includes the operational current of the real-time clock.
 - 4. Current flowing only to the 12-bit interval timer (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either IDD1 or IDD2, and IIT, when the 12-bit interval timer operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, IFIL should be added.
 - 5. Current flowing only to the watchdog timer (including the operating current of the low-speed on-chip oscillator). The supply current of the RL78 microcontrollers is the sum of IDD1, IDD2 or IDD3 and IWDT when the watchdog timer is in operation.
 - 6. Current flowing only to the A/D converter. The supply current of the RL78 microcontrollers is the sum of IDD1 or IDD2 and IADC when the A/D converter operates in an operation mode or the HALT mode.
 - 7. Current flowing only to the LVD circuit. The supply current of the RL78 microcontrollers is the sum of IDD1, IDD2 or IDD3 and ILVD when the LVD circuit is in operation.
 - 8. Current flowing only during data flash rewrite.
 - 9. Current flowing only during self programming.
 - **10.** For shift time to the SNOOZE mod.
 - 11. Current flowing only to the LCD controller/driver. The supply current value of the RL78 microcontrollers is the sum of the LCD operating current (ILCD1, ILCD2 or ILCD3) to the supply current (IDD1 or IDD2) when the LCD controller/driver operates in an operation mode or HALT mode. Not including the current that flows through the LCD panel.

The TYP. value and MAX. value are following conditions.

- When fsuB is selected for system clock, LCD clock = 128 Hz (LCDC0 = 07H)
- 4-Time-Slice, 1/3 Bias Method
- **12.** Not including the current that flows through the external divider resistor when the external resistance division method is used.
- Remarks 1. fil: Low-speed on-chip oscillator clock frequency
 - 2. fsub: Subsystem clock frequency (XT1 clock oscillation frequency)
 - 3. fcLK: CPU/peripheral hardware clock frequency
 - 4. Temperature condition of the TYP. value is T_A = 25°C



Minimum Instruction Execution Time during Main System Clock Operation





----- When the high-speed on-chip oscillator clock is selected

--- During self programming

---- When high-speed system clock is selected



(4) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode)

 $(T_A = -40 \text{ to } +85^{\circ}\text{C}, 1.8 \text{ V} \le \text{EV}_{DD} = \text{V}_{DD} \le 5.5 \text{ V}, \text{ V}_{SS} = \text{EV}_{SS} = 0 \text{ V})$

(1/2)

Parameter	Symbol		Conditions		HS (high main) l	n-speed Mode	LS (low main)	-speed Mode	LV (low- main)	-voltage Mode	Unit
						MAX.	MIN.	MAX.	MIN.	MAX.	Ť
Transfer rate		Reception	4.0 V \leq EV _{DD} \leq 5.5 V, 2.7 V \leq V _b \leq 4.0 V Theoretical value of the			fмск/6 Note 1		fмск/6 Note 1		fмск/6 Note 1	bps
				Theoretical value of the maximum transfer rate $f_{MCK} = f_{CLK}^{Note 3}$		4.0		1.3		0.6	Mbps
			$\begin{array}{l} 2.7 \ V \leq E V_{DD} < 4.0 \ V, \\ 2.3 \ V \leq V_b \leq 2.7 \ V \end{array}$			fмск/6 Note 1		fмск/6 Note 1		fмск/6 Note 1	bps
			Theoretical value of the maximum transfer rate $f_{MCK} = f_{CLK}$. Note 3			4.0		1.3		0.6	Mbps
			2.4 V ≤ EV 1.6 V ≤ V _b	′ _{DD} < 3.3 V, ≤ 2.0 V		fмск/6 Note 1		fмск/6 Note 1		fмск/6 Note 1	bps
				Theoretical value of the maximum transfer rate $f_{MCK} = f_{CLK}$ Note 3		4.0		1.3		0.6	Mbps
			$1.8 V \le EV_{DD} < 3.3 V,$ 1.6 V \le V_b \le 2.0 V					fMCK/6 Notes 1, 2		fMCK/6 Notes 1, 2	bps
				Theoretical value of the maximum transfer rate $f_{MCK} = f_{CLK}^{Note 3}$				1.3		0.6	Mbps

Notes 1. Transfer rate in the SNOOZE mode is 4800 bps only.

- **2.** Use it with $EV_{DD} \ge V_b$.
- 3. The maximum operating frequencies of the CPU/peripheral hardware clock (f_{CLK}) are:

 HS (high-speed main) mode:
 24 MHz $(2.7 V \le V_{DD} \le 5.5 V)$

 16 MHz $(2.4 V \le V_{DD} \le 5.5 V)$

 LS (low-speed main) mode:
 8 MHz $(1.8 V \le V_{DD} \le 5.5 V)$

 LV (low-voltage main) mode:
 4 MHz $(1.6 V \le V_{DD} \le 5.5 V)$

- Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance (32-pin to 52pin products)/EV_{DD} tolerance (64-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.
- **Remarks 1.** V_b[V]: Communication line voltage
 - 2. q: UART number (q = 0), g: PIM and POM number (g = 1)
 - fMCK: Serial array unit operation clock frequency (Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 01)

3. The smaller maximum transfer rate derived by using fMCK/6 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 2.7 V \leq EV_{DD} < 4.0 V and 2.3 V \leq V_b \leq 2.7 V

Maximum transfer rate = $\frac{1}{\{-C_b \times R_b \times \ln (1 - \frac{2.0}{V_b})\} \times 3}$ [bps]

Baud rate error (theoretical value) =
$$\frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

- * This value is the theoretical value of the relative difference between the transmission and reception sides.
- **4.** This value as an example is calculated when the conditions described in the "Conditions" column are met. Refer to Note 3 above to calculate the maximum transfer rate under conditions of the customer.
- 5. Use it with $EV_{DD} \ge V_b$.
- **6.** The smaller maximum transfer rate derived by using fMCK/6 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 1.8 V \leq EV_{DD} < 3.3 V and 1.6 V \leq V_b \leq 2.0 V

Maximum transfer rate =
$$\frac{1}{\{-C_b \times R_b \times \ln (1 - \frac{1.5}{V_b})\} \times 3}$$
 [bps]

Baud rate error (theoretical value) = $\frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 [\%]$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

- 7. This value as an example is calculated when the conditions described in the "Conditions" column are met. Refer to Note 6 above to calculate the maximum transfer rate under conditions of the customer.
- Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance (32-pin to 52pin products)/EV_{DD} tolerance (64-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.



(T _A = -40 to +85°0	C, 1.8 V ≤	$EV_{DD} = V_{DD} \le 5.5 V, V_{SS} = EV_{SS} = 0$	V)						(2/2)
Parameter	Symbol	Conditions		HS (high- speed main) mode		LS (low-speed main) mode		low- e main) ode	Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Delay time from SCKp↓ to SOp output ^{Note 5}	tkso2	$\begin{array}{l} 4.0 \; V \leq EV_{\text{DD}} \leq 5.5 \; V, 2.7 \; V \leq V_b \leq 4.0 \; V, \\ C_b = 30 \; pF, \; R_b = 1.4 \; k\Omega \end{array}$		2/fмск + 120		2/fмск + 573		2/fмск + 573	ns
		$\label{eq:VD} \begin{array}{l} 2.7 \ V \leq EV_{\text{DD}} < 4.0 \ V, \ 2.3 \ V \leq V_b \leq 2.7 \ V, \\ C_b = 30 \ pF, \ R_b = 2.7 \ k\Omega \end{array}$		2/fмск + 214		2/fмск + 573		2/fмск + 573	ns
		$\label{eq:V_def} \begin{array}{l} 2.4 \ V \leq EV_{\text{DD}} < 3.3 \ V, \ 1.6 \ V \leq V_b \leq 2.0 \ V, \\ C_b = 30 \ pF, \ R_b = 5.5 \ k\Omega \end{array}$		2/fмск + 573		2/fмск + 573		2/fмск + 573	ns
		$ \begin{split} & 1.8 \ V \leq EV_{DD} < 3.3 \ V, \\ & 1.6 \ V \leq V_b \leq 2.0 \ V^{\text{Note 2}}, \\ & C_b = 30 \ pF, \ R_b = 5.5 \ k\Omega \end{split} $				2/f _{мск} + 573		2/fмск + 573	ns

(7) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (slave mode, SCKp... external clock input)

Notes 1. Transfer rate in the SNOOZE mode : MAX. 1 Mbps

- **2.** Use it with $EV_{DD} \ge V_b$.
- **3.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp \downarrow " when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
- **4.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp \downarrow " when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
- 5. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp[↑]" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
- Caution Select the TTL input buffer for the SIp pin and SCKp pin and the N-ch open drain output (VDD tolerance (32-pin to 52-pin products)/EVDD tolerance (64-pin products)) mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For VIH and VIL, see the DC characteristics with TTL input buffer selected.

CSI mode connection diagram (during communication at different potential)



- **Remarks 1.** R_b[Ω]:Communication line (SOp) pull-up resistance, C_b[F]: Communication line (SOp) load capacitance, V_b[V]: Communication line voltage
 - p: CSI number (p = 00, 01), m: Unit number (m = 0), n: Channel number (n = 0, 1), g: PIM and POM number (g = 1)
 - **3.** fMCK: Serial array unit operation clock frequency

(Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 01))



CSI mode serial transfer timing (slave mode) (during communication at different potential) (When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)





Remark p: CSI number (p = 00, 01), m: Unit number (m = 0), n: Channel number (n = 0, 1), g: PIM and POM number (g = 1)

2.5.2 Serial interface IICA

(1) I^2C standard mode

(TA = -40 to +85°C, 1.6 V \leq EV_DD = V_DD \leq 5.5 V, Vss = EVss = 0 V)

Parameter	Symbol	(Conditions	HS (speed Mo	high- main) ode	LS (low main)	/-speed Mode	LV (voltage Mo	low- e main) ode	Unit
				MIN.	MAX.	MIN.	MIN.	MAX.	MIN.	
SCLA0 clock frequency	fscL	Standard	$2.7~V \leq EV_{\text{DD}} \leq 5.5~V$	0	100	0	100	0	100	kHz
			$2.4~V \leq EV_{\text{DD}} \leq 5.5~V$	0	100	0	100	0	100	
			$1.8~V \le EV_{\text{DD}} \le 5.5~V$			0	100	0	100	
			$1.6~V \le EV_{\text{DD}} \le 5.5~V$					0	100	
Setup time of restart condition	tsu:sta	$2.7 \text{ V} \leq \text{EV}_{\text{DD}} \leq 5.5 \text{ V}$		4.7		4.7		4.7		μs
		$2.4 \text{ V} \leq \text{EV}_{\text{DD}}$	≤ 5.5 V	4.7		4.7		4.7		
		$1.8 V \le EV_{DD}$	≤ 5.5 V			4.7		4.7		
		$1.6 V \le EV_{DD} \le$	≤ 5.5 V					4.7		
Hold time Note 1	thd:sta	$2.7 \text{ V} \leq \text{EV}_{\text{DD}}$	≤ 5.5 V	4.0		4.0		4.0		μs
		$2.4 \text{ V} \leq \text{EV}_{\text{DD}}$	≤ 5.5 V	4.0		4.0		4.0		
		$1.8 V \le EV_{DD}$	≤ 5.5 V			4.0		4.0		
		$1.6 V \le EV_{DD}$	≤ 5.5 V					4.0		
Hold time when SCLA0 = "L"	t LOW	$2.7 \text{ V} \leq EV_{DD}$	≤ 5.5 V	4.7		4.7		4.7		μs
		$2.4 \text{ V} \leq \text{EV}_{\text{DD}}$	≤ 5.5 V	4.7		4.7		4.7		
		$1.8 V \le EV_{DD}$	≤ 5.5 V			4.7		4.7		
		$1.6~V \leq EV_{\text{DD}} \leq 5.5~V$						4.7		
Hold time when SCLA0 = "H"	t ніgh	$2.7~V \leq EV_{\text{DD}} \leq 5.5~V$		4.0		4.0		4.0		μs
		$2.4 V \le EV_{DD}$	≤ 5.5 V	4.0		4.0		4.0		
		$1.8 V \le EV_{DD} \le$	≤ 5.5 V			4.0		4.0		
		$1.6 V \le EV_{DD} \le$	≤ 5.5 V					4.0		
Data setup time (reception)	tsu:dat	$2.7 V \le EV_{DD}$	≤ 5.5 V	250		250		250		ns
		$2.4 \text{ V} \le \text{EV}_{\text{DD}} \le$	≤ 5.5 V	250		250		250		
		$1.8 V \le EV_{DD} \le$	≤ 5.5 V			250		250		
		$1.6 V \le EV_{DD} \le$	≤ 5.5 V					250		
Data hold time (transmission) ^{Note 2}	thd:dat	$2.7 V \le EV_{DD} \le$	≤ 5.5 V	0	3.45	0	3.45	0	3.45	μs
		$2.4 V \le EV_{DD}$	≤ 5.5 V	0	3.45	0	3.45	0	3.45	
		$1.8 V \le EV_{DD} \le$	≤ 5.5 V			0	3.45	0	3.45	
		$1.6 V \le EV_{DD} \le$	≤ 5.5 V					0	3.45	
Setup time of stop condition	tsu:sto	$2.7 V \le EV_{DD} \le$	≤ 5.5 V	4.0		4.0		4.0		μs
		$2.4 \text{ V} \le \text{EV}_{\text{DD}} \le$	≤ 5.5 V	4.0		4.0		4.0		
		$1.8 V \le EV_{DD} \le$	≤ 5.5 V			4.0		4.0		
		$1.6 V \le EV_{DD}$	≤ 5.5 V					4.0		
Bus-free time	t BUF	$2.7 V \le EV_{DD} \le$	≤ 5.5 V	4.7		4.7		4.7		μs
		$2.4 V \le EV_{DD} \le$	≤ 5.5 V	4.7		4.7		4.7		
		$1.8 V \le EV_{DD}$	≤ 5.5 V			4.7		4.7		
		$1.6 V \le EV_{DD} \le$	≤ 5.5 V					4.7		

(Notes and Remark are listed on the next page.)

(3) I^2C fast mode plus

 $(T_A = -40 \text{ to } +85^{\circ}C, 1.6 \text{ V} \le EV_{DD} = V_{DD} \le 5.5 \text{ V}, \text{ Vss} = EV_{SS} = 0 \text{ V})$

Parameter	Symbol	Conditions	HS (hig main)	h-speed Mode	LS (low main)	/-speed Mode	LV (low main)	-voltage Mode	Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	fsc∟	Fast mode plus: $2.7 V \le EV_{DD} \le 5.5 V$ fclk \ge 10 MHz	0	1000	_	-	_	_	kHz
Setup time of restart condition	tsu:sta	$2.7 \text{ V} \leq \text{EV}_{\text{DD}} \leq 5.5 \text{ V}$	0.26		_	-	_	_	μs
Hold time ^{Note 1}	thd:sta	$2.7 \text{ V} \leq \text{EV}_{\text{DD}} \leq 5.5 \text{ V}$	0.26			-	_	_	μs
Hold time when SCLA0 = "L"	t∟ow	$2.7 \text{ V} \leq \text{EV}_{\text{DD}} \leq 5.5 \text{ V}$	0.5		—		—		μs
Hold time when SCLA0 = "H"	tнigн	$2.7 \text{ V} \leq \text{EV}_{\text{DD}} \leq 5.5 \text{ V}$	0.26		_	-	-	_	μs
Data setup time (reception)	tsu:dat	$2.7 \text{ V} \leq \text{EV}_{\text{DD}} \leq 5.5 \text{ V}$	50		_	_	-	_	μs
Data hold time (transmission) ^{Note 2}	thd:dat	$2.7 \text{ V} \leq \text{EV}_{\text{DD}} \leq 5.5 \text{ V}$	0	0.45	_	-	-	_	μs
Setup time of stop condition	tsu:sto	$2.7 \text{ V} \leq \text{EV}_{\text{DD}} \leq 5.5 \text{ V}$	0.26			_		_	μs
Bus-free time	tBUF	$2.7 \text{ V} \leq \text{EV}_{\text{DD}} \leq 5.5 \text{ V}$	0.5			_	_	_	μs

- Notes 1. The first clock pulse is generated after this period when the start/restart condition is detected.
 - 2. The maximum value (MAX.) of the during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.
- Caution The values in the above table are applied even when bit 2 (PIOR2) in the peripheral I/O redirection register (PIOR) is 1. At this time, the pin characteristics (IOH1, IOL1, VOH1, VOL1) must satisfy the values in the redirect destination.
- **Remark** The maximum value of Cb (communication line capacitance) and the value of Rb (communication line pull-up resistor) at that time in each mode are as follows.

Fast mode plus: C_b = 120 pF, R_b = 1.1 k Ω

IICA serial transfer timing





(4) When reference voltage (+) = Internal reference voltage (ADREFP1 = 1, ADREFP0 = 0), reference voltage (-) = AV_{REFM}/ANI1 (ADREFM = 1), target pin : ANI0, ANI16 to ANI23

 $(T_A = -40 \text{ to } +85^{\circ}\text{C}, 2.4 \text{ V} \le \text{EV}_{\text{DD}} = \text{V}_{\text{DD}} \le 5.5 \text{ V}, \text{ Vss} = \text{EV}_{\text{ss}} = 0 \text{ V}, \text{ Reference voltage (+)} = \text{V}_{\text{BGR}}^{\text{Note 3}}, \text{ Reference voltage (-)} = \text{AV}_{\text{REFM}}^{\text{Note 4}} = 0 \text{ V}, \text{ HS (high-speed main) mode)}$

Parameter	Symbol	Cond	itions	MIN.	TYP.	MAX.	Unit
Resolution	RES				8		bit
Conversion time	t CONV	8-bit resolution	$2.4~V \leq V \text{DD} \leq 5.5~V$	17		39	μs
Zero-scale error ^{Notes 1, 2}	Ezs	8-bit resolution	$2.4~V \leq V \text{DD} \leq 5.5~V$			±0.60	%FSR
Integral linearity error ^{Note 1}	ILE	8-bit resolution	$2.4~\text{V} \leq \text{V}\text{DD} \leq 5.5~\text{V}$			±2.0	LSB
Differential linearity error Note 1	DLE	8-bit resolution	$2.4~V \leq V \text{DD} \leq 5.5~V$			±1.0	LSB
Analog input voltage	VAIN			0		VBGR Note 3	V

Notes 1. Excludes quantization error ($\pm 1/2$ LSB).

- **2.** This value is indicated as a ratio (%FSR) to the full-scale value.
- 3. Refer to 2.6.2 Temperature sensor/internal reference voltage characteristics.
- **4.** When reference voltage (–) = Vss, the MAX. values are as follows.

Zero-scale error: Add $\pm 0.35\%$ FSR to the MAX. value when reference voltage (–) = AV_{REFM}. Integral linearity error: Add ± 0.5 LSB to the MAX. value when reference voltage (–) = AV_{REFM}. Differential linearity error: Add ± 0.2 LSB to the MAX. value when reference voltage (–) = AV_{REFM}.

2.6.2 Temperature sensor/internal reference voltage characteristics

•				•		
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Temperature sensor output voltage	VTMPS25	Setting ADS register = 80H, TA = +25°C		1.05		V
Internal reference voltage	VBGR	Setting ADS register = 81H	1.38	1.45	1.5	V
Temperature coefficient	Fvtmps	Temperature sensor that depends on the temperature		-3.6		mV/°C
Operation stabilization wait time	tamp		5			μs

$(T_A = -40 \text{ to } +85^{\circ}\text{C}, 2.4 \text{ V} \le \text{EV}_{DD} = \text{V}_{DD} \le 5.5 \text{ V}, \text{V}_{SS} = \text{EV}_{SS} = 0 \text{ V})$ (HS (high-speed main) mode)



<R>

2.8 RAM Data Retention Characteristics

(T_A = -40 to +85°C, Vss = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	VDDDR		1.46 ^{Note}		5.5	V

<R> Note This depends on the POR detection voltage. For a falling voltage, data in RAM are retained until the voltage reaches the level that triggers a POR reset but not once it reaches the level at which a POR reset is generated.



2.9 Flash Memory Programming Characteristics

$(T_A = -40 \text{ to } +85^{\circ}\text{C}, 1.8 \text{ V} \le \text{EV}_{\text{DD}} = \text{V}_{\text{DD}} \le 5.5 \text{ V}, \text{V}_{\text{SS}} = \text{EV}_{\text{SS}} = 0 \text{ V})$

	Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
	System clock frequency	fclĸ	$1.8 \text{ V} \leq \text{Vdd} \leq 5.5 \text{ V}$	1		24	MHz
<r></r>	Number of code flash rewrites Note 1, 2, 3	Cerwr	Retained for 20 years T _A = 85°C	1,000			Times
<r></r>	Number of data flash rewrites Note 1, 2, 3		Retained for 1 year $T_A = 25^{\circ}C$		1,000,000		
<r></r>			Retained for 5 years $T_A = 85^{\circ}C$	100,000			
<r></r>			Retained for 20 years $T_A = 85^{\circ}C$	10,000			

Notes 1. 1 erase + 1 write after the erase is regarded as 1 rewrite.

- The retaining years are until next rewrite after the rewrite.
- 2. When using flash memory programmer and Renesas Electronics self programming library
- 3. This characteristic indicates the flash memory characteristic and based on Renesas Electronics reliability test.

Remark When updating data multiple times, use the flash memory as one for updating data.

2.10 Dedicated Flash Memory Programmer Communication (UART)

$(T_A = -40 \text{ to } +85^{\circ}C, 1.8 \text{ V} \le EV_{DD} = V_{DD} \le 5.5 \text{ V}, \text{ Vss} = EV_{SS} = 0 \text{ V})$

Parameter	Symbol	Conditions		TYP.	MAX.	Unit
Transfer rate		During flash memory programming	115,200		1,000,000	bps



Absolute Maximum Ratings (T_A = 25°C)

(3/3)

Parameter	Symbols		Conditions	Ratings	Unit
Output current, high	Іон1	Per pin	P10 to P17, P30 to P32, P40 to P43, P50 to P54, P70 to P74, P120, P125 to P127, P130, P140 to P147	-40	mA
		Total of all pins –170 mA	P10 to P14, P40 to P43, P120, P130, P140 to P147	-70	mA
			P15 to P17, P30 to P32, P50 to P54, P70 to P74, P125 to P127	-100	mA
	Іон2	Per pin	P20, P21	-0.5	mA
		Total of all pins		–1	mA
Output current, low	lo∟1	Per pin	P10 to P17, P30 to P32, P40 to P43, P50 to P54, P60, P61, P70 to P74, P120, P125 to P127, P130, P140 to P147	40	mA
		Total of all pins 170 mA	P10 to P14, P40 to P43, P120, P130, P140 to P147	70	mA
			P15 to P17, P30 to P32, P50 to P54, P60, P61, P70 to P74, P125 to P127	100	mA
	IOL2	Per pin	P20, P21	1	mA
		Total of all pins		2	mA
Operating ambient	TA	In normal operation	on mode	-40 to +105	°C
temperature		In flash memory p	programming mode		
Storage temperature	Tstg			-65 to +150	°C

- Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.
- **Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.



3.2 Oscillator Characteristics

3.2.1 X1, XT1 oscillator characteristics

$(T_A = -40 \text{ to } +105^{\circ}C, 2.4 \text{ V} \le EV_{DD} = V_{DD} \le 5.5 \text{ V}, \text{ Vss} = EV_{SS} = 0 \text{ V})$
--

Parameter	Resonator	Conditions	MIN.	TYP.	MAX.	Unit
X1 clock oscillation	Ceramic resonator/	$2.7~V \leq V_{\text{DD}} \leq 5.5~V$	1.0		20.0	MHz
frequency (fx) ^{Note}	crystal resonator	$2.4~V \leq V_{\text{DD}} < 2.7~V$	1.0		16.0	MHz
XT1 clock oscillation frequency (f _{XT}) ^{Note}	Crystal resonator		32	32.768	35	kHz

- **Note** Indicates only permissible oscillator frequency ranges. Refer to **3.4 AC Characteristics** for instruction execution time. Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.
- Caution Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.

3.2.2 On-chip oscillator characteristics

$(T_A = -40 \text{ to } +105^{\circ}\text{C}, 2.4 \text{ V} \le \text{EV}_{\text{DD}} = \text{V}_{\text{DD}} \le 5.5 \text{ V}, \text{V}_{\text{SS}} = \text{EV}_{\text{SS}} = 0 \text{ V})$

Oscillators	Parameters	Conditions			TYP.	MAX.	Unit
High-speed on-chip oscillator clock frequency Notes 1, 2	fін			1		24	MHz
High-speed on-chip oscillator clock frequency accuracy		–20 to +85°C	$2.4~V \leq V_{\text{DD}} \leq 5.5~V$	-1		+1	%
		–40 to –20°C	$2.4~V \leq V_{\text{DD}} \leq 5.5~V$	-1.5		+1.5	%
		+85 to +105°C	$2.4~V \leq V_{\text{DD}} \leq 5.5~V$	-2.0		+2.0	%
Low-speed on-chip oscillator clock frequency	fı∟				15		kHz
Low-speed on-chip oscillator clock frequency accuracy				-15		+15	%

Notes 1. High-speed on-chip oscillator frequency is selected by bits 0 to 3 of option byte (000C2H) and bits 0 to 2 of HOCODIV register.

2. This indicates the oscillator characteristics only. Refer to 3.4 AC Characteristics for instruction execution time.



(4) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (1/2) (T_A = -40 to +105°C, 2.4 V \leq EV_{DD} = V_{DD} \leq 5.5 V, V_{SS} = EV_{SS} = 0 V)

Parameter	Symbol		Conditions			ed main) Mode	Unit
					MIN.	MAX.	
Transfer rate		Reception	$4.0~V \leq EV_{\text{DD}} \leq 5.5~V,$			fмск/12 ^{Note 1}	bps
			$\begin{array}{l} 2.7 \ V \leq V_b \leq 4.0 \ V \\ \\ \hline \\ 2.7 \ V \leq EV_{DD} < 4.0 \ V, \\ \\ 2.3 \ V \leq V_b \leq 2.7 \ V \end{array}$	Theoretical value of the maximum transfer rate $f_{MCK} = f_{CLK}^{Note 2}$		2.0	Mbps
						fмск/12 ^{Note 1}	bps
				Theoretical value of the maximum transfer rate $f_{MCK} = f_{CLK}^{Note 2}$		2.0	Mbps
			$\begin{array}{l} 2.4 \ V \leq EV_{\text{DD}} < 3.3 \ V, \\ 1.6 \ V \leq V_{\text{b}} \leq 2.0 \ V \end{array}$			f _{MCK} /12 Note 1	bps
				Theoretical value of the maximum transfer rate $f_{MCK} = f_{CLK}^{Note 2}$		2.0	Mbps

Notes 1. Transfer rate in the SNOOZE mode is 4800 bps only.

- 2. The maximum operating frequencies of the CPU/peripheral hardware clock (fcLk) are:
HS (high-speed main) mode:24 MHz (2.7 V \leq VDD \leq 5.5 V)16 MHz (2.4 V \leq VDD \leq 5.5 V)
- Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (VDD tolerance (32- to 52-pin products)/EVDD tolerance (64-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For VIH and VIL, see the DC characteristics with TTL input buffer selected.
- **Remarks 1.** V_b[V]: Communication line voltage
 - **2.** q: UART number (q = 0), g: PIM and POM number (g = 1)
 - fMCK: Serial array unit operation clock frequency (Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 01)



- Notes 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.
 - **2.** When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
- Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance (32- to 52-pin products)/EV_{DD} tolerance (64-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

CSI mode connection diagram (during communication at different potential)



- Remarks 1. Rb[Ω]:Communication line (SCKp, SOp) pull-up resistance,

 Cb[F]: Communication line (SCKp, SOp) load capacitance, Vb[V]: Communication line voltage
 - 2. p: CSI number (p = 00, 01), m: Unit number (m = 0), n: Channel number (n = 0, 1), g: PIM and POM number (g = 1)
 - **3.** fmcκ: Serial array unit operation clock frequency (Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00))



(4) When reference voltage (+) = Internal reference voltage (ADREFP1 = 1, ADREFP0 = 0), reference voltage (-) = AVREFM/ANI1 (ADREFM = 1), target pin : ANI0, ANI16 to ANI23

$(T_A = -40 \text{ to } +105^{\circ}\text{C}, 2.4 \text{ V} \le \text{EV}_{\text{DD}} = \text{V}_{\text{DD}} \le 5.5 \text{ V}, \text{ V}_{\text{SS}} = \text{EV}_{\text{SS}} = 0 \text{ V}, \text{ Reference voltage (+)} = \text{V}_{\text{BGR}}^{\text{Note 3}}, \text{ Reference voltage (-)} = \text{AV}_{\text{REFM}}^{\text{Note 4}} = 0 \text{ V}, \text{ HS (high-speed main) mode)}$

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES				8		bit
Conversion time	t CONV	8-bit resolution	$2.4~V \leq V \text{DD} \leq 5.5~V$	17		39	μs
Zero-scale error ^{Notes 1, 2}	Ezs	8-bit resolution	$2.4~V \leq V \text{DD} \leq 5.5~V$			±0.60	%FSR
Integral linearity error ^{Note 1}	ILE	8-bit resolution	$2.4~\text{V} \leq \text{V}\text{DD} \leq 5.5~\text{V}$			±2.0	LSB
Differential linearity error Note 1	DLE	8-bit resolution	$2.4~V \leq V \text{DD} \leq 5.5~V$			±1.0	LSB
Analog input voltage	VAIN			0		VBGR Note 3	V

Notes 1. Excludes quantization error ($\pm 1/2$ LSB).

- **2.** This value is indicated as a ratio (%FSR) to the full-scale value.
- 3. Refer to 3.6.2 Temperature sensor/internal reference voltage characteristics.
- **4.** When reference voltage (-) = Vss, the MAX. values are as follows.

Zero-scale error: Add $\pm 0.35\%$ FSR to the MAX. value when reference voltage (–) = AV_{REFM}. Integral linearity error: Add ± 0.5 LSB to the MAX. value when reference voltage (–) = AV_{REFM}. Differential linearity error: Add ± 0.2 LSB to the MAX. value when reference voltage (–) = AV_{REFM}.



3.6.4 LVD circuit characteristics

(TA = -40 to +105°C, VPDR \leq EVDD = VDD \leq 5.5 V, Vss = EVss = 0 V)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection	Supply voltage level	VLVD0	Power supply rise time	3.90	4.06	4.22	V
voltage			Power supply fall time	3.83	3.98	4.13	V
		VLVD1	Power supply rise time	3.60	3.75	3.90	V
			Power supply fall time	3.53	3.67	3.81	V
		VLVD2	Power supply rise time	3.01	3.13	3.25	V
			Power supply fall time	2.94	3.06	3.18	V
		VLVD3	Power supply rise time	2.90	3.02	3.14	V
			Power supply fall time	2.85	2.96	3.07	V
		VLVD4	Power supply rise time	2.81	2.92	3.03	V
			Power supply fall time	2.75	2.86	2.97	V
		VLVD5	Power supply rise time	2.70	2.81	2.92	V
			Power supply fall time	2.64	2.75	2.86	V
		VLVD6	Power supply rise time	2.61	2.71	2.81	V
			Power supply fall time	2.55	2.65	2.75	V
		VLVD7	Power supply rise time	2.51	2.61	2.71	V
			Power supply fall time	2.45	2.55	2.65	V
Minimum puls	Minimum pulse width			300			μs
Detection del	ay time					300	μs

LVD Detection Voltage of Interrupt & Reset Mode

$(T_A = -40 \text{ to } +105^{\circ}\text{C}, V_{PDR} \le EV_{DD} = V_{DD} \le 5.5 \text{ V}, V_{SS} = EV_{SS} = 0 \text{ V})$

Parameter	Symbol		Conditions			TYP.	MAX.	Unit
Interrupt and reset	VLVDD0	Vpoc2,	VPOC2, VPOC1, VPOC0 = 0, 1, 1, falling reset voltage		2.64	2.75	2.86	V
mode	VLVDD1		LVIS1, LVIS0 = 1, 0	Rising release reset voltage	2.81	2.92	3.03	V
				Falling interrupt voltage	2.75	2.86	2.97	V
	VLVDD2		LVIS1, LVIS0 = 0, 1	Rising release reset voltage	2.90	3.02	3.14	V
				Falling interrupt voltage	2.85	2.96	3.07	V
	VLVDD3		LVIS1, LVIS0 = 0, 0	Rising release reset voltage	3.90	4.06	4.22	V
				Falling interrupt voltage	3.83	3.98	4.13	V

3.6.5 Power supply voltage rising slope characteristics

$(T_A = -40 \text{ to } +105^{\circ}\text{C}, \text{Vss} = 0 \text{ V})$

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power supply voltage rising slope	SVDD				54	V/ms

Caution Make sure to keep the internal reset state by the LVD circuit or an external reset until V_{DD} reaches the operating voltage range shown in 31.4 AC Characteristics.

4.2 44-pin Products

R5F10RF8AFP, R5F10RFAAFP, R5F10RFCAFP R5F10RF8GFP, R5F10RFAGFP, R5F10RFCGFP

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LQFP44-10x10-0.80	PLQP0044GC-A	P44GB-80-UES-2	0.36



NOTE

Each lead centerline is located within 0.20 mm of its true position at maximum material condition.

© 2012 Renesas Electronics Corporation. All rights reserved.

у

ZD

ZE

0.10

1.00

1.00



R5F10RLAAFB, R5F10RLCAFB R5F10RLAGFB, R5F10RLCGFB



Each lead centerline is located within 0.08 mm of its true position at maximum material condition.

©2012 Renesas Electronics Corporation. All rights reserved.



		Description			
Rev.	Date	Page	Summary		
2.00	Jan 10, 2014	35	Modification of table in 2.4 AC Characteristics		
		36	Addition of Minimum Instruction Execution Time during Main System Clock Operation		
		37	Modification of AC Timing Test Points and External System Clock Timing		
		39	Modification of AC Timing Test Points		
		39	Modification of description, notes 1 and 2 in (1) During communication at same potential (UART mode)		
		41, 42	Modification of description, remark 2 in (2) During communication at same potential (CSI mode)		
		42, 43	Modification of description in (3) During communication at same potential (CSI mode)		
		45	Modification of description, notes 1 and 3, and remark 3 in (4) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (1/2)		
		46, 48	Modification of description, and remark 3 in (4) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (2/2)		
		49, 50	Modification of table, and note 1, caution, and remark 3 in (5) Communication at different potential (2.5 V, 3 V) (CSI mode)		
		51	Modification of table and note in (6) Communication at different potential (1.8 V, 2.5 V, 3 V) (1/3)		
		52	Modification of table and notes 1 to 3 in (6) Communication at different potential (1.8 V, 2.5 V, 3 V) (2/3)		
		53, 54	Modification of table, note 3, and remark 3 in (6) Communication at different potential (1.8 V, 2.5 V, 3 V) (3/3)		
		56	Modification of table in (7) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (1/2)		
		57	Modification of table in (7) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (2/2)		
		59, 60	Addition of (1) I ² C standard mode		
		61	Addition of (2) I ² C fast mode		
		62	Addition of (3) I ² C fast mode plus		
		63	Addition of table in 2.6.1 A/D converter characteristics		
		63, 64	Modification of description and notes 3 to 5 in 2.6.1 (1)		
		65	Modification of description, notes 3 and 4 in 2.6.1 (2)		
		67	Modification of description, notes 3 and 4 in 2.6.1 (3)		
		67	Modification of the table in 2.6.2 Temperature sensor/internal reference voltage		
		07	characteristics		
		68	Modification of the table and note in 2.6.3 POR circuit characteristics		
		70	Modification of the table of LVD Detection Voltage of Interrupt & Reset Mode		
		70	Modification from V_{DD} rise slope to Power supply voltage rising slope in 2.6.5 Supply voltage rise time		
		75	Modification of description in 2.10 Dedicated Flash Memory Programmer Communication (UART)		
		76	Modification of the figure in 2.11 Timing Specifications for Switching Flash Memory Programming Modes		
		77 to 126	Addition of products for industrial applications (G: T _A = -40 to +105°C)		
		127 to 133	Addition of product names for industrial applications (G: $T_A = -40$ to $+105^{\circ}C$)		
2.10	Sep 30, 2016	5	Modification of pin configuration in 1.3.1 32-pin products		
		6	Modification of pin configuration in 1.3.2 44-pin products		
		7	Modification of pin configuration in 1.3.3 48-pin products		
		δ 0 10	Modification of pin configuration in 1.3.4 52-pin products		
		9, 10	Modification of phil conliguration in 1.5.5 64-phil products		
		74	Modification of title of 2.8 RAM Data Retention Characteristics Note and figure		
		74	Modification of table of 2.9 Flash Memory Programming Characteristics		
		123	Modification of title of 3.8 RAM Data Retention Characteristics. Note, and figure		
		123	Modification of table of 3.9 Flash Memory Programming Characteristics and addition of Note 4		
		131	Modification of 4.5 64-pin Products		