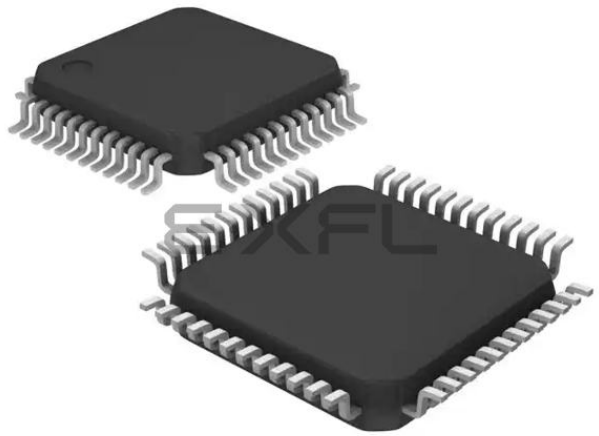
# Renesas Electronics America Inc - R5F10RGCGFB#X0 Datasheet



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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | RL78 |
| Core Size | 16-Bit |
| Speed | 24MHz |
| Connectivity | CSI, I²C, LINbus, UART/USART |
| Peripherals | DMA, LCD, LVD, POR, PWM, WDT |
| Number of I/O | 33 |
| Program Memory Size | 32KB (32K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 2K x 8 |
| RAM Size | 1.5K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.6V ~ 5.5V |
| Data Converters | A/D 9x8/10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 48-LQFP |
| Supplier Device Package | 48-LFQFP (7x7) |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f10rgcgfb-x0 |

### 1.3.4 52-pin products

- 52-pin plastic LQFP (10 × 10)

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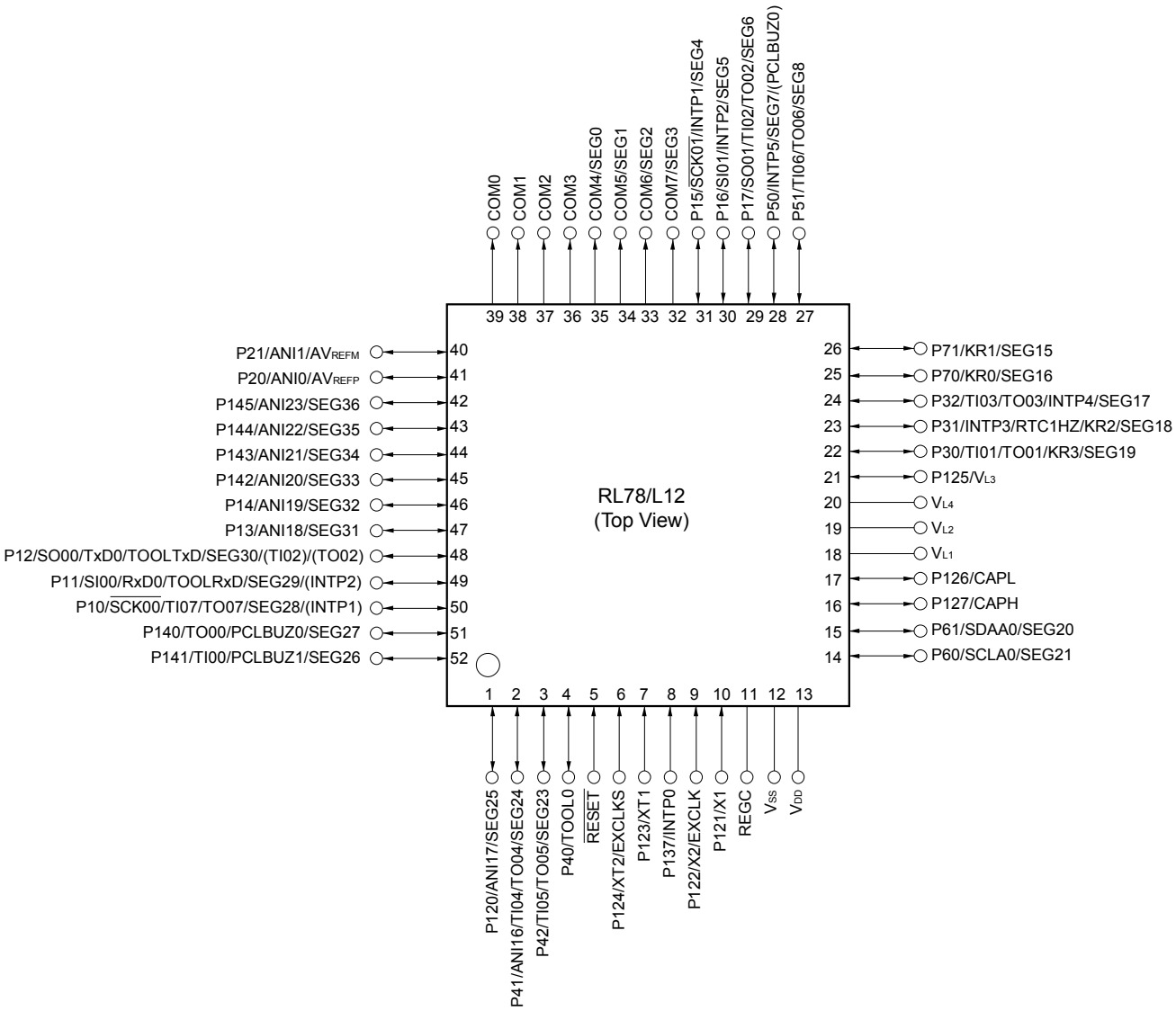



**Caution Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).**

**Remarks 1.** For pin identification, see **1.4 Pin Identification**.

**2.** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

## 2.1 Absolute Maximum Ratings

**Absolute Maximum Ratings ($T_A$ = 25°C) (1/3)**

| Parameter | Symbols | Conditions | Ratings | Unit |
|---|---|---|---|---|
| Supply voltage | $V_{DD}$ | $V_{DD}$ = $EV_{DD}$ | –0.5 to +6.5 | V |
| | $EV_{DD}$ | $V_{DD}$ = $EV_{DD}$ | –0.5 to +6.5 | V |
| | $EV_{SS}$ | | –0.5 to +0.3 | V |
| REGC pin input voltage | $V_{IREGC}$ | REGC | –0.3 to +2.8 and –0.3 to $V_{DD}$ + 0.3 Note 1 | V |
| Input voltage | $V_{I1}$ | P10 to P17, P30 to P32, P40 to P43, P50 to P54, P70 to P74, P120, P125 to P127,P140 to P147 | –0.3 to $EV_{DD}$ +0.3 and –0.3 to $V_{DD}$ + 0.3 Note 2 | V |
| | $V_{I2}$ | P60, P61 (N-ch open-drain) | –0.3 to $EV_{DD}$ +0.3 and –0.3 to $V_{DD}$ + 0.3 Note 2 | V |
| | $V_{I3}$ | P20, P21, P121 to P124, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$ | –0.3 to $V_{DD}$ + 0.3 Note 2 | V |
| Output voltage | $V_{O1}$ | P10 to P17, P30 to P32, P40 to P43, P50 to P54, P60, P61, P70 to P74, P120, P125 to P127, P130, P140 to P147 | –0.3 to $EV_{DD}$ + 0.3 and –0.3 to $V_{DD}$ + 0.3 Note 2 | V |
| | $V_{O2}$ | P20, P21 | –0.3 to $V_{DD}$ + 0.3 Note 2 | V |
| Analog input voltage | $V_{AI1}$ | ANI16 to ANI23 | –0.3 to $EV_{DD}$ + 0.3 and –0.3 to $AV_{REF(+)}$ + 0.3 Notes 2, 3 | V |
| | $V_{AI2}$ | ANI0, ANI1 | –0.3 to $V_{DD}$ + 0.3 and –0.3 to $AV_{REF(+)}$ + 0.3 Notes 2, 3 | V |

**Notes 1.** Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.

**2.** Must be 6.5 V or lower.

**3.** Do not exceed $AV_{REF(+)}$ + 0.3 V in case of A/D conversion target pin.

**Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.**

**Remarks 1.** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

**2.** $AV_{REF(+)}$ : + side reference voltage of the A/D converter.

**3.** $V_{SS}$ : Reference voltage

**Absolute Maximum Ratings ($T_A$ = 25°C) (3/3)**

| Parameter | Symbols | Conditions | | Ratings | Unit |
|---|---|---|---|---|---|
| Output current, high | $I_{OH1}$ | Per pin | P10 to P17, P30 to P32, P40 to P43, P50 to P54, P70 to P74, P120, P125 to P127, P130, P140 to P147 | −40 | mA |
| | | Total of all pins −170 mA | P10 to P14, P40 to P43, P120, P130, P140 to P147 | −70 | mA |
| | | | P15 to P17, P30 to P32, P50 to P54, P70 to P74, P125 to P127 | −100 | mA |
| | $I_{OH2}$ | Per pin | P20, P21 | −0.5 | mA |
| | | Total of all pins | | −1 | mA |
| Output current, low | $I_{OL1}$ | Per pin | P10 to P17, P30 to P32, P40 to P43, P50 to P54, P60, P61, P70 to P74, P120, P125 to P127, P130, P140 to P147 | 40 | mA |
| | | Total of all pins 170 mA | P10 to P14, P40 to P43, P120, P130, P140 to P147 | 70 | mA |
| | | | P15 to P17, P30 to P32, P50 to P54, P60, P61, P70 to P74, P125 to P127 | 100 | mA |
| | $I_{OL2}$ | Per pin | P20, P21 | 1 | mA |
| | | Total of all pins | | 2 | mA |
| Operating ambient temperature | $T_A$ | In normal operation mode | | −40 to +85 | °C |
| | | In flash memory programming mode | | | |
| Storage temperature | $T_{stg}$ | | | −65 to +150 | °C |

**Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.**

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

## 2.2 Oscillator Characteristics

### 2.2.1 X1, XT1 oscillator characteristics

**($T_A$ = –40 to +85°C, 1.6 V ≤ $EV_{DD}$ = $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS}$ = 0 V)**

| Parameter | Resonator | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| X1 clock oscillation frequency ($f_X$)Note | Ceramic resonator/ crystal resonator | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 1.0 | | 20.0 | MHz |
| | | 2.4 V ≤ $V_{DD}$ ≤ 2.7 V | 1.0 | | 16.0 | MHz |
| | | 1.8 V ≤ $V_{DD}$ < 2.7 V | 1.0 | | 8.0 | MHz |
| | | 1.6 V ≤ $V_{DD}$ <1.8 V | 1.0 | | 4.0 | MHz |
| XT1 clock oscillation frequency ($f_{XT}$)Note | Crystal resonator | | 32 | 32.768 | 35 | kHz |

**Note** Indicates only permissible oscillator frequency ranges. Refer to **2.4 AC Characteristics** for instruction execution time. Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

**Caution Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.**

### 2.2.2 On-chip oscillator characteristics

**($T_A$ = –40 to +85°C, 1.6 V ≤ $EV_{DD}$ = $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS}$ = 0 V)**

| Oscillators | Parameters | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| High-speed on-chip oscillator clock frequency Notes 1, 2 | $f_{IH}$ | | | 1 | | 24 | MHz |
| High-speed on-chip oscillator clock frequency accuracy | | –20 to +85°C | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V | –1 | | +1 | % |
| | | | 1.6 V ≤ $V_{DD}$ < 1.8 V | –5 | | +5 | % |
| | | –40 to –20°C | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V | –1.5 | | +1.5 | % |
| | | | 1.6 V ≤ $V_{DD}$ < 1.8 V | –5.5 | | +5.5 | % |
| Low-speed on-chip oscillator clock frequency | $f_{IL}$ | | | | 15 | | kHz |
| Low-speed on-chip oscillator clock frequency accuracy | | | | –15 | | +15 | % |

**Notes 1.** High-speed on-chip oscillator frequency is selected by bits 0 to 3 of option byte (000C2H) and bits 0 to 2 of HOCODIV register.

**2.** This indicates the oscillator characteristics only. Refer to **2.4 AC Characteristics** for instruction execution time.

## 2.3 DC Characteristics

### 2.3.1 Pin characteristics

**($T_A$ = –40 to +85°C, 1.6 V ≤ $EV_{DD}$ = $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS}$ = 0 V) (1/5)**

| Items | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Output current, high[Note 1] | $I_{OH1}$ | Per pin for P10 to P17, P30 to P32, P40 to P43, P50 to P54, P70 to P74, P120, P125 to P127, P130, P140 to P147 | | | | –10.0 [Note 2] | mA |
| | | Total of P10 to P14, P40 to P43, P120, P130, P140 to P147 (When duty = 70% [Note 3]) | 4.0 V ≤ $EV_{DD}$ ≤ 5.5 V | | | –40.0 | mA |
| | | | 2.7 V ≤ $EV_{DD}$ < 4.0 V | | | –8.0 | mA |
| | | | 1.8 V ≤ $EV_{DD}$ < 2.7 V | | | –4.0 | mA |
| | | | 1.6 V ≤ $EV_{DD}$ < 1.8 V | | | –2.0 | mA |
| | | Total of P15 to P17, P30 to P32, P50 to P54, P70 to P74, P125 to P127 (When duty = 70% [Note 3]) | 4.0 V ≤ $EV_{DD}$ ≤ 5.5 V | | | –60.0 | mA |
| | | | 2.7 V ≤ $EV_{DD}$ < 4.0 V | | | –15.0 | mA |
| | | | 1.8 V ≤ $EV_{DD}$ < 2.7 V | | | –8.0 | mA |
| | | | 1.6 V ≤ $EV_{DD}$ < 1.8 V | | | –4.0 | mA |
| | | Total of all pins (When duty = 70% [Note 3]) | | | | –100.0 | mA |
| | $I_{OH2}$ | P20, P21 | Per pin | | | –0.1 | mA |
| | | | Total of all pins | 1.6 V ≤ $V_{DD}$ ≤ 5.5 V | | –0.2 | mA |

**Notes 1.** Value of current at which the device operation is guaranteed even if the current flows from the $V_{DD}$ and $EV_{DD}$ pins to an output pin.

**2.** Do not exceed the total current value.

**3.** Specification under conditions where the duty factor ≤ 70%.
The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = ($I_{OH}$ × 0.7)/(n × 0.01)

<Example> Where n = 80% and $I_{OH}$ = –40.0 mA

Total output current of pins = (–40.0 × 0.7)/(80 × 0.01) ≅ –35.0 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

**Caution P10, P12, P15, and P17 do not output high level in N-ch open-drain mode.**

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

**($T_A$ = –40 to +85°C, 1.6 V ≤ $EV_{DD}$ = $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS}$ = 0 V) (3/5)**

| Items | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Input voltage, high | $V_{IH1}$ | P10 to P17, P30 to P32, P40 to P43, P50 to P54, P70 to P74, P120, P125 to P127, P140 to P147 | Normal input buffer | 0.8$EV_{DD}$ | | $EV_{DD}$ | V |
| | $V_{IH2}$ | P10, P11, P15, P16 | TTL input buffer 4.0 V ≤ $EV_{DD}$ ≤ 5.5 V | 2.2 | | $EV_{DD}$ | V |
| | | | TTL input buffer 3.3 V ≤ $EV_{DD}$ < 4.0 V | 2.0 | | $EV_{DD}$ | V |
| | | | TTL input buffer 1.6 V ≤ $EV_{DD}$ < 3.3 V | 1.50 | | $EV_{DD}$ | V |
| | $V_{IH3}$ | P20, P21 | | 0.7$V_{DD}$ | | $V_{DD}$ | V |
| | $V_{IH4}$ | P60, P61 | | 0.7$EV_{DD}$ | | $EV_{DD}$ | V |
| | $V_{IH5}$ | P121 to P124, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$ | | 0.8$V_{DD}$ | | $V_{DD}$ | V |
| Input voltage, low | $V_{IL1}$ | P10 to P17, P30 to P32, P40 to P43, P50 to P54, P70 to P74, P120, P125 to P127, P140 to P147 | Normal input buffer | 0 | | 0.2$EV_{DD}$ | V |
| | $V_{IL2}$ | P10, P11, P15, P16 | TTL input buffer 4.0 V ≤ $EV_{DD}$ ≤ 5.5 V | 0 | | 0.8 | V |
| | | | TTL input buffer 3.3 V ≤ $EV_{DD}$ < 4.0 V | 0 | | 0.5 | V |
| | | | TTL input buffer 1.6 V ≤ $EV_{DD}$ < 3.3 V | 0 | | 0.32 | V |
| | $V_{IL3}$ | P20, P21 | | 0 | | 0.3$V_{DD}$ | V |
| | $V_{IL4}$ | P60, P61 | | 0 | | 0.3$EV_{DD}$ | V |
| | $V_{IL5}$ | P121 to P124, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$ | | 0 | | 0.2$V_{DD}$ | V |

**Caution The maximum value of $V_{IH}$ of P10, P12, P15, P17 is $EV_{DD}$, even in the N-ch open-drain mode.**

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

## 2.4 AC Characteristics

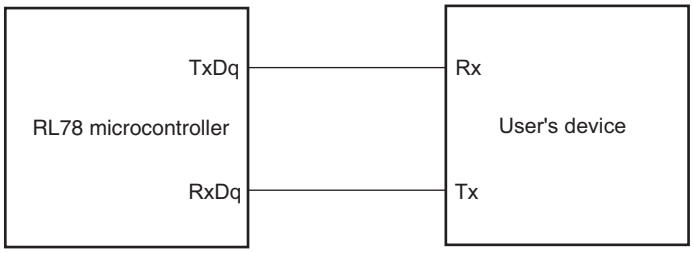
### 2.4.1 Basic operation

**($T_A$ = –40 to +85°C, 1.6 V ≤ $EV_{DD}$ = $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS}$ = 0 V)**

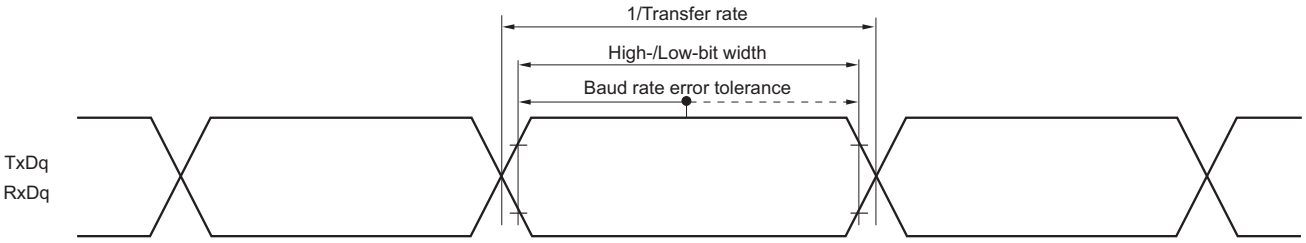
| Items | Symbol | Conditions | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|
| Instruction cycle (minimum instruction execution time) | $T_{CY}$ | Main system clock ($f_{MAIN}$) operation | HS (high-speed main) mode | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 0.04167 | | 1 | μs |
| | | | | 2.4 V ≤ $V_{DD}$ < 2.7 V | 0.0625 | | 1 | μs |
| | | | LV (low voltage main) mode | 1.6 V ≤ $V_{DD}$ ≤ 5.5 V | 0.25 | | 1 | μs |
| | | | LS (low-speed main) mode | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V | 0.125 | | 1 | μs |
| | | Subsystem clock ($f_{SUB}$) operation | | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V | 28.5 | 30.5 | 31.3 | μs |
| | | In the self programming mode | HS (high-speed main) mode | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 0.04167 | | 1 | μs |
| | | | | 2.4 V ≤ $V_{DD}$ < 2.7 V | 0.0625 | | 1 | μs |
| | | | LV (low voltage main) mode | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V | 0.25 | | 1 | μs |
| | | | LS (low-speed main) mode | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V | 0.125 | | 1 | μs |
| External main system clock frequency | $f_{EX}$ | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | | | 1.0 | | 20.0 | MHz |
| | | 2.4 V ≤ $V_{DD}$ < 2.7 V | | | 1.0 | | 16.0 | MHz |
| | | 1.8 V ≤ $V_{DD}$ < 2.4 V | | | 1.0 | | 8.0 | MHz |
| | | 1.6 V ≤ $V_{DD}$ < 1.8 V | | | 1.0 | | 4.0 | MHz |
| | $f_{EXS}$ | | | | 32 | | 35 | kHz |
| External main system clock input high-level width, low-level width | $t_{EXH}$, $t_{EXL}$ | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | | | 24 | | | ns |
| | | 2.4 V ≤ $V_{DD}$ < 2.7 V | | | 30 | | | ns |
| | | 1.8 V ≤ $V_{DD}$ < 2.4 V | | | 60 | | | ns |
| | | 1.6 V ≤ $V_{DD}$ < 1.8 V | | | 120 | | | ns |
| | $t_{EXHS}$, $t_{EXLS}$ | | | | 13.7 | | | μs |
| TI00 to TI07 input high-level width, low-level width | $t_{TIH}$, $t_{TIL}$ | | | | 1/$f_{MCK}$+10 | | | ns |
| TO00 to TO07 output frequency | $f_{TO}$ | HS (high-speed main) mode | | 4.0 V ≤ $EV_{DD}$ ≤ 5.5 V | | | 16 | MHz |
| | | | | 2.7 V ≤ $EV_{DD}$ < 4.0 V | | | 8 | MHz |
| | | | | 2.4 V ≤ $EV_{DD}$ < 2.7 V | | | 4 | MHz |
| | | LS (low-speed main) mode | | 1.8 V ≤ $EV_{DD}$ ≤ 5.5 V | | | 4 | MHz |
| | | LV (low voltage main) mode | | 1.6 V ≤ $EV_{DD}$ ≤ 5.5 V | | | 2 | MHz |
| PCLBUZ0, PCLBUZ1 output frequency | $f_{PCL}$ | HS (high-speed main) mode | | 4.0 V ≤ $EV_{DD}$ ≤ 5.5 V | | | 16 | MHz |
| | | | | 2.7 V ≤ $EV_{DD}$ < 4.0 V | | | 8 | MHz |
| | | | | 2.4 V ≤ $EV_{DD}$ < 2.7 V | | | 4 | MHz |
| | | LS (low-speed main) mode | | 1.8 V ≤ $EV_{DD}$ ≤ 5.5 V | | | 4 | MHz |
| | | LV (low-voltage main) mode | | 1.8 V ≤ $EV_{DD}$ ≤ 5.5 V | | | 4 | MHz |
| | | | | 1.6 V ≤ $EV_{DD}$ < 1.8 V | | | 2 | MHz |
| Interrupt input high-level width, low-level width | $t_{INTH}$, $t_{INTL}$ | INTP0 | | 1.6 V ≤ $V_{DD}$ ≤ 5.5 V | 1 | | | μs |
| | | INTP1 to INTP7 | | 1.6 V ≤ $EV_{DD}$ ≤ 5.5 V | 1 | | | μs |
| Key interrupt input low-level width | $t_{KR}$ | KR0 to KR3 | | 1.8 V ≤ $EV_{DD}$ ≤ 5.5 V | 250 | | | ns |
| | | | | 1.6 V ≤ $EV_{DD}$ < 1.8 V | 1 | | | μs |
| $\overline{RESET}$ low-level width | $t_{RSL}$ | | | | 10 | | | μs |

**Remark** $f_{MCK}$: Timer array unit operation clock frequency
(Operation clock to be set by the CKS0n bit of timer mode register 0n (TMR0n). n: Channel number (n = 0 to 7))

**UART mode connection diagram (during communication at same potential)**




**UART mode bit width (during communication at same potential) (reference)**




**Remarks 1.** q: UART number (q = 0), g: PIM and POM number (g = 1)

**2.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 01))

**(2) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output)**

**($T_A$ = –40 to +85°C, 1.6 V ≤ $EV_{DD}$ = $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | | HS (high-speed main) Mode | | LS (low-speed main) Mode | | LV (low-voltage main) Mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SCKp cycle time | $t_{KCY1}$ | 2.7 V ≤ $EV_{DD}$ ≤ 5.5 V | | 167 Note 1 | | 500 Note 1 | | 1000 Note 1 | | ns |
| | | 2.4 V ≤ $EV_{DD}$ ≤ 5.5 V | | 250 Note 1 | | 500 Note 1 | | 1000 Note 1 | | ns |
| | | 1.8 V ≤ $EV_{DD}$ ≤ 5.5 V | | | | 500 Note 1 | | 1000 Note 1 | | ns |
| | | 1.6 V ≤ $EV_{DD}$ ≤ 5.5 V | | | | | | 1000 Note 1 | | ns |
| SCKp high-/low-level width | $t_{KH1}$, $t_{KL1}$ | 4.0 V ≤ $EV_{DD}$ ≤ 5.5 V | | $t_{KCY1}$/2 – 12 | | $t_{KCY1}$/2 – 50 | | $t_{KCY1}$/2 – 50 | | ns |
| | | 2.7 V ≤ $EV_{DD}$ ≤ 5.5 V | | $t_{KCY1}$/2 – 18 | | $t_{KCY1}$/2 – 50 | | $t_{KCY1}$/2 – 50 | | ns |
| | | 2.4 V ≤ $EV_{DD}$ ≤ 5.5 V | | $t_{KCY1}$/2 – 38 | | $t_{KCY1}$/2 – 50 | | $t_{KCY1}$/2 – 50 | | ns |
| | | 1.8 V ≤ $EV_{DD}$ ≤ 5.5 V | | | | $t_{KCY1}$/2 – 50 | | $t_{KCY1}$/2 – 50 | | ns |
| | | 1.6 V ≤ $EV_{DD}$ ≤ 5.5 V | | | | | | $t_{KCY1}$/2 – 100 | | ns |
| SIp setup time (to SCKp↑) Note 2 | $t_{SIK1}$ | 2.7 V ≤ $EV_{DD}$ ≤ 5.5 V | | 44 | | 110 | | 110 | | ns |
| | | 2.4 V ≤ $EV_{DD}$ ≤ 5.5 V | | 75 | | 110 | | 110 | | ns |
| | | 1.8 V ≤ $EV_{DD}$ ≤ 5.5 V | | | | 110 | | 110 | | ns |
| | | 1.6 V ≤ $EV_{DD}$ ≤ 5.5 V | | | | | | 220 | | ns |
| SIp hold time (from SCKp↑) Note 3 | $t_{KSI1}$ | 2.4 V ≤ $EV_{DD}$ ≤ 5.5 V | | 19 | | 19 | | 19 | | ns |
| | | 1.8 V ≤ $EV_{DD}$ ≤ 5.5 V | | | | 19 | | 19 | | |
| | | 1.6 V ≤ $EV_{DD}$ ≤ 5.5 V | | | | | | 19 | | |
| Delay time from SCKp↓ to SOp output Note 4 | $t_{KSO1}$ | C = 30 pF Note 5 | 2.4 V ≤ $EV_{DD}$ ≤ 5.5 V | | 25 | | 25 | | 25 | ns |
| | | | 1.8 V ≤ $EV_{DD}$ ≤ 5.5 V | | | | 25 | | 25 | |
| | | | 1.6 V ≤ $EV_{DD}$ ≤ 5.5 V | | | | | | 25 | |

**Notes 1.** For CSI00, set a cycle of 2/$f_{MCK}$ or longer. For CSI01, set a cycle of 4/$f_{MCK}$ or longer.

**2.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**3.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

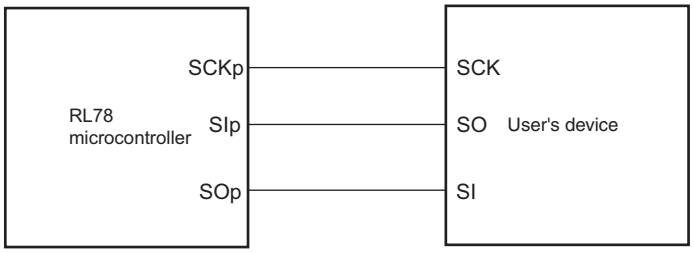
**4.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**5.** C is the load capacitance of the SCKp and SOp output lines.

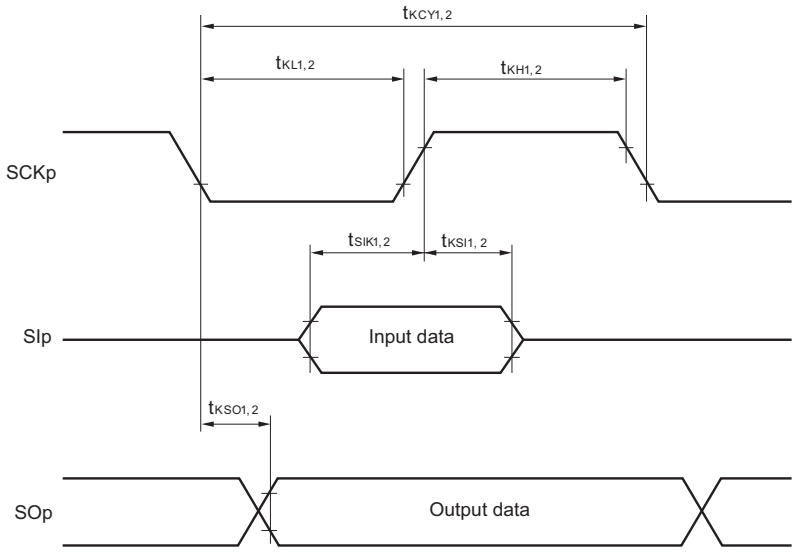
**Caution Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).**

(**Remarks** are listed on the next page.)

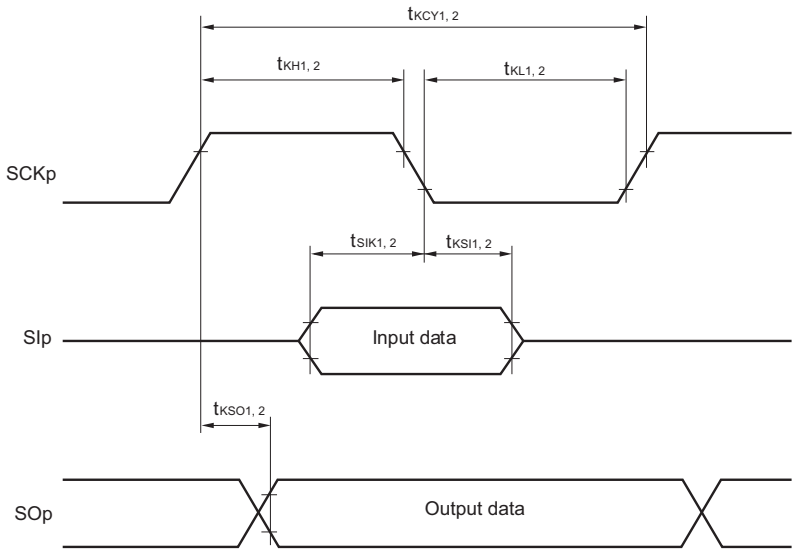
**CSI mode connection diagram (during communication at same potential)**




**CSI mode serial transfer timing (during communication at same potential)**
**(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)**



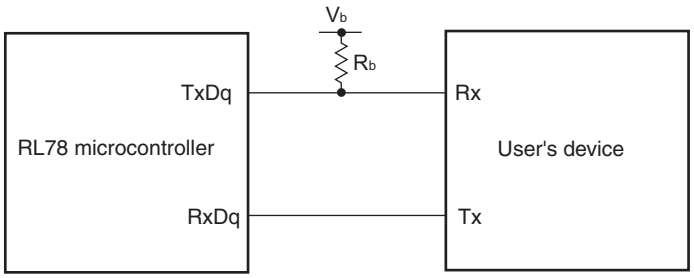

**CSI mode serial transfer timing (during communication at same potential)**
**(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)**



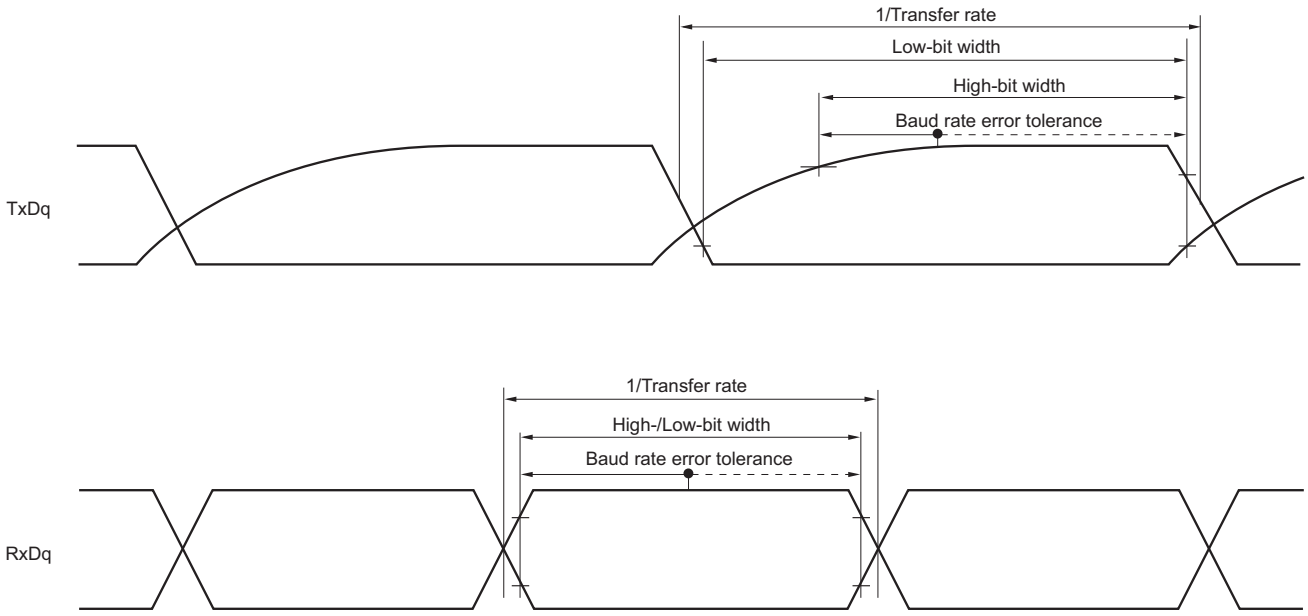

**Remarks 1.** p: CSI number (p = 00, 01)

**2.** m: Unit number, n: Channel number (mn = 00, 01)

**UART mode connection diagram (during communication at different potential)**




**UART mode bit width (during communication at different potential) (reference)**




**Remarks 1.** $R_b$[Ω]:Communication line (TxDq) pull-up resistance,
$C_b$[F]: Communication line (TxDq) load capacitance, $V_b$[V]: Communication line voltage

**2.** q: UART number (q = 0, 1), g: PIM and POM number (g = 1)

**3.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 01))

## 2.7.2 Internal voltage boosting method

**(1) 1/3 bias method**

**($T_A$ = –40 to +85°C, 1.8 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| LCD output voltage variation range | $V_{L1}$ | C1 to C4[Note 1] = 0.47 μF | VLCD = 04H | 0.90 | 1.00 | 1.08 | V |
| | | | VLCD = 05H | 0.95 | 1.05 | 1.13 | V |
| | | | VLCD = 06H | 1.00 | 1.10 | 1.18 | V |
| | | | VLCD = 07H | 1.05 | 1.15 | 1.23 | V |
| | | | VLCD = 08H | 1.10 | 1.20 | 1.28 | V |
| | | | VLCD = 09H | 1.15 | 1.25 | 1.33 | V |
| | | | VLCD = 0AH | 1.20 | 1.30 | 1.38 | V |
| | | | VLCD = 0BH | 1.25 | 1.35 | 1.43 | V |
| | | | VLCD = 0CH | 1.30 | 1.40 | 1.48 | V |
| | | | VLCD = 0DH | 1.35 | 1.45 | 1.53 | V |
| | | | VLCD = 0EH | 1.40 | 1.50 | 1.58 | V |
| | | | VLCD = 0FH | 1.45 | 1.55 | 1.63 | V |
| | | | VLCD = 10H | 1.50 | 1.60 | 1.68 | V |
| | | | VLCD = 11H | 1.55 | 1.65 | 1.73 | V |
| | | | VLCD = 12H | 1.60 | 1.70 | 1.78 | V |
| | | | VLCD = 13H | 1.65 | 1.75 | 1.83 | V |
| Doubler output voltage | $V_{L2}$ | C1 to C4[Note 1] = 0.47 μF | | 2 $V_{L1}$ – 0.1 | 2 $V_{L1}$ | 2 $V_{L1}$ | V |
| Tripler output voltage | $V_{L4}$ | C1 to C4[Note 1] = 0.47 μF | | 3 $V_{L1}$ – 0.15 | 3 $V_{L1}$ | 3 $V_{L1}$ | V |
| Reference voltage setup time[Note 2] | $t_{VWAIT1}$ | | | 5 | | | ms |
| Voltage boost wait time[Note 3] | $t_{VWAIT2}$ | C1 to C4[Note 1] = 0.47 μF | | 500 | | | ms |

**Notes 1.** This is a capacitor that is connected between voltage pins used to drive the LCD.
C1: A capacitor connected between CAPH and CAPL
C2: A capacitor connected between $V_{L1}$ and GND
C3: A capacitor connected between $V_{L2}$ and GND
C4: A capacitor connected between $V_{L4}$ and GND
C1 = C2 = C3 = C4 = 0.47 μF±30%

**2.** This is the time required to wait from when the reference voltage is specified by using the VLCD register (or when the internal voltage boosting method is selected [by setting the MDSET1 and MDSET0 bits of the LCDM0 register to 01B] if the default value reference voltage is used) until voltage boosting starts (VLCON = 1).

**3.** This is the wait time from when voltage boosting is started (VLCON = 1) until display is enabled (LCDON = 1).

**Absolute Maximum Ratings ($T_A$ = 25°C) (3/3)**

| Parameter | Symbols | Conditions | | Ratings | Unit |
|---|---|---|---|---|---|
| Output current, high | $I_{OH1}$ | Per pin | P10 to P17, P30 to P32, P40 to P43, P50 to P54, P70 to P74, P120, P125 to P127, P130, P140 to P147 | −40 | mA |
| | | Total of all pins −170 mA | P10 to P14, P40 to P43, P120, P130, P140 to P147 | −70 | mA |
| | | | P15 to P17, P30 to P32, P50 to P54, P70 to P74, P125 to P127 | −100 | mA |
| | $I_{OH2}$ | Per pin | P20, P21 | −0.5 | mA |
| | | Total of all pins | | −1 | mA |
| Output current, low | $I_{OL1}$ | Per pin | P10 to P17, P30 to P32, P40 to P43, P50 to P54, P60, P61, P70 to P74, P120, P125 to P127, P130, P140 to P147 | 40 | mA |
| | | Total of all pins 170 mA | P10 to P14, P40 to P43, P120, P130, P140 to P147 | 70 | mA |
| | | | P15 to P17, P30 to P32, P50 to P54, P60, P61, P70 to P74, P125 to P127 | 100 | mA |
| | $I_{OL2}$ | Per pin | P20, P21 | 1 | mA |
| | | Total of all pins | | 2 | mA |
| Operating ambient temperature | $T_A$ | In normal operation mode | | −40 to +105 | °C |
| | | In flash memory programming mode | | | |
| Storage temperature | $T_{stg}$ | | | −65 to +150 | °C |

**Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.**

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

**($T_A$ = –40 to +105°C, 2.4 V ≤ $EV_{DD}$ = $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS}$ = 0 V) (2/5)**

| Items | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Output current, low Note 1 | $I_{OL1}$ | Per pin for P10 to P17, P30 to P32, P40 to P43, P50 to P54, P70 to P74, P120, P125 to P127, P130, P140 to P147 | | | | 8.5 Note 2 | mA |
| | | Per pin for P60, P61 | | | | 15.0 Note 2 | mA |
| | | Total of P10 to P14, P40 to P43, P120, P130, P140 to P147 (When duty = 70% Note 3) | 4.0 V ≤ $EV_{DD}$ ≤ 5.5 V | | | 40.0 | mA |
| | | | 2.7 V ≤ $EV_{DD}$ < 4.0 V | | | 15.0 | mA |
| | | | 2.4 V ≤ $EV_{DD}$ < 2.7 V | | | 9.0 | mA |
| | | Total of P15 to P17, P30 to P32, P50 to P54, P60, P61, P70 to P74, P125 to P127 (When duty = 70% Note 3) | 4.0 V ≤ $EV_{DD}$ ≤ 5.5 V | | | 40.0 | mA |
| | | | 2.7 V ≤ $EV_{DD}$ < 4.0 V | | | 35.0 | mA |
| | | | 2,4 V ≤ $EV_{DD}$ < 2.7 V | | | 20.0 | mA |
| | | Total of all pins (When duty = 70% Note 3) | | | | 80.0 | mA |
| | $I_{OL2}$ | P20, P21 | Per pin | | | 0.4 | mA |
| | | | Total of all pins | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | | | 0.8 | mA |

**Notes 1.** Value of current at which the device operation is guaranteed even if the current flows from the $V_{DD}$ and $EV_{DD}$ pins to an output pin.

**2.** Do not exceed the total current value.

**3.** Specification under conditions where the duty factor ≤ 70%.
The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = ($I_{OL}$ × 0.7)/(n × 0.01)

<Example> Where n = 80% and $I_{OL}$ = 40.0 mA

Total output current of pins = (40.0 × 0.7)/(80 × 0.01) ≅ 35.0 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

**($T_A$ = –40 to +105°C, 2.4 V ≤ $EV_{DD}$ = $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS}$ = 0 V) (3/5)**

| Items | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Input voltage, high | $V_{IH1}$ | P10 to P17, P30 to P32, P40 to P43, P50 to P54, P70 to P74, P120, P125 to P127, P140 to P147 | Normal input buffer | 0.8$EV_{DD}$ | | $EV_{DD}$ | V |
| | $V_{IH2}$ | P10, P11, P15, P16 | TTL input buffer 4.0 V ≤ $EV_{DD}$ ≤ 5.5 V | 2.2 | | $EV_{DD}$ | V |
| | | | TTL input buffer 3.3 V ≤ $EV_{DD}$ < 4.0 V | 2.0 | | $EV_{DD}$ | V |
| | | | TTL input buffer 2.4 V ≤ $EV_{DD}$ < 3.3 V | 1.50 | | $EV_{DD}$ | V |
| | $V_{IH3}$ | P20, P21 | | 0.7$V_{DD}$ | | $V_{DD}$ | V |
| | $V_{IH4}$ | P60, P61 | | 0.7$EV_{DD}$ | | $EV_{DD}$ | V |
| | $V_{IH5}$ | P121 to P124, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$ | | 0.8$V_{DD}$ | | $V_{DD}$ | V |
| Input voltage, low | $V_{IL1}$ | P10 to P17, P30 to P32, P40 to P43, P50 to P54, P70 to P74, P120, P125 to P127, P140 to P147 | Normal input buffer | 0 | | 0.2$EV_{DD}$ | V |
| | $V_{IL2}$ | P10, P11, P15, P16 | TTL input buffer 4.0 V ≤ $EV_{DD}$ ≤ 5.5 V | 0 | | 0.8 | V |
| | | | TTL input buffer 3.3 V ≤ $EV_{DD}$ < 4.0 V | 0 | | 0.5 | V |
| | | | TTL input buffer 2.4 V ≤ $EV_{DD}$ < 3.3 V | 0 | | 0.32 | V |
| | $V_{IL3}$ | P20, P21 | | 0 | | 0.3$V_{DD}$ | V |
| | $V_{IL4}$ | P60, P61 | | 0 | | 0.3$EV_{DD}$ | V |
| | $V_{IL5}$ | P121 to P124, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$ | | 0 | | 0.2$V_{DD}$ | V |

**Caution The maximum value of $V_{IH}$ of pins P10, P12, P15, and P17 is $EV_{DD}$, even in the N-ch open-drain mode.**

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

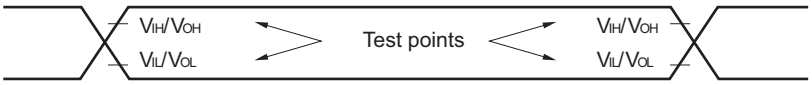
**($T_A$ = –40 to +105°C, 2.4 V ≤ $EV_{DD}$ = $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS}$ = 0 V) (5/5)**

| Items | Symbol | Conditions | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|
| Input leakage current, high | $I_{LIH1}$ | P10 to P17, P30 to P32, P40 to P43, P50 to P54, P60, P61, P70 to P74, P120, P125 to P127, P140 to P147 | $V_I$ = $EV_{DD}$ | | | | 1 | μA |
| | $I_{LIH2}$ | P20, P21, P137, $\overline{\text{RESET}}$ | $V_I$ = $V_{DD}$ | | | | 1 | μA |
| | $I_{LIH3}$ | P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS) | $V_I$ = $V_{DD}$ | In input port or external clock input | | | 1 | μA |
| | | | | In resonator connection | | | 10 | μA |
| Input leakage current, low | $I_{LIL1}$ | P10 to P17, P30 to P32, P40 to P43, P50 to P54, P60, P61, P70 to P74, P120, P125 to P127, P140 to P147 | $V_I$ = $EV_{SS}$ | | | | –1 | μA |
| | $I_{LIL2}$ | P20, P21, P137, $\overline{\text{RESET}}$ | $V_I$ = $V_{SS}$ | | | | –1 | μA |
| | $I_{LIL3}$ | P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS) | $V_I$ = $V_{SS}$ | In input port or external clock input | | | –1 | μA |
| | | | | In resonator connection | | | –10 | μA |
| On-chip pll-up resistance | $R_{U1}$ | $V_I$ = $EV_{SS}$ | SEGxx port | | | | | |
| | | | 2.4 V ≤ $EV_{DD}$ = $V_{DD}$ ≤ 5.5 V | | 10 | 20 | 100 | kΩ |
| | $R_{U2}$ | | Ports other than above (Except for P60, P61, and P130) | | 10 | 20 | 100 | kΩ |

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

## 3.5 Peripheral Functions Characteristics

**AC Timing Test Points**




### 3.5.1 Serial array unit

**(1) During communication at same potential (UART mode)**

**($T_A$ = –40 to +105°C, 2.4 V ≤ $EV_{DD}$ = $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | Unit |
|---|---|---|---|---|---|
| | | | MIN. | MAX. | |
| Transfer rate Note 1 | | | | $f_{MCK}$/12 | bps |
| | | Theoretical value of the maximum transfer rate $f_{MCK}$ = $f_{CLK}$ Note 2 | | 2.0 | Mbps |

**Notes 1.** Transfer rate in the SNOOZE mode is 4800 bps only.

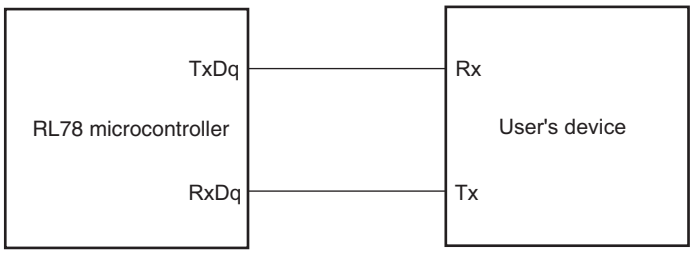
**2.** The maximum operating frequencies of the CPU/peripheral hardware clock ($f_{CLK}$) are:

HS (high-speed main) mode: 24 MHz (2.7 V ≤ $V_{DD}$ ≤ 5.5 V)

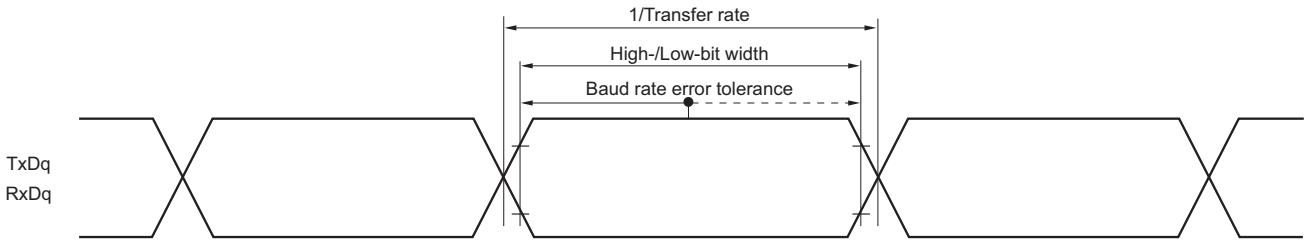
16 MHz (2.4 V ≤ $V_{DD}$ ≤ 5.5 V)

**Caution Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).**

**UART mode connection diagram (during communication at same potential)**




**UART mode bit width (during communication at same potential) (reference)**

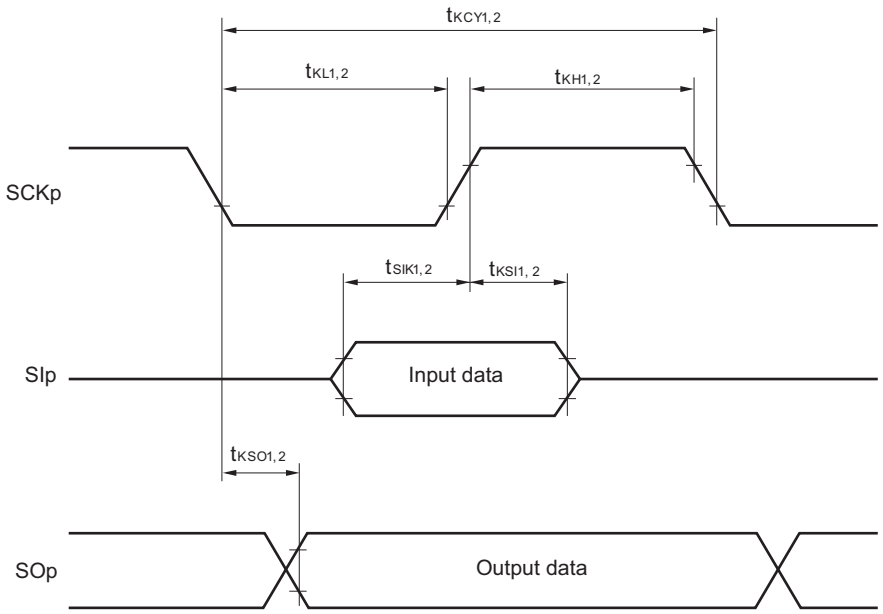



**Remarks 1.** q: UART number (q = 0), g: PIM and POM number (g = 1)

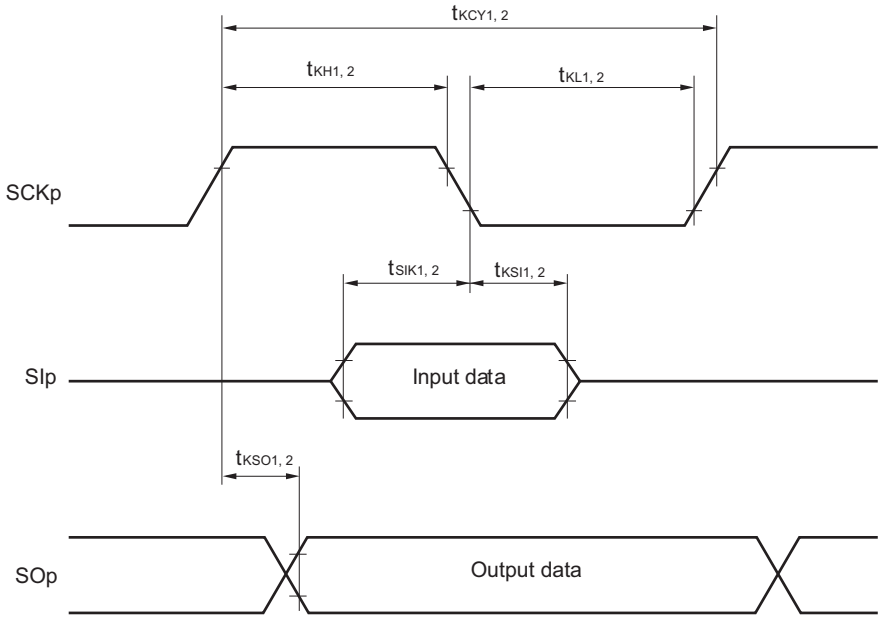
**2.** $f_{MCK}$: Serial array unit operation clock frequency

(Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 01))

**CSI mode serial transfer timing (during communication at same potential)**
**(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)**



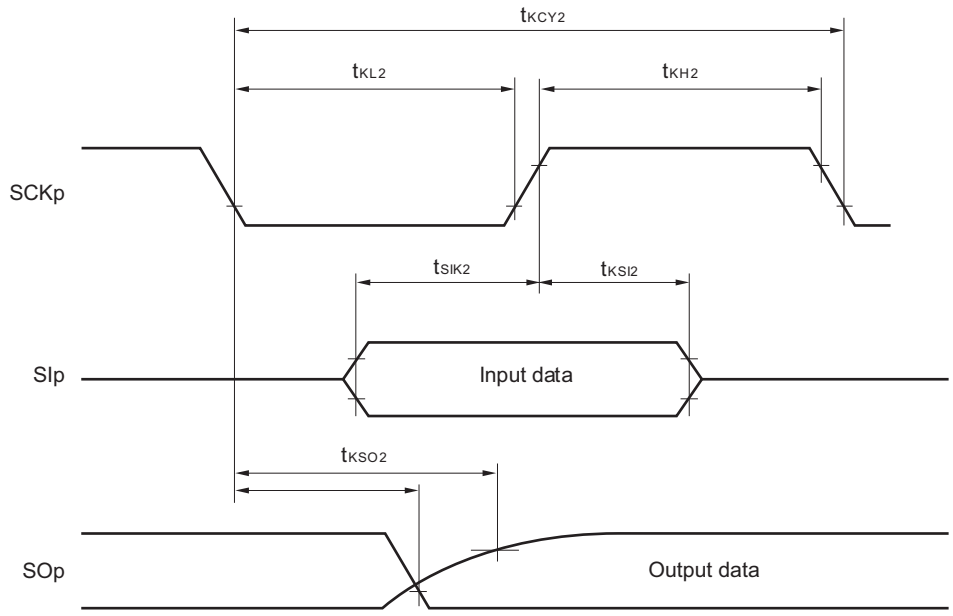

**CSI mode serial transfer timing (during communication at same potential)**
**(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)**



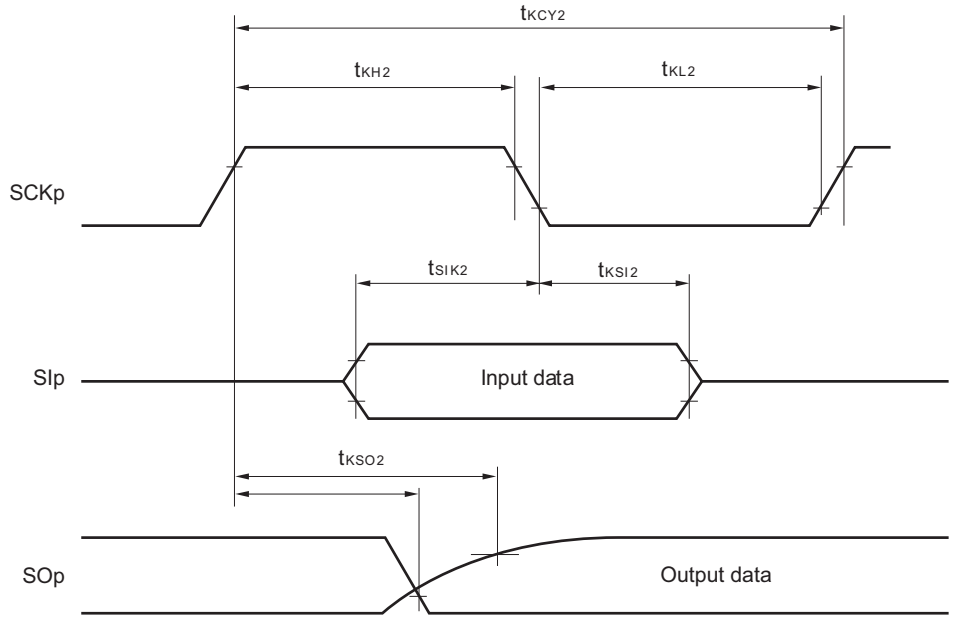

**Remarks 1.** p: CSI number (p = 00, 01)

**2.** m: Unit number, n: Channel number (mn = 00, 01)

**CSI mode serial transfer timing (slave mode) (during communication at different potential)**
**(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)**




**CSI mode serial transfer timing (slave mode) (during communication at different potential)**
**(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)**




**Remark** p: CSI number (p = 00, 01), m: Unit number (m = 0),
n: Channel number (n = 0, 1), g: PIM and POM number (g = 1)

## 3.6.4 LVD circuit characteristics

**($T_A$ = –40 to +105°C, $V_{PDR} \le EV_{DD} = V_{DD} \le 5.5$ V, $V_{SS} = EV_{SS}$ = 0 V)**

| Parameter | | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Detection voltage | Supply voltage level | $V_{LVD0}$ | Power supply rise time | 3.90 | 4.06 | 4.22 | V |
| | | | Power supply fall time | 3.83 | 3.98 | 4.13 | V |
| | | $V_{LVD1}$ | Power supply rise time | 3.60 | 3.75 | 3.90 | V |
| | | | Power supply fall time | 3.53 | 3.67 | 3.81 | V |
| | | $V_{LVD2}$ | Power supply rise time | 3.01 | 3.13 | 3.25 | V |
| | | | Power supply fall time | 2.94 | 3.06 | 3.18 | V |
| | | $V_{LVD3}$ | Power supply rise time | 2.90 | 3.02 | 3.14 | V |
| | | | Power supply fall time | 2.85 | 2.96 | 3.07 | V |
| | | $V_{LVD4}$ | Power supply rise time | 2.81 | 2.92 | 3.03 | V |
| | | | Power supply fall time | 2.75 | 2.86 | 2.97 | V |
| | | $V_{LVD5}$ | Power supply rise time | 2.70 | 2.81 | 2.92 | V |
| | | | Power supply fall time | 2.64 | 2.75 | 2.86 | V |
| | | $V_{LVD6}$ | Power supply rise time | 2.61 | 2.71 | 2.81 | V |
| | | | Power supply fall time | 2.55 | 2.65 | 2.75 | V |
| | | $V_{LVD7}$ | Power supply rise time | 2.51 | 2.61 | 2.71 | V |
| | | | Power supply fall time | 2.45 | 2.55 | 2.65 | V |
| Minimum pulse width | | $t_{LW}$ | | 300 | | | μs |
| Detection delay time | | | | | | 300 | μs |

**LVD Detection Voltage of Interrupt & Reset Mode**

**($T_A$ = –40 to +105°C, $V_{PDR} \le EV_{DD} = V_{DD} \le 5.5$ V, $V_{SS} = EV_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|
| Interrupt and reset mode | $V_{LVDD0}$ | $V_{POC2}$, $V_{POC1}$, $V_{POC0}$ = 0, 1, 1, falling reset voltage | | | 2.64 | 2.75 | 2.86 | V |
| | $V_{LVDD1}$ | | LVIS1, LVIS0 = 1, 0 | Rising release reset voltage | 2.81 | 2.92 | 3.03 | V |
| | | | | Falling interrupt voltage | 2.75 | 2.86 | 2.97 | V |
| | $V_{LVDD2}$ | | LVIS1, LVIS0 = 0, 1 | Rising release reset voltage | 2.90 | 3.02 | 3.14 | V |
| | | | | Falling interrupt voltage | 2.85 | 2.96 | 3.07 | V |
| | $V_{LVDD3}$ | | LVIS1, LVIS0 = 0, 0 | Rising release reset voltage | 3.90 | 4.06 | 4.22 | V |
| | | | | Falling interrupt voltage | 3.83 | 3.98 | 4.13 | V |

## 3.6.5 Power supply voltage rising slope characteristics

**($T_A$ = –40 to +105°C, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Power supply voltage rising slope | $S_{VDD}$ | | | | 54 | V/ms |

**Caution Make sure to keep the internal reset state by the LVD circuit or an external reset until $V_{DD}$ reaches the operating voltage range shown in 31.4 AC Characteristics.**