



Welcome to [E-XFL.COM](#)

What is "[Embedded - Microcontrollers](#)"?

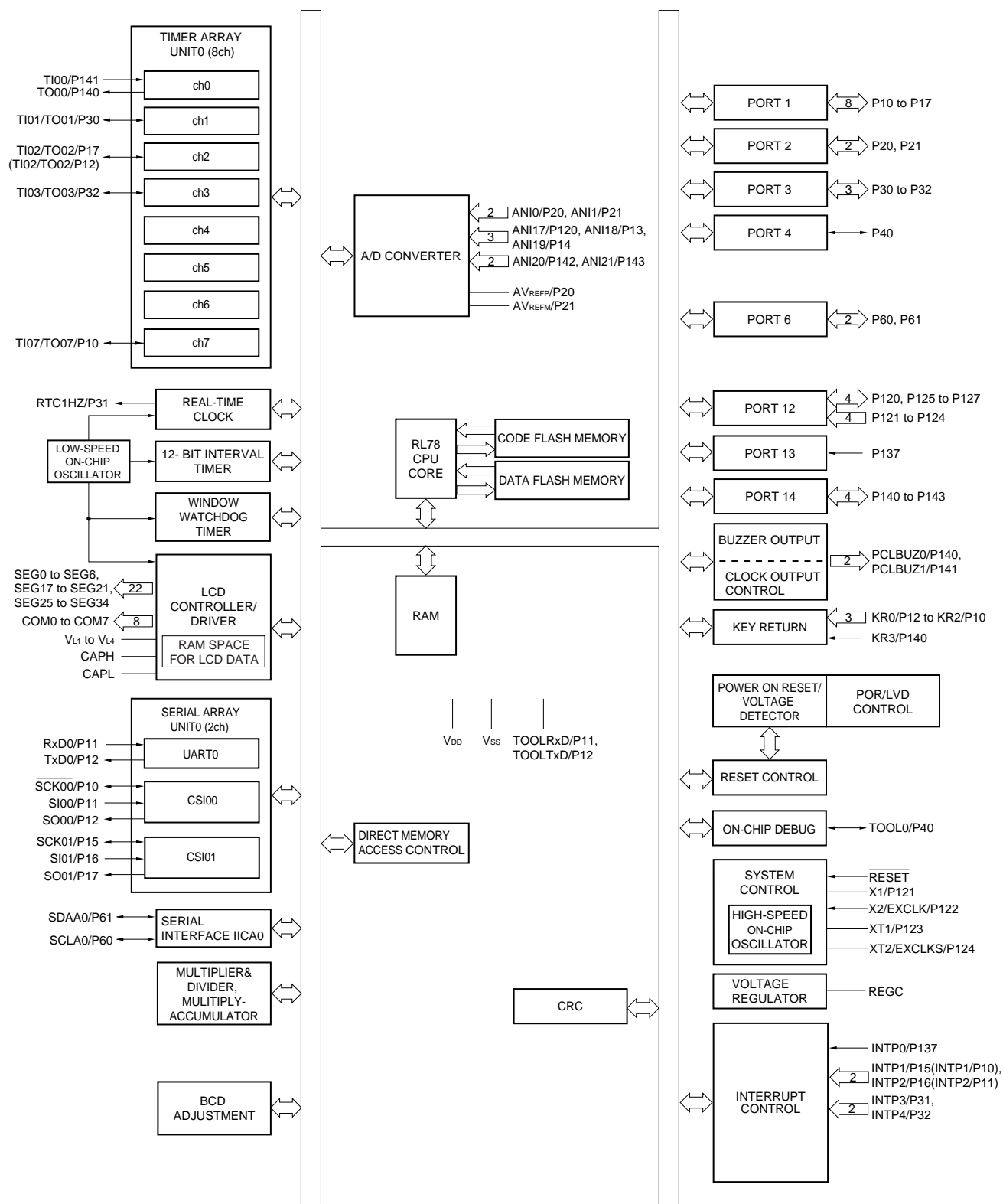
"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	RL78
Core Size	16-Bit
Speed	24MHz
Connectivity	CSI, I ² C, LINbus, UART/USART
Peripherals	DMA, LCD, LVD, POR, PWM, WDT
Number of I/O	37
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 10x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	52-LQFP
Supplier Device Package	52-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f10rj8gfa-30

1.5.2 44-pin products



Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR)

Absolute Maximum Ratings (T_A = 25°C)**(3/3)**

Parameter	Symbols	Conditions		Ratings	Unit
Output current, high	I _{OH1}	Per pin	P10 to P17, P30 to P32, P40 to P43, P50 to P54, P70 to P74, P120, P125 to P127, P130, P140 to P147	−40	mA
		Total of all pins −170 mA	P10 to P14, P40 to P43, P120, P130, P140 to P147	−70	mA
			P15 to P17, P30 to P32, P50 to P54, P70 to P74, P125 to P127	−100	mA
	I _{OH2}	Per pin	P20, P21	−0.5	mA
		Total of all pins		−1	mA
Output current, low	I _{OL1}	Per pin	P10 to P17, P30 to P32, P40 to P43, P50 to P54, P60, P61, P70 to P74, P120, P125 to P127, P130, P140 to P147	40	mA
		Total of all pins 170 mA	P10 to P14, P40 to P43, P120, P130, P140 to P147	70	mA
			P15 to P17, P30 to P32, P50 to P54, P60, P61, P70 to P74, P125 to P127	100	mA
	I _{OL2}	Per pin	P20, P21	1	mA
		Total of all pins		2	mA
Operating ambient temperature	T _A	In normal operation mode		−40 to +85	°C
		In flash memory programming mode			
Storage temperature	T _{stg}			−65 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = -40 to +85°C, 1.6 V ≤ E_{VDD} = V_{DD} ≤ 5.5 V, V_{SS} = E_{VSS} = 0 V)

(3/5)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V _{IH1}	P10 to P17, P30 to P32, P40 to P43, P50 to P54, P70 to P74, P120, P125 to P127, P140 to P147	Normal input buffer	0.8E _{VDD}		E _{VDD}	V
	V _{IH2}	P10, P11, P15, P16	TTL input buffer 4.0 V ≤ E _{VDD} ≤ 5.5 V	2.2		E _{VDD}	V
			TTL input buffer 3.3 V ≤ E _{VDD} < 4.0 V	2.0		E _{VDD}	V
			TTL input buffer 1.6 V ≤ E _{VDD} < 3.3 V	1.50		E _{VDD}	V
	V _{IH3}	P20, P21		0.7V _{DD}		V _{DD}	V
	V _{IH4}	P60, P61		0.7E _{VDD}		E _{VDD}	V
	V _{IH5}	P121 to P124, P137, EXCLK, EXCLKS, RESET		0.8V _{DD}		V _{DD}	V
Input voltage, low	V _{IL1}	P10 to P17, P30 to P32, P40 to P43, P50 to P54, P70 to P74, P120, P125 to P127, P140 to P147	Normal input buffer	0		0.2E _{VDD}	V
	V _{IL2}	P10, P11, P15, P16	TTL input buffer 4.0 V ≤ E _{VDD} ≤ 5.5 V	0		0.8	V
			TTL input buffer 3.3 V ≤ E _{VDD} < 4.0 V	0		0.5	V
			TTL input buffer 1.6 V ≤ E _{VDD} < 3.3 V	0		0.32	V
	V _{IL3}	P20, P21		0		0.3V _{DD}	V
	V _{IL4}	P60, P61		0		0.3E _{VDD}	V
	V _{IL5}	P121 to P124, P137, EXCLK, EXCLKS, RESET		0		0.2V _{DD}	V

Caution The maximum value of V_{IH} of P10, P12, P15, P17 is E_{VDD}, even in the N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

- Notes**
1. Total current flowing into V_{DD} and EV_{DD}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, EV_{DD} or V_{SS}, EV_{SS}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
 2. When high-speed on-chip oscillator and subsystem clock are stopped.
 3. When high-speed system clock and subsystem clock are stopped.
 4. When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). However, not including the current flowing into the RTC, 12-bit interval timer, watchdog timer, and LCD controller/driver.
 5. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
 - HS (high-speed main) mode: $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ @1 MHz to 24 MHz
 - $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ @1 MHz to 16 MHz
 - LS (low-speed main) mode: $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ @1 MHz to 8 MHz
 - LV (low-voltage main) mode: $1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ @1 MHz to 4 MHz

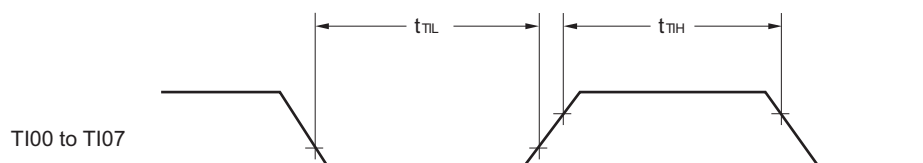
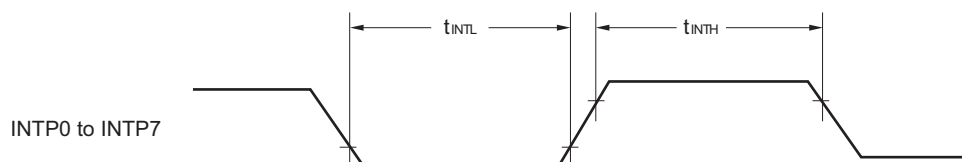
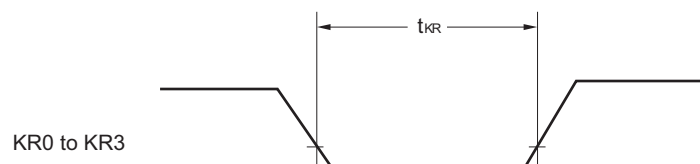
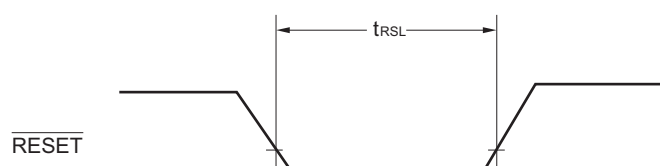
- Remarks**
1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
 2. f_{IH}: High-speed on-chip oscillator clock frequency
 3. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)
 4. Except subsystem clock operation, temperature condition of the TYP. value is T_A = 25°C

(T_A = -40 to +85°C, 1.6 V ≤ E_{VDD} = V_{DD} ≤ 5.5 V, V_{SS} = E_{VSS} = 0 V)

(3/3)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Low-speed on-chip oscillator operating current	I _{FIL} ^{Note 1}				0.20		μA
RTC operating current	I _{RTC} Notes 1, 2, 3	f _{MAIN} is stopped			0.08		μA
12-bit interval timer current	I _{IT} Notes 1, 2, 4				0.08		μA
Watchdog timer operating current	I _{WDT} Notes 1, 2, 5	f _{IL} = 15 kHz			0.24		μA
A/D converter operating current	I _{ADC} Notes 1, 6	When conversion at maximum speed	Normal mode, AV _{REFP} = V _{DD} = 5.0 V		1.3	1.7	mA
			Low voltage mode, AV _{REFP} = V _{DD} = 3.0 V		0.5	0.7	mA
A/D converter reference voltage current	I _{ADREF} ^{Note 1}				75.0		μA
Temperature sensor operating current	I _{TMPS} ^{Note 1}				75.0		μA
LVD operating current	I _{LVD} Notes 1, 7				0.08		μA
Self-programming operating current	I _{FSP} Notes 1, 9				2.50	12.20	mA
BGO operating current	I _{BGO} Notes 1, 8				2.00	12.20	mA
LCD operating current	I _{LCD1} Notes 11, 12	External resistance division method	V _{DD} = E _{VDD} = 5.0 V V _{L4} = 5.0 V		0.04	0.20	μA
	I _{LCD2} ^{Note 11}	Internal voltage boosting method	V _{DD} = E _{VDD} = 5.0 V V _{L4} = 5.1 V (VLCD = 12H)		1.12	3.70	μA
			V _{DD} = E _{VDD} = 3.0 V V _{L4} = 3.0 V (VLCD = 04H)		0.63	2.20	μA
	I _{LCD3} ^{Note 11}	Capacitor split method	V _{DD} = E _{VDD} = 3.0 V V _{L4} = 3.0 V		0.12	0.50	μA
SNOOZE operating current	I _{SNOZ} ^{Note 1}	ADC operation	The mode is performed ^{Note 10}		0.50	0.60	mA
			The A/D conversion operations are performed, Low voltage mode, AV _{REFP} = V _{DD} = 3.0 V		1.20	1.44	mA
		CSI/UART operation			0.70	0.84	mA

(Notes and Remarks are listed on the next page.)

TI/TO Timing**Interrupt Request Input Timing****Key Interrupt Input Timing****RESET Input Timing**

(4) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode)

(1/2)

(T_A = -40 to +85°C, 1.8 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Transfer rate		Reception	4.0 V ≤ EV _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V			f _{MCK} /6 Note 1		f _{MCK} /6 Note 1	bps
			Theoretical value of the maximum transfer rate f _{MCK} = f _{CLK} Note 3			4.0		1.3	Mbps
			2.7 V ≤ EV _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V			f _{MCK} /6 Note 1		f _{MCK} /6 Note 1	bps
			Theoretical value of the maximum transfer rate f _{MCK} = f _{CLK} Note 3			4.0		1.3	Mbps
			2.4 V ≤ EV _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V			f _{MCK} /6 Note 1		f _{MCK} /6 Note 1	bps
			Theoretical value of the maximum transfer rate f _{MCK} = f _{CLK} Note 3			4.0		1.3	Mbps
			1.8 V ≤ EV _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V					f _{MCK} /6 Notes 1, 2	bps
			Theoretical value of the maximum transfer rate f _{MCK} = f _{CLK} Note 3					1.3	Mbps

Notes 1. Transfer rate in the SNOOZE mode is 4800 bps only.**2.** Use it with EV_{DD} ≥ V_b.**3.** The maximum operating frequencies of the CPU/peripheral hardware clock (f_{CLK}) are:HS (high-speed main) mode: 24 MHz (2.7 V ≤ V_{DD} ≤ 5.5 V)16 MHz (2.4 V ≤ V_{DD} ≤ 5.5 V)LS (low-speed main) mode: 8 MHz (1.8 V ≤ V_{DD} ≤ 5.5 V)LV (low-voltage main) mode: 4 MHz (1.6 V ≤ V_{DD} ≤ 5.5 V)

Caution Select the TTL input buffer for the Rx_{Dq} pin and the N-ch open drain output (V_{DD} tolerance (32-pin to 52-pin products)/EV_{DD} tolerance (64-pin products)) mode for the Tx_{Dq} pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

Remarks 1. V_b[V]: Communication line voltage**2.** q: UART number (q = 0), g: PIM and POM number (g = 1)**3.** f_{MCK}: Serial array unit operation clock frequency(Operation clock to be set by the serial clock select register m (SPS_m) and the CKS_{mn} bit of serial mode register mn (SMR_{mn}). m: Unit number, n: Channel number (mn = 00, 01))

(4) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode)

(2/2)

(T_A = -40 to +85°C, 1.8 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Transfer rate		Transmission	4.0 V ≤ EV _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V			Note 1		Note 1	bps
			Theoretical value of the maximum transfer rate C _b = 50 pF, R _b = 1.4 kΩ, V _b = 2.7 V			2.8 ^{Note 2}		2.8 ^{Note 2}	Mbps
			2.7 V ≤ EV _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V			Note 3		Note 3	bps
			Theoretical value of the maximum transfer rate C _b = 50 pF, R _b = 2.7 kΩ, V _b = 2.3 V			1.2 ^{Note 4}		1.2 ^{Note 4}	Mbps
			2.4 V ≤ EV _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V			Note 6		Note 6	bps
			Theoretical value of the maximum transfer rate C _b = 50 pF, R _b = 5.5 kΩ, V _b = 1.6 V			0.43 ^{Note 7}		0.43 ^{Note 7}	Mbps
			1.8 V ≤ EV _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V				Notes 5, 6	Notes 5, 6	bps
			Theoretical value of the maximum transfer rate C _b = 50 pF, R _b = 5.5 kΩ, V _b = 1.6 V				0.43 ^{Note 7}	0.43 ^{Note 7}	Mbps

Notes 1. The smaller maximum transfer rate derived by using f_{MCK}/6 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 4.0 V ≤ EV_{DD} ≤ 5.5 V and 2.7 V ≤ V_b ≤ 4.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

- 2.** This value as an example is calculated when the conditions described in the "Conditions" column are met. Refer to Note 1 above to calculate the maximum transfer rate under conditions of the customer.

- Notes**
1. The first clock pulse is generated after this period when the start/restart condition is detected.
 2. The maximum value (MAX.) of t_{HD:DAT} is during normal transfer and a wait state is inserted in the $\overline{\text{ACK}}$ (acknowledge) timing.

Remark The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.

Standard mode: C_b = 400 pF, R_b = 2.7 kΩ

2.7 LCD Characteristics

2.7.1 Resistance division method

(1) Static display mode

(T_A = -40 to +85°C, V_{L4} (MIN.) ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
LCD drive voltage	V _{L4}		2.0		V _{DD}	V

(2) 1/2 bias method, 1/4 bias method

(T_A = -40 to +85°C, V_{L4} (MIN.) ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
LCD drive voltage	V _{L4}		2.7		V _{DD}	V

(3) 1/3 bias method

(T_A = -40 to +85°C, V_{L4} (MIN.) ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
LCD drive voltage	V _{L4}		2.5		V _{DD}	V

(2) 1/4 bias method

(T_A = -40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
LCD output voltage variation range	V _{L1} ^{Note 4}	C1 to C5 ^{Note 1} = 0.47 μF	VLCD = 04H	0.90	1.00	1.08	V
			VLCD = 05H	0.95	1.05	1.13	V
			VLCD = 06H	1.00	1.10	1.18	V
			VLCD = 07H	1.05	1.15	1.23	V
			VLCD = 08H	1.10	1.20	1.28	V
			VLCD = 09H	1.15	1.25	1.33	V
			VLCD = 0AH	1.20	1.30	1.38	V
			VLCD = 0BH	1.25	1.35	1.43	V
			VLCD = 0CH	1.30	1.40	1.48	V
			VLCD = 0DH	1.35	1.45	1.53	V
			VLCD = 0EH	1.40	1.50	1.58	V
			VLCD = 0FH	1.45	1.55	1.63	V
			VLCD = 10H	1.50	1.60	1.68	V
			VLCD = 11H	1.55	1.65	1.73	V
			VLCD = 12H	1.60	1.70	1.78	V
			VLCD = 13H	1.65	1.75	1.83	V
Doubler output voltage	V _{L2}	C1 to C5 ^{Note 1} = 0.47 μF	2 V _{L1} - 0.08	2 V _{L1}	2 V _{L1}	V	
Tripler output voltage	V _{L3}	C1 to C5 ^{Note 1} = 0.47 μF	3 V _{L1} - 0.12	3 V _{L1}	3 V _{L1}	V	
Quadruply output voltage	V _{L4} ^{Note 4}	C1 to C5 ^{Note 1} = 0.47 μF	4 V _{L1} - 0.16	4 V _{L1}	4 V _{L1}	V	
Reference voltage setup time ^{Note 2}	t _{WAIT1}		5			ms	
Voltage boost wait time ^{Note 3}	t _{WAIT2}	C1 to C5 ^{Note 1} = 0.47 μF	500			ms	

Notes 1. This is a capacitor that is connected between voltage pins used to drive the LCD.

C1: A capacitor connected between CAPH and CAPL

C2: A capacitor connected between V_{L1} and GNDC3: A capacitor connected between V_{L2} and GNDC4: A capacitor connected between V_{L3} and GNDC5: A capacitor connected between V_{L4} and GND

C1 = C2 = C3 = C4 = C5 = 0.47 μF ± 30%

2. This is the time required to wait from when the reference voltage is specified by using the VLCD register (or when the internal voltage boosting method is selected [by setting the MDSET1 and MDSET0 bits of the LCDM0 register to 01B] if the default value reference voltage is used) until voltage boosting starts (VLCON = 1).

3. This is the wait time from when voltage boosting is started (VLCON = 1) until display is enabled (LCDON = 1).

4. V_{L4} must be 5.5 V or lower.

2.7.3 Capacitor split method

1/3 bias method

(T_A = -40 to +85°C, 2.2 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
V _{L4} voltage	V _{L4}	C1 to C4 = 0.47 μF ^{Note 2}		V _{DD}		V
V _{L2} voltage	V _{L2}	C1 to C4 = 0.47 μF ^{Note 2}	2/3 V _{L4} - 0.1	2/3 V _{L4}	2/3 V _{L4} + 0.1	V
V _{L1} voltage	V _{L1}	C1 to C4 = 0.47 μF ^{Note 2}	1/3 V _{L4} - 0.1	1/3 V _{L4}	1/3 V _{L4} + 0.1	V
Capacitor split wait time ^{Note 1}	t _{WAIT}		100			ms

3. ELECTRICAL SPECIFICATIONS (G: $T_A = -40$ to $+105^{\circ}\text{C}$)

This chapter describes the electrical specifications for the products "G: Industrial applications ($T_A = -40$ to $+105^{\circ}\text{C}$)".

- Cautions**
1. The RL78 microcontrollers have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.
 2. With products not provided with an EV_{DD} or EV_{SS} pin, replace EV_{DD} with V_{DD} , or replace EV_{SS} with V_{SS} .
 3. For derating with $T_A = +85$ to $+105^{\circ}\text{C}$, contact our Sales Division or the vender's sales division. Derating means the specified reduction in an operating parameter to improve reliability.

There are following differences between the products "G: Industrial applications (T_A = -40 to +105°C)" and the products "A: Consumer applications, and G: Industrial applications (T_A = -40 to +85°C)".

Parameter	Application	
	A: Consumer applications, G: Industrial applications (with T _A = -40 to +85°C)	G: Industrial applications
Operating ambient temperature	T _A = -40 to +85°C	T _A = -40 to +105°C
Operating mode Operating voltage range	HS (high-speed main) mode: 2.7 V ≤ V _{DD} ≤ 5.5 V@1 MHz to 32 MHz 2.4 V ≤ V _{DD} ≤ 5.5 V@1 MHz to 16 MHz LS (low-speed main) mode: 1.8 V ≤ V _{DD} ≤ 5.5 V@1 MHz to 8 MHz LV (low-voltage main) mode: 1.6 V ≤ V _{DD} ≤ 5.5 V@1 MHz to 4 MHz	HS (high-speed main) mode only: 2.7 V ≤ V _{DD} ≤ 5.5 V@1 MHz to 32 MHz 2.4 V ≤ V _{DD} ≤ 5.5 V@1 MHz to 16 MHz
High-speed on-chip oscillator clock accuracy	1.8 V ≤ V _{DD} ≤ 5.5 V: ±1.0%@ T _A = -20 to +85°C ±1.5%@ T _A = -40 to -20°C 1.6 V ≤ V _{DD} < 1.8 V: ±5.0%@ T _A = -20 to +85°C ±5.5%@ T _A = -40 to -20°C	2.4 V ≤ V _{DD} ≤ 5.5 V: ±2.0%@ T _A = +85 to +105°C ±1.0%@ T _A = -20 to +85°C ±1.5%@ T _A = -40 to -20°C
Serial array unit	UART CSI00: f _{CLK} /2 (supporting 16 Mbps), f _{CLK} /4 CSI01 Simplified I ² C communication	UART CSI00: f _{CLK} /4 CSI01 Simplified I ² C communication
IICA	Normal mode Fast mode Fast mode plus	Normal mode Fast mode
Voltage detector	Rise detection voltage: 1.67 V to 4.06 V (14 levels) Fall detection voltage: 1.63 V to 3.98 V (14 levels)	Rise detection voltage: 2.61 V to 4.06 V (8 levels) Fall detection voltage: 2.55 V to 3.98 V (8 levels)

Remark The electrical characteristics of the products G: Industrial applications (T_A = -40 to +105°C) are different from those of the products "A: Consumer applications, and G: Industrial applications (only with T_A = -40 to +85°C)". For details, refer to **3.1** to **3.10**.

Absolute Maximum Ratings (T_A = 25°C)**(2/3)**

Parameter	Symbols	Conditions		Ratings	Unit
LCD voltage	V _{L1}	V _{L1} voltage ^{Note 1}		−0.3 to +2.8 and −0.3 to V _{L4} + 0.3	V
	V _{L2}	V _{L2} voltage ^{Note 1}		−0.3 to V _{L4} + 0.3 ^{Note 2}	V
	V _{L3}	V _{L3} voltage ^{Note 1}		−0.3 to V _{L4} + 0.3 ^{Note 2}	V
	V _{L4}	V _{L4} voltage ^{Note 1}		−0.3 to +6.5	V
	V _{LCAP}	CAPL, CAPH voltage ^{Note 1}		−0.3 to V _{L4} + 0.3 ^{Note 2}	V
	V _{LOUT}	COM0 to COM7, SEG0 to SEG38, output voltage	External resistance division method	−0.3 to V _{DD} + 0.3 ^{Note 2}	V
			Capacitor split method	−0.3 to V _{DD} + 0.3 ^{Note 2}	
Internal voltage boosting method			−0.3 to V _{L4} + 0.3 ^{Note 2}		

Notes 1. This value only indicates the absolute maximum ratings when applying voltage to the V_{L1}, V_{L2}, V_{L3}, and V_{L4} pins; it does not mean that applying voltage to these pins is recommended. When using the internal voltage boosting method or capacitance split method, connect these pins to V_{SS} via a capacitor (0.47 μF ± 30%) and connect a capacitor (0.47 μF ± 30%) between the CAPL and CAPH pins.

2. Must be 6.5 V or lower.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark V_{SS} : Reference voltage

- Notes**
1. Total current flowing into V_{DD} and EV_{DD}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, EV_{DD} or V_{SS}, EV_{SS}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
 2. During HALT instruction execution by flash memory.
 3. When high-speed on-chip oscillator and subsystem clock are stopped.
 4. When high-speed system clock and subsystem clock are stopped.
 5. When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1). The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer, watchdog timer, and LCD controller/driver.
 6. Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.
 7. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
 HS (high-speed main) mode: $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }24\text{ MHz}$
 $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }16\text{ MHz}$
 8. Regarding the value for current operate the subsystem clock in STOP mode, refer to that in HALT mode.

- Remarks**
1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
 2. f_{IH}: High-speed on-chip oscillator clock frequency
 3. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)
 4. Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is T_A = 25°C

3.4 AC Characteristics

3.4.1 Basic operation

(T_A = -40 to +105°C, 2.4 V ≤ E_{VDD} = V_{DD} ≤ 5.5 V, V_{SS} = E_{VSS} = 0 V)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Instruction cycle (minimum instruction execution time)	T _{CY}	Main system clock (f _{MAIN}) operation	HS (high-speed main) mode	2.7 V ≤ V _{DD} ≤ 5.5 V	0.04167	1	μs
				2.4 V ≤ V _{DD} < 2.7 V	0.0625	1	μs
		Subsystem clock (f _{SUB}) operation		2.4 V ≤ V _{DD} ≤ 5.5 V	28.5	30.5	μs
		In the self programming mode	HS (high-speed main) mode	2.7 V ≤ V _{DD} ≤ 5.5 V	0.04167	1	μs
				2.4 V ≤ V _{DD} < 2.7 V	0.0625	1	μs
External system clock frequency	f _{EX}	2.7 V ≤ V _{DD} ≤ 5.5 V		1.0		20.0	MHz
		2.4 V ≤ V _{DD} < 2.7 V		1.0		16.0	MHz
	f _{EXS}			32		35	kHz
External system clock input high-level width, low-level width	t _{EXH} , t _{EXL}	2.7 V ≤ V _{DD} ≤ 5.5 V		24			ns
		2.4 V ≤ V _{DD} < 2.7 V		30			ns
	t _{EXHS} , t _{EXLS}			13.7			μs
TI00 to TI07 input high-level width, low-level width	t _{TIH} , t _{TIL}			1/f _{MCK} +10			ns
TO00 to TO07 output frequency	f _{TO}	HS (high-speed main) mode	4.0 V ≤ E _{VDD} ≤ 5.5 V			16	MHz
			2.7 V ≤ E _{VDD} < 4.0 V			8	MHz
			2.4 V ≤ E _{VDD} < 2.7 V			4	MHz
PCLBUZ0, PCLBUZ1 output frequency	f _{PCL}	HS (high-speed main) mode	4.0 V ≤ E _{VDD} ≤ 5.5 V			16	MHz
			2.7 V ≤ E _{VDD} < 4.0 V			8	MHz
			2.4 V ≤ E _{VDD} < 2.7 V			4	MHz
Interrupt input high-level width, low-level width	t _{INTH} , t _{INTL}	INTP0	2.4 V ≤ V _{DD} ≤ 5.5 V	1			μs
		INTP1 to INTP7	2.4 V ≤ V _{DD} ≤ 5.5 V	1			μs
Key interrupt input low-level width	t _{KR}	KR0 to KR3	2.4 V ≤ E _{VDD} ≤ 5.5 V	250			ns
RESET low-level width	t _{RSL}			10			μs

Remark f_{MCK}: Timer array unit operation clock frequency

(Operation clock to be set by the CKS0n bit of timer mode register 0n (TMR0n).

n: Channel number (n = 0 to 7))

5. The smaller maximum transfer rate derived by using $f_{MCK}/6$ or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when $1.8\text{ V} \leq EV_{DD} < 3.3\text{ V}$ and $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\} \times 3} \text{ [bps]}$$

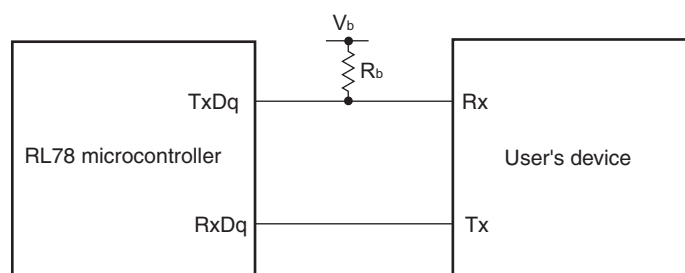
$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

6. This value as an example is calculated when the conditions described in the "Conditions" column are met. Refer to Note 5 above to calculate the maximum transfer rate under conditions of the customer.

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance (32- to 52-pin products)/EV_{DD} tolerance (64-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

UART mode connection diagram (during communication at different potential)



(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (slave mode, SCKp... external clock input)
(T_A = -40 to +105°C, 2.4 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		Unit
				MIN.	MAX.	
SCKp cycle time ^{Note 1}	t _{KCY2}	4.0 V ≤ EV _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V	20 MHz < f _{MCK} ≤ 24 MHz	24/f _{MCK}		ns
			8 MHz < f _{MCK} ≤ 20 MHz	20/f _{MCK}		ns
			4 MHz < f _{MCK} ≤ 8 MHz	16/f _{MCK}		ns
			f _{MCK} ≤ 4 MHz	12/f _{MCK}		ns
		2.7 V ≤ EV _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V	20 MHz < f _{MCK} ≤ 24 MHz	32/f _{MCK}		ns
			16 MHz < f _{MCK} ≤ 20 MHz	28/f _{MCK}		ns
			8 MHz < f _{MCK} ≤ 16 MHz	24/f _{MCK}		ns
			4 MHz < f _{MCK} ≤ 8 MHz	16/f _{MCK}		ns
			f _{MCK} ≤ 4 MHz	12/f _{MCK}		ns
		2.4 V ≤ EV _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V	20 MHz < f _{MCK} ≤ 24 MHz	72/f _{MCK}		ns
			16 MHz < f _{MCK} ≤ 20 MHz	64/f _{MCK}		ns
			8 MHz < f _{MCK} ≤ 16 MHz	52/f _{MCK}		ns
			4 MHz < f _{MCK} ≤ 8 MHz	32/f _{MCK}		ns
			f _{MCK} ≤ 4 MHz	20/f _{MCK}		ns
SCKp high-/low-level width	t _{KH2} , t _{KL2}	4.0 V ≤ EV _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V		t _{KCY2} /2 – 24		ns
		2.7 V ≤ EV _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V		t _{KCY2} /2 – 36		ns
		2.4 V ≤ EV _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V		t _{KCY2} /2 – 100		ns
Slp setup time (to SCKp↑) ^{Note 2}	t _{SIK2}	4.0 V ≤ EV _{DD} < 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V		1/f _{MCK} + 40		ns
		2.7 V ≤ EV _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V		1/f _{MCK} + 40		ns
		2.4 V ≤ EV _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V		1/f _{MCK} + 60		ns
Slp hold time (from SCKp↑) ^{Note 3}	t _{KSI2}	4.0 V ≤ EV _{DD} < 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V		1/f _{MCK} + 62		ns
		2.7 V ≤ EV _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V		1/f _{MCK} + 62		ns
		2.4 V ≤ EV _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V		1/f _{MCK} + 62		ns
Delay time from SCKp↓ to SOp output ^{Note 4}	t _{KSO2}	4.0 V ≤ EV _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 30 pF, R _b = 1.4 kΩ			2/f _{MCK} + 240	ns
		2.7 V ≤ EV _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ			2/f _{MCK} + 428	ns
		2.4 V ≤ EV _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V C _b = 30 pF, R _b = 5.5 kΩ			2/f _{MCK} + 1146	ns

(Notes, Caution and Remarks are listed on the page after the next page.)

(3) When reference voltage (+) = V_{DD} (ADREFP1 = 0, ADREFP0 = 0), reference voltage (-) = V_{SS} (ADREFM = 0), target pin : ANI0, ANI1, ANI16 to ANI23, internal reference voltage, and temperature sensor output voltage

(T_A = -40 to +105°C, 2.4 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V, Reference voltage (+) = V_{DD}, Reference voltage (-) = V_{SS})

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error ^{Note 1}	AINL	10-bit resolution	2.4 V ≤ V _{DD} ≤ 5.5 V		1.2	±7.0	LSB
Conversion time	t _{CONV}	10-bit resolution	3.6 V ≤ V _{DD} ≤ 5.5 V	2.125		39	μs
			2.7 V ≤ V _{DD} ≤ 5.5 V	3.1875		39	μs
			2.4 V ≤ V _{DD} ≤ 5.5 V	17		39	μs
		10-bit resolution Target pin: Internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode)	3.6 V ≤ V _{DD} ≤ 5.5 V	2.375		39	μs
			2.7 V ≤ V _{DD} ≤ 5.5 V	3.5625		39	μs
			2.4 V ≤ V _{DD} ≤ 5.5 V	17		39	μs
Zero-scale error ^{Notes 1, 2}	E _{ZS}	10-bit resolution	2.4 V ≤ V _{DD} ≤ 5.5 V			±0.60	%FSR
Full-scale error ^{Notes 1, 2}	E _{FS}	10-bit resolution	2.4 V ≤ V _{DD} ≤ 5.5 V			±0.60	%FSR
Integral linearity error ^{Note 1}	ILE	10-bit resolution	2.4 V ≤ V _{DD} ≤ 5.5 V			±4.0	LSB
Differential linearity error ^{Note 1}	DLE	10-bit resolution	2.4 V ≤ V _{DD} ≤ 5.5 V			±2.0	LSB
Analog input voltage	V _{AIN}	ANI0, ANI1		0		V _{DD}	V
		ANI16 to ANI23		0		EV _{DD}	V
		Internal reference voltage output (2.4 V ≤ V _{DD} ≤ 5.5 V, HS (high-speed main) mode)		V _{BGR} ^{Note 3}			V
		Temperature sensor output voltage (2.4 V ≤ V _{DD} ≤ 5.5 V, HS (high-speed main) mode)		V _{TMPS25} ^{Note 3}			V

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. Refer to 3.6.2 Temperature sensor/internal reference voltage characteristics.

3.7.3 Capacitor split method

1/3 bias method

(T_A = -40 to +105°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
V _{L4} voltage	V _{L4}	C1 to C4 = 0.47 μF ^{Note 2}		V _{DD}		V
V _{L2} voltage	V _{L2}	C1 to C4 = 0.47 μF ^{Note 2}	2/3 V _{L4} - 0.1	2/3 V _{L4}	2/3 V _{L4} + 0.1	V
V _{L1} voltage	V _{L1}	C1 to C4 = 0.47 μF ^{Note 2}	1/3 V _{L4} - 0.1	1/3 V _{L4}	1/3 V _{L4} + 0.1	V
Capacitor split wait time ^{Note 1}	t _{WAIT}		100			ms

Notes 1. This is the wait time from when voltage bucking is started (VLCON = 1) until display is enabled (LCDON = 1).

2. This is a capacitor that is connected between voltage pins used to drive the LCD.

C1: A capacitor connected between CAPH and CAPL

C2: A capacitor connected between V_{L1} and GND

C3: A capacitor connected between V_{L2} and GND

C4: A capacitor connected between V_{L4} and GND

C1 = C2 = C3 = C4 = 0.47 μF±30%