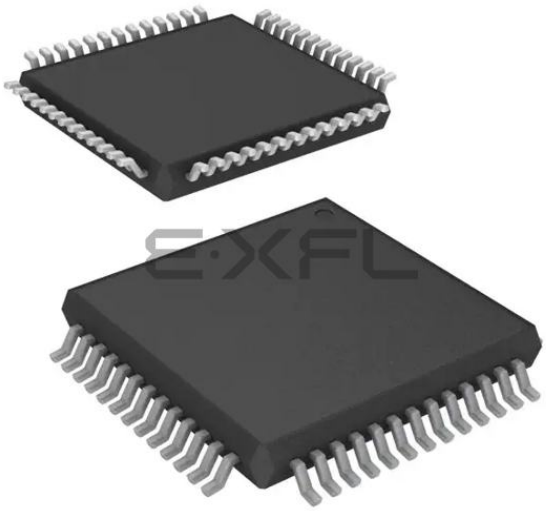
# Renesas Electronics America Inc - R5F10RJAAFA#30 Datasheet



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## What is "Embedded - Microcontrollers"?

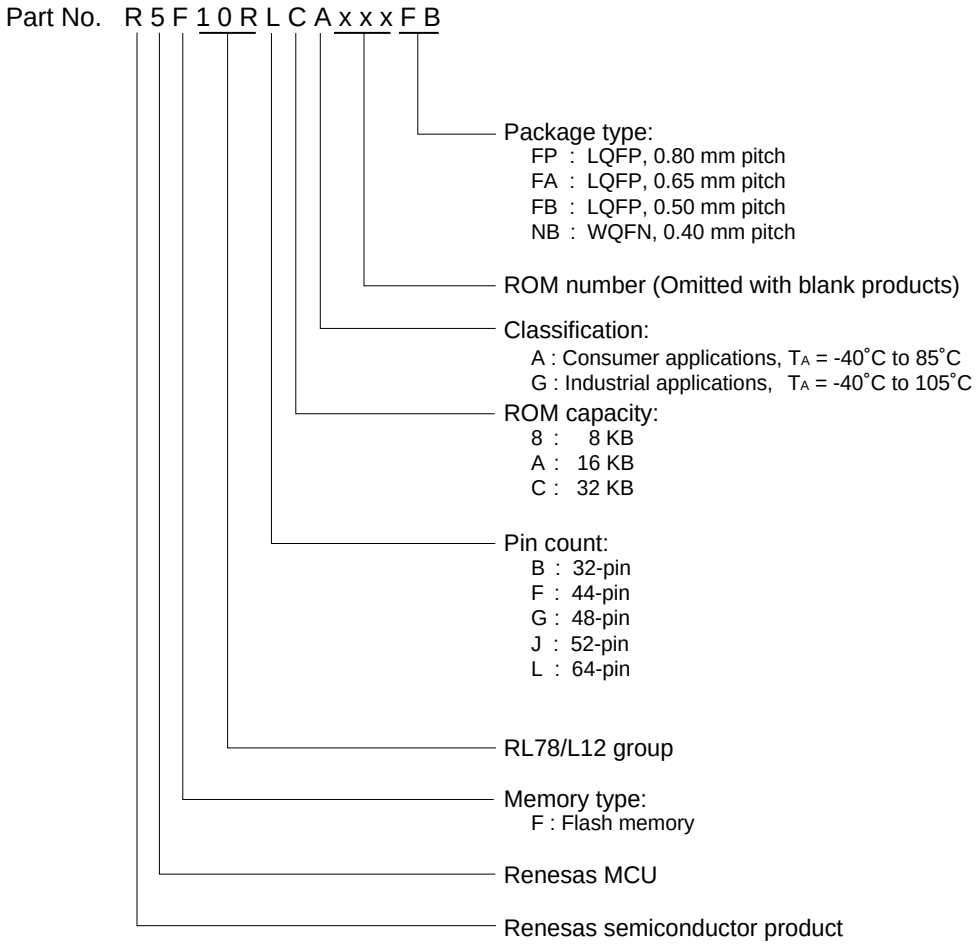
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | RL78 |
| Core Size | 16-Bit |
| Speed | 24MHz |
| Connectivity | CSI, I²C, LINbus, UART/USART |
| Peripherals | DMA, LCD, LVD, POR, PWM, WDT |
| Number of I/O | 37 |
| Program Memory Size | 16KB (16K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 2K x 8 |
| RAM Size | 1K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.6V ~ 5.5V |
| Data Converters | A/D 10x8/10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 52-LQFP |
| Supplier Device Package | 52-LQFP (10x10) |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f10rjaafa-30 |

## 1.2 List of Part Numbers

**Figure 1-1 Part Number, Memory Size, and Package of RL78/L12**



## 1.4 Pin Identification

| | | | |
|---|---|---|---|
| ANI0, ANI1, ANI16 to ANI23: | Analog Input | P130, P137: | Port 13 |
| | | P140 to P147: | Port 14 |
| $AV_{REFM}$: | Analog Reference Voltage Minus | PCLBUZ0, PCLBUZ1: | Programmable Clock Output/Buzzer Output |
| $AV_{REFP}$: | Analog Reference Voltage Plus | REGC: | Regulator Capacitance |
| | | $\overline{RESET}$: | Reset |
| CAPH, CAPL: | Capacitor for LCD | RTC1HZ: | Real-time Clock Correction Clock (1 Hz) Output |
| COM0 to COM7, | | | |
| $EV_{DD}$: | Power Supply for Port | RxD0: | Receive Data |
| $EV_{SS}$: | Ground for Port | $\overline{SCK00}$, $\overline{SCK01}$: | Serial Clock Input/Output |
| EXCLK: | External Clock Input (Main System Clock) | SCLA0: | Serial Clock Input/Output |
| | | SDAA0: | Serial Data Input/Output |
| EXCLKS: | External Clock Input (Subsystem Clock) | SEG0 to SEG38: | LCD Segment Output |
| | | SI00, SI01: | Serial Data Input |
| INTP0 to INTP7: | Interrupt Request From Peripheral | SO00, SO01: | Serial Data Output |
| | | TI00 to TI07: | Timer Input |
| KR0 to KR3: | Key Return | TO00 to TO07: | Timer Output |
| P10 to P17: | Port 1 | TOOL0: | Data Input/Output for Tool |
| P20, P21: | Port 2 | TOOLRxD, TOOLTxD: | Data Input/Output for External Device |
| P30 to P32: | Port 3 | TxD0: | Transmit Data |
| P40 to P43: | Port 4 | $V_{DD}$: | Power Supply |
| P50 to P54: | Port 5 | $V_{L1}$ to $V_{L4}$: | LCD Power Supply |
| P60, P61: | Port 6 | $V_{SS}$: | Ground |
| P70 to P74: | Port 7 | X1, X2: | Crystal Oscillator (Main System Clock) |
| P120 to P127: | Port 12 | XT1, XT2: | Crystal Oscillator (Subsystem Clock) |

## 2.2 Oscillator Characteristics

### 2.2.1 X1, XT1 oscillator characteristics

**($T_A$ = –40 to +85°C, 1.6 V ≤ $EV_{DD}$ = $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS}$ = 0 V)**

| Parameter | Resonator | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| X1 clock oscillation frequency ($f_X$)Note | Ceramic resonator/ crystal resonator | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 1.0 | | 20.0 | MHz |
| | | 2.4 V ≤ $V_{DD}$ ≤ 2.7 V | 1.0 | | 16.0 | MHz |
| | | 1.8 V ≤ $V_{DD}$ < 2.7 V | 1.0 | | 8.0 | MHz |
| | | 1.6 V ≤ $V_{DD}$ <1.8 V | 1.0 | | 4.0 | MHz |
| XT1 clock oscillation frequency ($f_{XT}$)Note | Crystal resonator | | 32 | 32.768 | 35 | kHz |

**Note** Indicates only permissible oscillator frequency ranges. Refer to **2.4 AC Characteristics** for instruction execution time. Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

**Caution Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.**

### 2.2.2 On-chip oscillator characteristics

**($T_A$ = –40 to +85°C, 1.6 V ≤ $EV_{DD}$ = $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS}$ = 0 V)**

| Oscillators | Parameters | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| High-speed on-chip oscillator clock frequency Notes 1, 2 | $f_{IH}$ | | | 1 | | 24 | MHz |
| High-speed on-chip oscillator clock frequency accuracy | | –20 to +85°C | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V | –1 | | +1 | % |
| | | | 1.6 V ≤ $V_{DD}$ < 1.8 V | –5 | | +5 | % |
| | | –40 to –20°C | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V | –1.5 | | +1.5 | % |
| | | | 1.6 V ≤ $V_{DD}$ < 1.8 V | –5.5 | | +5.5 | % |
| Low-speed on-chip oscillator clock frequency | $f_{IL}$ | | | | 15 | | kHz |
| Low-speed on-chip oscillator clock frequency accuracy | | | | –15 | | +15 | % |

**Notes 1.** High-speed on-chip oscillator frequency is selected by bits 0 to 3 of option byte (000C2H) and bits 0 to 2 of HOCODIV register.

**2.** This indicates the oscillator characteristics only. Refer to **2.4 AC Characteristics** for instruction execution time.

**($T_A$ = –40 to +85°C, 1.6 V ≤ $EV_{DD}$ = $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS}$ = 0 V)** **(3/3)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Low-speed on-chip oscillator operating current | $I_{FIL}$ Note 1 | | | | 0.20 | | μA |
| RTC operating current | $I_{RTC}$ Notes 1, 2, 3 | $f_{MAIN}$ is stopped | | | 0.08 | | μA |
| 12-bit interval timer current | $I_{IT}$ Notes 1, 2, 4 | | | | 0.08 | | μA |
| Watchdog timer operating current | $I_{WDT}$ Notes 1, 2, 5 | $f_{IL}$ = 15 kHz | | | 0.24 | | μA |
| A/D converter operating current | $I_{ADC}$ Notes 1, 6 | When conversion at maximum speed | Normal mode, $AV_{REFP}$ = $V_{DD}$ = 5.0 V | | 1.3 | 1.7 | mA |
| | | | Low voltage mode, $AV_{REFP}$ = $V_{DD}$ = 3.0 V | | 0.5 | 0.7 | mA |
| A/D converter reference voltage current | $I_{ADREF}$ Note 1 | | | | 75.0 | | μA |
| Temperature sensor operating current | $I_{TMPS}$ Note 1 | | | | 75.0 | | μA |
| LVD operating current | $I_{LVD}$ Notes 1, 7 | | | | 0.08 | | μA |
| Self-programming operating current | $I_{FSP}$ Notes 1, 9 | | | | 2.50 | 12.20 | mA |
| BGO operating current | $I_{BGO}$ Notes 1, 8 | | | | 2.00 | 12.20 | mA |
| LCD operating current | $I_{LCD1}$ Notes 11, 12 | External resistance division method | $V_{DD}$ = $EV_{DD}$ = 5.0 V, $V_{L4}$ = 5.0 V | | 0.04 | 0.20 | μA |
| | $I_{LCD2}$ Note 11 | Internal voltage boosting method | $V_{DD}$ = $EV_{DD}$ = 5.0 V, $V_{L4}$ = 5.1 V (VLCD = 12H) | | 1.12 | 3.70 | μA |
| | | | $V_{DD}$ = $EV_{DD}$ = 3.0 V, $V_{L4}$ = 3.0 V (VLCD = 04H) | | 0.63 | 2.20 | μA |
| | $I_{LCD3}$ Note 11 | Capacitor split method | $V_{DD}$ = $EV_{DD}$ = 3.0 V, $V_{L4}$ = 3.0 V | | 0.12 | 0.50 | μA |
| SNOOZE operating current | $I_{SNOZ}$ Note 1 | ADC operation | The mode is performed Note 10 | | 0.50 | 0.60 | mA |
| | | | The A/D conversion operations are performed, Low voltage mode, $AV_{REFP}$ = $V_{DD}$ = 3.0 V | | 1.20 | 1.44 | mA |
| | | CSI/UART operation | | | 0.70 | 0.84 | mA |

(**Notes** and **Remarks** are listed on the next page.)

**(2) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output)**

**($T_A$ = –40 to +85°C, 1.6 V ≤ $EV_{DD}$ = $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | | HS (high-speed main) Mode | | LS (low-speed main) Mode | | LV (low-voltage main) Mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SCKp cycle time | $t_{KCY1}$ | 2.7 V ≤ $EV_{DD}$ ≤ 5.5 V | | 167 Note 1 | | 500 Note 1 | | 1000 Note 1 | | ns |
| | | 2.4 V ≤ $EV_{DD}$ ≤ 5.5 V | | 250 Note 1 | | 500 Note 1 | | 1000 Note 1 | | ns |
| | | 1.8 V ≤ $EV_{DD}$ ≤ 5.5 V | | | | 500 Note 1 | | 1000 Note 1 | | ns |
| | | 1.6 V ≤ $EV_{DD}$ ≤ 5.5 V | | | | | | 1000 Note 1 | | ns |
| SCKp high-/low-level width | $t_{KH1}$, $t_{KL1}$ | 4.0 V ≤ $EV_{DD}$ ≤ 5.5 V | | $t_{KCY1}$/2 – 12 | | $t_{KCY1}$/2 – 50 | | $t_{KCY1}$/2 – 50 | | ns |
| | | 2.7 V ≤ $EV_{DD}$ ≤ 5.5 V | | $t_{KCY1}$/2 – 18 | | $t_{KCY1}$/2 – 50 | | $t_{KCY1}$/2 – 50 | | ns |
| | | 2.4 V ≤ $EV_{DD}$ ≤ 5.5 V | | $t_{KCY1}$/2 – 38 | | $t_{KCY1}$/2 – 50 | | $t_{KCY1}$/2 – 50 | | ns |
| | | 1.8 V ≤ $EV_{DD}$ ≤ 5.5 V | | | | $t_{KCY1}$/2 – 50 | | $t_{KCY1}$/2 – 50 | | ns |
| | | 1.6 V ≤ $EV_{DD}$ ≤ 5.5 V | | | | | | $t_{KCY1}$/2 – 100 | | ns |
| SIp setup time (to SCKp↑) Note 2 | $t_{SIK1}$ | 2.7 V ≤ $EV_{DD}$ ≤ 5.5 V | | 44 | | 110 | | 110 | | ns |
| | | 2.4 V ≤ $EV_{DD}$ ≤ 5.5 V | | 75 | | 110 | | 110 | | ns |
| | | 1.8 V ≤ $EV_{DD}$ ≤ 5.5 V | | | | 110 | | 110 | | ns |
| | | 1.6 V ≤ $EV_{DD}$ ≤ 5.5 V | | | | | | 220 | | ns |
| SIp hold time (from SCKp↑) Note 3 | $t_{KSI1}$ | 2.4 V ≤ $EV_{DD}$ ≤ 5.5 V | | 19 | | 19 | | 19 | | ns |
| | | 1.8 V ≤ $EV_{DD}$ ≤ 5.5 V | | | | 19 | | 19 | | |
| | | 1.6 V ≤ $EV_{DD}$ ≤ 5.5 V | | | | | | 19 | | |
| Delay time from SCKp↓ to SOp output Note 4 | $t_{KSO1}$ | C = 30 pF Note 5 | 2.4 V ≤ $EV_{DD}$ ≤ 5.5 V | | 25 | | 25 | | 25 | ns |
| | | | 1.8 V ≤ $EV_{DD}$ ≤ 5.5 V | | | | 25 | | 25 | |
| | | | 1.6 V ≤ $EV_{DD}$ ≤ 5.5 V | | | | | | 25 | |

**Notes 1.** For CSI00, set a cycle of 2/$f_{MCK}$ or longer. For CSI01, set a cycle of 4/$f_{MCK}$ or longer.

**2.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**3.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**4.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**5.** C is the load capacitance of the SCKp and SOp output lines.

**Caution Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).**

(**Remarks** are listed on the next page.)

**Notes 1.** For CSI00, set a cycle of 2/$f_{MCK}$ or longer. For CSI01, set a cycle of 4/$f_{MCK}$ or longer.

**2.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

**3.** When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output ($V_{DD}$ tolerance (32-pin to 52-pin products)/$EV_{DD}$ tolerance (64-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

**Remarks 1.** $R_b$[Ω]:Communication line (SCKp, SOp) pull-up resistance, $C_b$[F]: Communication line (SCKp, SOp) load capacitance, $V_b$[V]: Communication line voltage

**2.** p: CSI number (p = 00, 01), m: Unit number (m = 0), n: Channel number (n = 0, 1), g: PIM and POM number (g = 1)

**3.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 01)

**(7) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (slave mode, SCKp... external clock input)**

**($T_A$ = –40 to +85°C, 1.8 V ≤ $EV_{DD}$ = $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS}$ = 0 V) (1/2)**

| Parameter | Symbol | Conditions | | HS (high-speed main) mode | | LS (low-speed main) mode | | LV (low-voltage main) mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SCKp cycle time Note 1 | $t_{KCY2}$ | 4.0 V ≤ $EV_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V | 20 MHz < $f_{MCK}$ ≤ 24 MHz | 12/$f_{MCK}$ | | | | | | ns |
| | | | 8 MHz < $f_{MCK}$ ≤ 20 MHz | 10/$f_{MCK}$ | | | | | | ns |
| | | | 4 MHz < $f_{MCK}$ ≤ 8 MHz | 8/$f_{MCK}$ | | 16/$f_{MCK}$ | | | | ns |
| | | | $f_{MCK}$ ≤ 4 MHz | 6/$f_{MCK}$ | | 10/$f_{MCK}$ | | 10/$f_{MCK}$ | | ns |
| | | 2.7 V ≤ $EV_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V | 20 MHz < $f_{MCK}$ ≤ 24 MHz | 16/$f_{MCK}$ | | | | | | ns |
| | | | 16 MHz < $f_{MCK}$ ≤ 20 MHz | 14/$f_{MCK}$ | | | | | | ns |
| | | | 8 MHz < $f_{MCK}$ ≤ 16 MHz | 12/$f_{MCK}$ | | | | | | ns |
| | | | 4 MHz < $f_{MCK}$ ≤ 8 MHz | 8/$f_{MCK}$ | | 16/$f_{MCK}$ | | | | ns |
| | | | $f_{MCK}$ ≤ 4 MHz | 6/$f_{MCK}$ | | 10/$f_{MCK}$ | | 10/$f_{MCK}$ | | ns |
| | | 2.4 V ≤ $EV_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V | 20 MHz < $f_{MCK}$ ≤ 24 MHz | 36/$f_{MCK}$ | | | | | | ns |
| | | | 16 MHz < $f_{MCK}$ ≤ 20 MHz | 32/$f_{MCK}$ | | | | | | ns |
| | | | 8 MHz < $f_{MCK}$ ≤ 16 MHz | 26/$f_{MCK}$ | | | | | | ns |
| | | | 4 MHz < $f_{MCK}$ ≤ 8 MHz | 16/$f_{MCK}$ | | 16/$f_{MCK}$ | | | | ns |
| | | | $f_{MCK}$ ≤ 4 MHz | 10/$f_{MCK}$ | | 10/$f_{MCK}$ | | 10/$f_{MCK}$ | | ns |
| | | 1.8 V ≤ $EV_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 2 | 4 MHz < $f_{MCK}$ ≤ 8 MHz | | | 16/$f_{MCK}$ | | | | ns |
| | | | $f_{MCK}$ ≤ 4 MHz | | | 10/$f_{MCK}$ | | 10/$f_{MCK}$ | | ns |
| SCKp high-/low-level width | $t_{KH2}$, $t_{KL2}$ | 4.0 V ≤ $EV_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V | | $t_{KCY2}$/2 – 12 | | $t_{KCY2}$/2 – 50 | | $t_{KCY2}$/2 – 50 | | ns |
| | | 2.7 V ≤ $EV_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V | | $t_{KCY2}$/2 – 18 | | $t_{KCY2}$/2 – 50 | | $t_{KCY2}$/2 – 50 | | ns |
| | | 2.4 V ≤ $EV_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V | | $t_{KCY2}$/2 – 50 | | $t_{KCY2}$/2 – 50 | | $t_{KCY2}$/2 – 50 | | ns |
| | | 1.8 V ≤ $EV_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 2 | | | | $t_{KCY2}$/2 – 50 | | $t_{KCY2}$/2 – 50 | | ns |
| SIp setup time (to SCKp↑) Note 3 | $t_{SIK2}$ | 4.0 V ≤ $EV_{DD}$ < 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V | | 1/$f_{MCK}$ + 20 | | 1/$f_{MCK}$ + 30 | | 1/$f_{MCK}$ + 30 | | ns |
| | | 2.7 V ≤ $EV_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V | | 1/$f_{MCK}$ + 20 | | 1/$f_{MCK}$ + 30 | | 1/$f_{MCK}$ + 30 | | ns |
| | | 2.4 V ≤ $EV_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V | | 1/$f_{MCK}$ + 30 | | 1/$f_{MCK}$ + 30 | | 1/$f_{MCK}$ + 30 | | ns |
| | | 1.8 V ≤ $EV_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 2 | | | | 1/$f_{MCK}$ + 30 | | 1/$f_{MCK}$ + 30 | | ns |
| SIp hold time (from SCKp↑) Note 4 | $t_{KSI2}$ | 4.0 V ≤ $EV_{DD}$ < 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V | | 1/$f_{MCK}$ + 31 | | 1/$f_{MCK}$ + 31 | | 1/$f_{MCK}$ + 31 | | ns |
| | | 2.7 V ≤ $EV_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V | | 1/$f_{MCK}$ + 31 | | 1/$f_{MCK}$ + 31 | | 1/$f_{MCK}$ + 31 | | ns |
| | | 2.4 V ≤ $EV_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V | | 1/$f_{MCK}$ + 31 | | 1/$f_{MCK}$ + 31 | | 1/$f_{MCK}$ + 31 | | ns |
| | | 1.8 V ≤ $EV_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 2 | | | | 1/$f_{MCK}$ + 31 | | 1/$f_{MCK}$ + 31 | | ns |

(**Notes**, **Caution** and **Remarks** are listed on the next page.)

**Notes 1.** The first clock pulse is generated after this period when the start/restart condition is detected.

**2.** The maximum value (MAX.) of $t_{HD:DAT}$ is during normal transfer and a wait state is inserted in the $\overline{ACK}$ (acknowledge) timing.

**Remark** The maximum value of Cb (communication line capacitance) and the value of Rb (communication line pull-up resistor) at that time in each mode are as follows.

Standard mode: $C_b$ = 400 pF, $R_b$ = 2.7 kΩ

**LVD Detection Voltage of Interrupt & Reset Mode**

**($T_A$ = –40 to +85°C, $V_{PDR} \leq EV_{DD} = V_{DD} \leq 5.5$ V, $V_{SS} = EV_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|
| Interrupt and reset mode | $V_{LVDA0}$ | $V_{POC2}$, $V_{POC1}$, $V_{POC0}$ = 0, 0, 0, falling reset voltage | | | 1.60 | 1.63 | 1.66 | V |
| | $V_{LVDA1}$ | LVIS1, LVIS0 = 1, 0 | | Rising release reset voltage | 1.74 | 1.77 | 1.81 | V |
| | | | | Falling interrupt voltage | 1.70 | 1.73 | 1.77 | V |
| | $V_{LVDA2}$ | LVIS1, LVIS0 = 0, 1 | | Rising release reset voltage | 1.84 | 1.88 | 1.91 | V |
| | | | | Falling interrupt voltage | 1.80 | 1.84 | 1.87 | V |
| | $V_{LVDA3}$ | LVIS1, LVIS0 = 0, 0 | | Rising release reset voltage | 2.86 | 2.92 | 2.97 | V |
| | | | | Falling interrupt voltage | 2.80 | 2.86 | 2.91 | V |
| | $V_{LVDB1}$ | $V_{POC2}$, $V_{POC1}$, $V_{POC0}$ = 0, 0, 1, falling reset voltage | | | 1.80 | 1.84 | 1.87 | V |
| | $V_{LVDB2}$ | LVIS1, LVIS0 = 1, 0 | | Rising release reset voltage | 1.94 | 1.98 | 2.02 | V |
| | | | | Falling interrupt voltage | 1.90 | 1.94 | 1.98 | V |
| | $V_{LVDB3}$ | LVIS1, LVIS0 = 0, 1 | | Rising release reset voltage | 2.05 | 2.09 | 2.13 | V |
| | | | | Falling interrupt voltage | 2.00 | 2.04 | 2.08 | V |
| | $V_{LVDB4}$ | LVIS1, LVIS0 = 0, 0 | | Rising release reset voltage | 3.07 | 3.13 | 3.19 | V |
| | | | | Falling interrupt voltage | 3.00 | 3.06 | 3.12 | V |
| | $V_{LVDC0}$ | $V_{POC2}$, $V_{POC1}$, $V_{POC0}$ = 0, 1, 0, falling reset voltage | | | 2.40 | 2.45 | 2.50 | V |
| | $V_{LVDC1}$ | LVIS1, LVIS0 = 1, 0 | | Rising release reset voltage | 2.56 | 2.61 | 2.66 | V |
| | | | | Falling interrupt voltage | 2.50 | 2.55 | 2.60 | V |
| | $V_{LVDC2}$ | LVIS1, LVIS0 = 0, 1 | | Rising release reset voltage | 2.66 | 2.71 | 2.76 | V |
| | | | | Falling interrupt voltage | 2.60 | 2.65 | 2.70 | V |
| | $V_{LVDC3}$ | LVIS1, LVIS0 = 0, 0 | | Rising release reset voltage | 3.68 | 3.75 | 3.82 | V |
| | | | | Falling interrupt voltage | 3.60 | 3.67 | 3.74 | V |
| | $V_{LVDD0}$ | $V_{POC2}$, $V_{POC1}$, $V_{POC0}$ = 0, 1, 1, falling reset voltage | | | 2.70 | 2.75 | 2.81 | V |
| | $V_{LVDD1}$ | LVIS1, LVIS0 = 1, 0 | | Rising release reset voltage | 2.86 | 2.92 | 2.97 | V |
| | | | | Falling interrupt voltage | 2.80 | 2.86 | 2.91 | V |
| | $V_{LVDD2}$ | LVIS1, LVIS0 = 0, 1 | | Rising release reset voltage | 2.96 | 3.02 | 3.08 | V |
| | | | | Falling interrupt voltage | 2.90 | 2.96 | 3.02 | V |
| | $V_{LVDD3}$ | LVIS1, LVIS0 = 0, 0 | | Rising release reset voltage | 3.98 | 4.06 | 4.14 | V |
| | | | | Falling interrupt voltage | 3.90 | 3.98 | 4.06 | V |

## 2.6.5 Supply voltage rise time

**($T_A$ = –40 to +85°C, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Power supply voltage rising slope | $S_{VDD}$ | | | | 54 | V/ms |

**Caution Make sure to keep the internal reset state by the LVD circuit or an external reset until $V_{DD}$ reaches the operating voltage range shown in 30.4 AC Characteristics.**

# 3. ELECTRICAL SPECIFICATIONS (G: $T_A$ = -40 to +105°C)

**This chapter describes the electrical specifications for the products "G: Industrial applications ($T_A$ = -40 to +105°C)".**

**Cautions 1. The RL78 microcontrollers have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.**

**2. With products not provided with an $EV_{DD}$ or $EV_{SS}$ pin, replace $EV_{DD}$ with $V_{DD}$, or replace $EV_{SS}$ with $V_{SS}$.**

**3. For derating with $T_A$ = +85 to +105°C, contact our Sales Division or the vender's sales division. Derating means the specified reduction in an operating parameter to improve reliability.**

## 3.1 Absolute Maximum Ratings

**Absolute Maximum Ratings ($T_A$ = 25°C) (1/3)**

| Parameter | Symbols | Conditions | Ratings | Unit |
|---|---|---|---|---|
| Supply voltage | $V_{DD}$ | $V_{DD}$ = $EV_{DD}$ | −0.5 to +6.5 | V |
| | $EV_{DD}$ | $V_{DD}$ = $EV_{DD}$ | −0.5 to +6.5 | V |
| | $EV_{SS}$ | | −0.5 to +0.3 | V |
| REGC pin input voltage | $V_{IREGC}$ | REGC | −0.3 to +2.8 and −0.3 to $V_{DD}$ + 0.3 Note 1 | V |
| Input voltage | $V_{I1}$ | P10 to P17, P30 to P32, P40 to P43, P50 to P54, P70 to P74, P120, P125 to P127, P140 to P147 | −0.3 to $EV_{DD}$ + 0.3 and −0.3 to $V_{DD}$ + 0.3 Note 2 | V |
| | $V_{I2}$ | P60, P61 (N-ch open-drain) | −0.3 to $EV_{DD}$ + 0.3 and −0.3 to $V_{DD}$ + 0.3 Note 2 | V |
| | $V_{I3}$ | P20, P21, P121 to P124, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$ | −0.3 to $V_{DD}$ + 0.3 Note 2 | V |
| Output voltage | $V_{O1}$ | P10 to P17, P30 to P32, P40 to P43, P50 to P54, P60, P61, P70 to P74, P120, P125 to P127, P130, P140 to P147 | −0.3 to $EV_{DD}$ + 0.3 and −0.3 to $V_{DD}$ + 0.3 Note 2 | V |
| | $V_{O2}$ | P20, P21 | −0.3 to $V_{DD}$ + 0.3 Note 2 | V |
| Analog input voltage | $V_{AI1}$ | ANI16 to ANI23 | −0.3 to $EV_{DD}$ + 0.3 and −0.3 to $AV_{REF}$(+) + 0.3 Notes 2, 3 | V |
| | $V_{AI2}$ | ANI0, ANI1 | −0.3 to $V_{DD}$ + 0.3 and −0.3 to $AV_{REF}$(+) + 0.3 Notes 2, 3 | V |

**Notes 1.** Connect the REGC pin to Vss via a capacitor (0.47 to 1 $\mu$F). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.

**2.** Must be 6.5 V or lower.

**3.** Do not exceed $AV_{REF}$(+) + 0.3 V in case of A/D conversion target pin.

**Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.**

**Remarks 1.** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

**2.** $AV_{REF}$(+) : + side reference voltage of the A/D converter.

**3.** $V_{SS}$ : Reference voltage

**Absolute Maximum Ratings ($T_A$ = 25°C) (2/3)**

| Parameter | Symbols | Conditions | | Ratings | Unit |
|---|---|---|---|---|---|
| LCD voltage | $V_{L1}$ | $V_{L1}$ voltage[Note 1] | | –0.3 to +2.8 and –0.3 to $V_{L4}$ + 0.3 | V |
| | $V_{L2}$ | $V_{L2}$ voltage[Note 1] | | –0.3 to $V_{L4}$ + 0.3[Note 2] | V |
| | $V_{L3}$ | $V_{L3}$ voltage[Note 1] | | –0.3 to $V_{L4}$ + 0.3[Note 2] | V |
| | $V_{L4}$ | $V_{L4}$ voltage[Note 1] | | –0.3 to +6.5 | V |
| | $V_{LCAP}$ | CAPL, CAPH voltage[Note 1] | | –0.3 to $V_{L4}$ + 0.3[Note 2] | V |
| | $V_{LOUT}$ | COM0 to COM7, SEG0 to SEG38, output voltage | External resistance division method | –0.3 to $V_{DD}$ + 0.3[Note 2] | V |
| | | | Capacitor split method | –0.3 to $V_{DD}$ + 0.3[Note 2] | |
| | | | Internal voltage boosting method | –0.3 to $V_{L4}$ + 0.3[Note 2] | |

**Notes 1.** This value only indicates the absolute maximum ratings when applying voltage to the $V_{L1}$, $V_{L2}$, $V_{L3}$, and $V_{L4}$ pins; it does not mean that applying voltage to these pins is recommended. When using the internal voltage boosting method or capacitance split method, connect these pins to $V_{SS}$ via a capacitor (0.47 $\mu$F ± 30%) and connect a capacitor (0.47 $\mu$F ± 30%) between the CAPL and CAPH pins.

**2.** Must be 6.5 V or lower.

**Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.**

**Remark** $V_{SS}$ : Reference voltage

## 3.3.2 Supply current characteristics

**($T_A$ = –40 to +105°C, 2.4 V ≤ $EV_{DD}$ = $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS}$ = 0 V)** **(1/3)**

| Parameter | Symbol | Conditions | | | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| Supply current Note 1 | $I_{DD1}$ | Operating mode | HS (high-speed main) mode Note 5 | $f_{IH}$ = 24 MHz Note 3 | Basic operation | $V_{DD}$ = 5.0 V | | 1.5 | | mA |
| | | | | | | $V_{DD}$ = 3.0 V | | 1.5 | | mA |
| | | | | | Normal operation | $V_{DD}$ = 5.0 V | | 3.3 | 5.3 | mA |
| | | | | | | $V_{DD}$ = 3.0 V | | 3.3 | 5.3 | mA |
| | | | | $f_{IH}$ = 16 MHz Note 3 | Normal operation | $V_{DD}$ = 5.0 V | | 2.5 | 3.9 | mA |
| | | | | | | $V_{DD}$ = 3.0 V | | 2.5 | 3.9 | mA |
| | | | HS (high-speed main) mode Note 5 | $f_{MX}$ = 20 MHz Note 2, $V_{DD}$ = 5.0 V | Normal operation | Square wave input | | 2.8 | 4.7 | mA |
| | | | | | | Resonator connection | | 3.0 | 4.8 | mA |
| | | | | $f_{MX}$ = 20 MHz Note 2, $V_{DD}$ = 3.0 V | Normal operation | Square wave input | | 2.8 | 4.7 | mA |
| | | | | | | Resonator connection | | 3.0 | 4.8 | mA |
| | | | | $f_{MX}$ = 10 MHz Note 2, $V_{DD}$ = 5.0 V | Normal operation | Square wave input | | 1.8 | 2.8 | mA |
| | | | | | | Resonator connection | | 1.8 | 2.8 | mA |
| | | | | $f_{MX}$ = 10 MHz Note 2, $V_{DD}$ = 3.0 V | Normal operation | Square wave input | | 1.8 | 2.8 | mA |
| | | | | | | Resonator connection | | 1.8 | 2.8 | mA |
| | | | Subsystem clock operation | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = –40°C | Normal operation | Square wave input | | 3.5 | 4.9 | μA |
| | | | | | | Resonator connection | | 3.6 | 5.0 | μA |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = +25°C | Normal operation | Square wave input | | 3.6 | 4.9 | μA |
| | | | | | | Resonator connection | | 3.7 | 5.0 | μA |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = +50°C | Normal operation | Square wave input | | 3.7 | 5.5 | μA |
| | | | | | | Resonator connection | | 3.8 | 5.6 | μA |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = +70°C | Normal operation | Square wave input | | 3.8 | 6.3 | μA |
| | | | | | | Resonator connection | | 3.9 | 6.4 | μA |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = +85°C | Normal operation | Square wave input | | 4.1 | 7.7 | μA |
| | | | | | | Resonator connection | | 4.2 | 7.8 | μA |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = +105°C | Normal operation | Square wave input | | 6.4 | 19.7 | μA |
| | | | | | | Resonator connection | | 6.5 | 19.8 | μA |

(**Notes** and **Remarks** are listed on the next page.)

**(4) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (1/2)**

**($T_A$ = –40 to +105°C, 2.4 V ≤ $EV_{DD}$ = $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | | | HS (high-speed main) Mode | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | MIN. | MAX. | |
| Transfer rate | | Reception | 4.0 V ≤ $EV_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V | | | $f_{MCK}$/12 Note 1 | bps |
| | | | | Theoretical value of the maximum transfer rate $f_{MCK}$ = $f_{CLK}$ Note 2 | | 2.0 | Mbps |
| | | | 2.7 V ≤ $EV_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V | | | $f_{MCK}$/12 Note 1 | bps |
| | | | | Theoretical value of the maximum transfer rate $f_{MCK}$ = $f_{CLK}$ Note 2 | | 2.0 | Mbps |
| | | | 2.4 V ≤ $EV_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V | | | $f_{MCK}$/12 Note 1 | bps |
| | | | | Theoretical value of the maximum transfer rate $f_{MCK}$ = $f_{CLK}$ Note 2 | | 2.0 | Mbps |

**Notes 1.** Transfer rate in the SNOOZE mode is 4800 bps only.

**2.** The maximum operating frequencies of the CPU/peripheral hardware clock ($f_{CLK}$) are:
HS (high-speed main) mode: 24 MHz (2.7 V ≤ $V_{DD}$ ≤ 5.5 V)
16 MHz (2.4 V ≤ $V_{DD}$ ≤ 5.5 V)

**Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output ($V_{DD}$ tolerance (32- to 52-pin products)/$EV_{DD}$ tolerance (64-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

**Remarks 1.** $V_b$[V]: Communication line voltage

**2.** q: UART number (q = 0), g: PIM and POM number (g = 1)

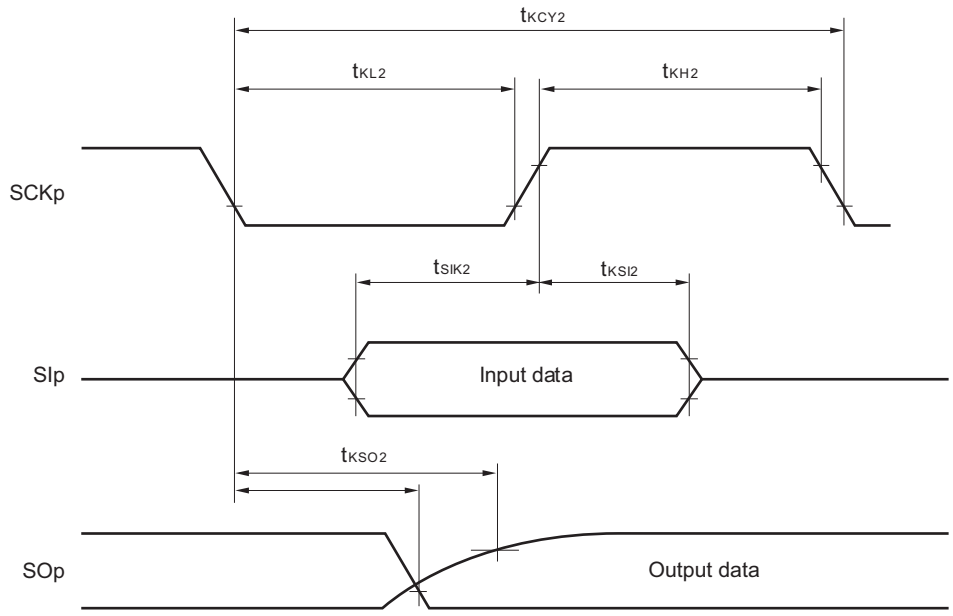
**3.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 01)

**(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (slave mode, SCKp... external clock input)**
**($T_A$ = –40 to +105°C, 2.4 V ≤ $EV_{DD}$ = $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS}$ = 0 V)**

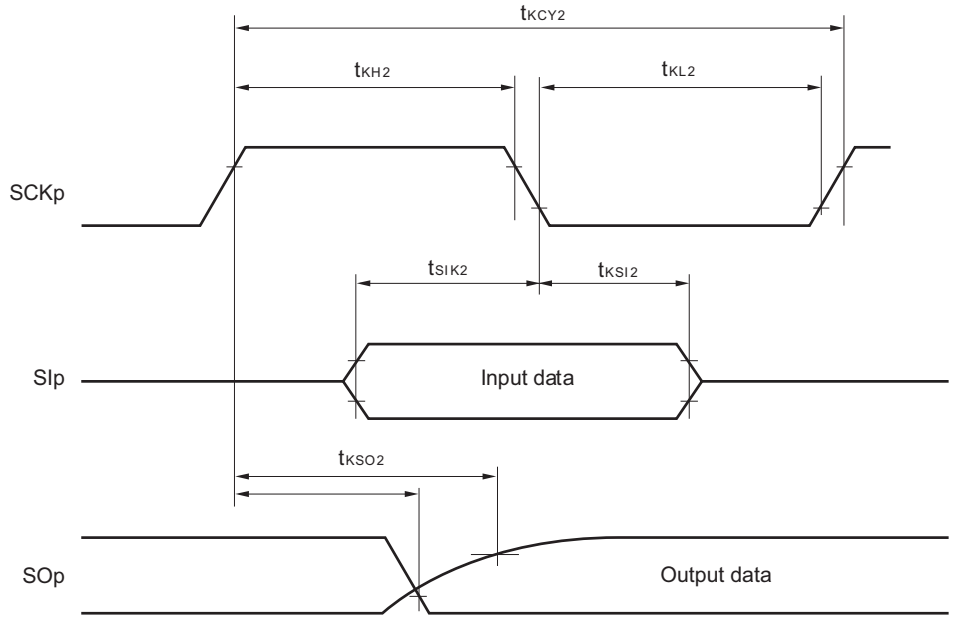
| Parameter | Symbol | Conditions | | HS (high-speed main) Mode | | Unit |
|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | |
| SCKp cycle time Note 1 | $t_{KCY2}$ | 4.0 V ≤ $EV_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V | 20 MHz < $f_{MCK}$ ≤ 24 MHz | 24/$f_{MCK}$ | | ns |
| | | | 8 MHz < $f_{MCK}$ ≤ 20 MHz | 20/$f_{MCK}$ | | ns |
| | | | 4 MHz < $f_{MCK}$ ≤ 8 MHz | 16/$f_{MCK}$ | | ns |
| | | | $f_{MCK}$ ≤ 4 MHz | 12/$f_{MCK}$ | | ns |
| | | 2.7 V ≤ $EV_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V | 20 MHz < $f_{MCK}$ ≤ 24 MHz | 32/$f_{MCK}$ | | ns |
| | | | 16 MHz < $f_{MCK}$ ≤ 20 MHz | 28/$f_{MCK}$ | | ns |
| | | | 8 MHz < $f_{MCK}$ ≤ 16 MHz | 24/$f_{MCK}$ | | ns |
| | | | 4 MHz < $f_{MCK}$ ≤ 8 MHz | 16/$f_{MCK}$ | | ns |
| | | | $f_{MCK}$ ≤ 4 MHz | 12/$f_{MCK}$ | | ns |
| | | 2.4 V ≤ $EV_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V | 20 MHz < $f_{MCK}$ ≤ 24 MHz | 72/$f_{MCK}$ | | ns |
| | | | 16 MHz < $f_{MCK}$ ≤ 20 MHz | 64/$f_{MCK}$ | | ns |
| | | | 8 MHz < $f_{MCK}$ ≤ 16 MHz | 52/$f_{MCK}$ | | ns |
| | | | 4 MHz < $f_{MCK}$ ≤ 8 MHz | 32/$f_{MCK}$ | | ns |
| | | | $f_{MCK}$ ≤ 4 MHz | 20/$f_{MCK}$ | | ns |
| SCKp high-/low-level width | $t_{KH2}$, $t_{KL2}$ | 4.0 V ≤ $EV_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V | | $t_{KCY2}$/2 – 24 | | ns |
| | | 2.7 V ≤ $EV_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V | | $t_{KCY2}$/2 – 36 | | ns |
| | | 2.4 V ≤ $EV_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V | | $t_{KCY2}$/2 – 100 | | ns |
| SIp setup time (to SCKp↑) Note2 | $t_{SIK2}$ | 4.0 V ≤ $EV_{DD}$ < 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V | | 1/$f_{MCK}$ + 40 | | ns |
| | | 2.7 V ≤ $EV_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V | | 1/$f_{MCK}$ + 40 | | ns |
| | | 2.4 V ≤ $EV_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V | | 1/$f_{MCK}$ + 60 | | ns |
| SIp hold time (from SCKp↑) Note 3 | $t_{KSI2}$ | 4.0 V ≤ $EV_{DD}$ < 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V | | 1/$f_{MCK}$ + 62 | | ns |
| | | 2.7 V ≤ $EV_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V | | 1/$f_{MCK}$ + 62 | | ns |
| | | 2.4 V ≤ $EV_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V | | 1/$f_{MCK}$ + 62 | | ns |
| Delay time from SCKp↓ to SOp output Note 4 | $t_{KSO2}$ | 4.0 V ≤ $EV_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | | | 2/$f_{MCK}$ + 240 | ns |
| | | 2.7 V ≤ $EV_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | | | 2/$f_{MCK}$ + 428 | ns |
| | | 2.4 V ≤ $EV_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | | | 2/$f_{MCK}$ + 1146 | ns |

(**Notes**, **Caution** and **Remarks** are listed on the page after the next page.)

**CSI mode serial transfer timing (slave mode) (during communication at different potential)**
**(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)**




**CSI mode serial transfer timing (slave mode) (during communication at different potential)**
**(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)**




**Remark** p: CSI number (p = 00, 01), m: Unit number (m = 0),
n: Channel number (n = 0, 1), g: PIM and POM number (g = 1)

## 3.6 Analog Characteristics

### 3.6.1 A/D converter characteristics

Classification of A/D converter characteristics

| Input channel | Reference Voltage | | |
|---|---|---|---|
| | Reference voltage (+) = $AV_{REFP}$<br>Reference voltage (–) = $AV_{REFM}$ | Reference voltage (+) = $V_{DD}$<br>Reference voltage (–) = $V_{SS}$ | Reference voltage (+) = $V_{BGR}$<br>Reference voltage (–) = $AV_{REFM}$ |
| ANI0, ANI1 | – | Refer to **3.6.1 (3)**. | Refer to **3.6.1 (4)**. |
| ANI16 to ANI23 | Refer to **3.6.1 (2)**. | | |
| Internal reference voltage<br>Temperature sensor output voltage | Refer to **3.6.1 (1)**. | | – |

**(1) When reference voltage (+) = $AV_{REFP}$/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (–) = $AV_{REFM}$/ANI1 (ADREFM = 1), target pin : internal reference voltage, and temperature sensor output voltage**

**($T_A$ = –40 to +105°C, 2.4 V ≤ $EV_{DD}$ = $V_{DD}$ ≤ 5.5 V, 2.4 V ≤ $AV_{REFP}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS}$ = 0 V, Reference voltage (+) = $AV_{REFP}$, Reference voltage (–) = $AV_{REFM}$ = 0 V)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Resolution | RES | | | 8 | | 10 | bit |
| Overall error[Note 1] | AINL | 10-bit resolution<br>$AV_{REFP}$ = $V_{DD}$ [Note 3] | 2.4 V ≤ $AV_{REFP}$ ≤ 5.5 V | | 1.2 | ±3.5 | LSB |
| Conversion time | $t_{CONV}$ | 10-bit resolution<br>Target pin: Internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode) | 3.6 V ≤ $V_{DD}$ ≤ 5.5 V | 2.375 | | 39 | μs |
| | | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 3.5625 | | 39 | μs |
| | | | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | 17 | | 39 | μs |
| Zero-scale error[Notes 1, 2] | $E_{ZS}$ | 10-bit resolution<br>$AV_{REFP}$ = $V_{DD}$ [Note 3] | 1.8 V ≤ $AV_{REFP}$ ≤ 5.5 V | | | ±0.25 | %FSR |
| Full-scale error[Notes 1, 2] | $E_{FS}$ | 10-bit resolution<br>$AV_{REFP}$ = $V_{DD}$ [Note 3] | 1.8 V ≤ $AV_{REFP}$ ≤ 5.5 V | | | ±0.25 | %FSR |
| Integral linearity error [Note 1] | ILE | 10-bit resolution<br>$AV_{REFP}$ = $V_{DD}$ [Note 3] | 1.8 V ≤ $AV_{REFP}$ ≤ 5.5 V | | | ±2.5 | LSB |
| Differential linearity error [Note 1] | DLE | 10-bit resolution<br>$AV_{REFP}$ = $V_{DD}$ [Note 3] | 1.8 V ≤ $AV_{REFP}$ ≤ 5.5 V | | | ±1.5 | LSB |
| Analog input voltage | $V_{AIN}$ | Internal reference voltage<br>(2.4 V ≤ $V_{DD}$ ≤ 5.5 V, HS (high-speed main) mode) | | $V_{BGR}$ [Note 4] | | | V |
| | | Temperature sensor output voltage<br>(2.4 V ≤ $V_{DD}$ ≤ 5.5 V, HS (high-speed main) mode) | | $V_{TMPS25}$ [Note 4] | | | V |

**Notes 1.** Excludes quantization error (±1/2 LSB).

**2.** This value is indicated as a ratio (%FSR) to the full-scale value.

**3.** When $AV_{REFP}$ < $V_{DD}$, the MAX. values are as follows.
Overall error: Add ±1.0 LSB to the MAX. value when $AV_{REFP}$ = $V_{DD}$.
Zero-scale error/Full-scale error: Add ±0.05%FSR to the MAX. value when $AV_{REFP}$ = $V_{DD}$.
Integral linearity error/ Differential linearity error: Add ±0.5 LSB to the MAX. value when $AV_{REFP}$ = $V_{DD}$.

**4.** Refer to **3.6.2 Temperature sensor/internal reference voltage characteristics**.

### 3.7.3 Capacitor split method

**1/3 bias method**

**($T_A$ = –40 to +105°C, 2.4 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| $V_{L4}$ voltage | $V_{L4}$ | C1 to C4 = 0.47 μF[Note 2] | | $V_{DD}$ | | V |
| $V_{L2}$ voltage | $V_{L2}$ | C1 to C4 = 0.47 μF[Note 2] | 2/3 $V_{L4}$ – 0.1 | 2/3 $V_{L4}$ | 2/3 $V_{L4}$ + 0.1 | V |
| $V_{L1}$ voltage | $V_{L1}$ | C1 to C4 = 0.47 μF[Note 2] | 1/3 $V_{L4}$ – 0.1 | 1/3 $V_{L4}$ | 1/3 $V_{L4}$ + 0.1 | V |
| Capacitor split wait time[Note 1] | $t_{VWAIT}$ | | 100 | | | ms |

**Notes 1.** This is the wait time from when voltage bucking is started (VLCON = 1) until display is enabled (LCDON = 1).

**2.** This is a capacitor that is connected between voltage pins used to drive the LCD.

C1: A capacitor connected between CAPH and CAPL

C2: A capacitor connected between $V_{L1}$ and GND

C3: A capacitor connected between $V_{L2}$ and GND

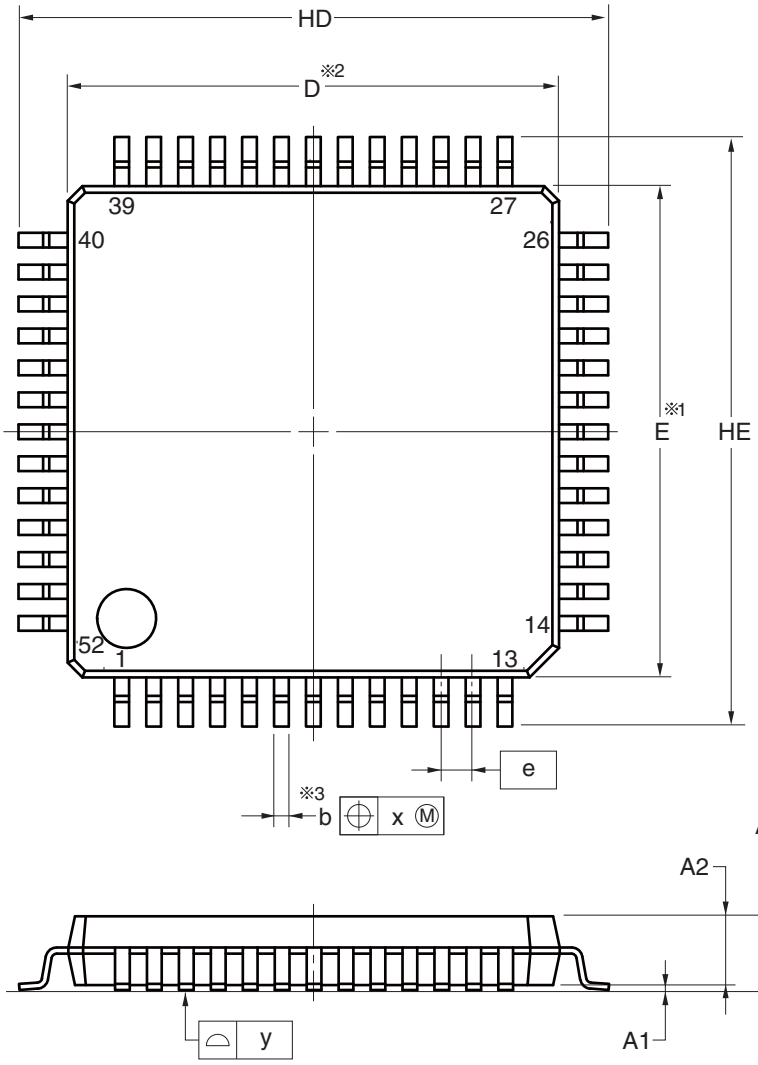
C4: A capacitor connected between $V_{L4}$ and GND

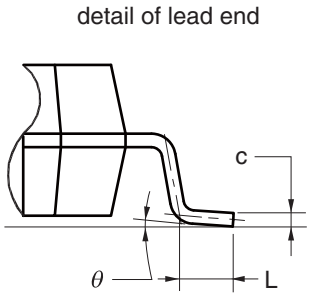
C1 = C2 = C3 = C4 = 0.47 μF±30%

## 4.4 52-pin Products

R5F10RJ8AFA, R5F10RJAAFA, R5F10RJCAFA
R5F10RJ8GFA, R5F10RJAGFA, R5F10RJCGFA

| JEITA Package Code | RENESAS Code | Previous Code | MASS (TYP.) [g] |
|---|---|---|---|
| P-LQFP52-10x10-0.65 | PLQP0052JA-A | P52GB-65-GBS-1 | 0.3 |




(UNIT:mm)

| ITEM | DIMENSIONS |
|---|---|
| D | 10.00±0.10 |
| E | 10.00±0.10 |
| HD | 12.00±0.20 |
| HE | 12.00±0.20 |
| A | 1.70 MAX. |
| A1 | 0.10±0.05 |
| A2 | 1.40 |
| b | 0.32±0.05 |
| c | 0.145±0.055 |
| L | 0.50±0.15 |
| θ | 0° to 8° |
| e | 0.65 |
| x | 0.13 |
| y | 0.10 |

**NOTE**1.Dimensions "※1" and "※2" do not include mold flash.

2.Dimension "※3" does not include trim offset.

| Rev. | Date | Description | |
|---|---|---|---|
| | | Page | Summary |
| 2.00 | Jan 10, 2014 | 35 | Modification of table in 2.4 AC Characteristics |
| | | 36 | Addition of Minimum Instruction Execution Time during Main System Clock Operation |
| | | 37 | Modification of AC Timing Test Points and External System Clock Timing |
| | | 39 | Modification of AC Timing Test Points |
| | | 39 | Modification of description, notes 1 and 2 in (1) During communication at same potential (UART mode) |
| | | 41, 42 | Modification of description, remark 2 in (2) During communication at same potential (CSI mode) |
| | | 42, 43 | Modification of description in (3) During communication at same potential (CSI mode) |
| | | 45 | Modification of description, notes 1 and 3, and remark 3 in (4) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (1/2) |
| | | 46, 48 | Modification of description, and remark 3 in (4) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (2/2) |
| | | 49, 50 | Modification of table, and note 1, caution, and remark 3 in (5) Communication at different potential (2.5 V, 3 V) (CSI mode) |
| | | 51 | Modification of table and note in (6) Communication at different potential (1.8 V, 2.5 V, 3 V) (1/3) |
| | | 52 | Modification of table and notes 1 to 3 in (6) Communication at different potential (1.8 V, 2.5 V, 3 V) (2/3) |
| | | 53, 54 | Modification of table, note 3, and remark 3 in (6) Communication at different potential (1.8 V, 2.5 V, 3 V) (3/3) |
| | | 56 | Modification of table in (7) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (1/2) |
| | | 57 | Modification of table in (7) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (2/2) |
| | | 59, 60 | Addition of (1) $I^2C$ standard mode |
| | | 61 | Addition of (2) $I^2C$ fast mode |
| | | 62 | Addition of (3) $I^2C$ fast mode plus |
| | | 63 | Addition of table in 2.6.1 A/D converter characteristics |
| | | 63, 64 | Modification of description and notes 3 to 5 in 2.6.1 (1) |
| | | 65 | Modification of description, notes 3 and 4 in 2.6.1 (2) |
| | | 66 | Modification of description, notes 3 and 4 in 2.6.1 (3) |
| | | 67 | Modification of description, notes 3 and 4 in 2.6.1 (4) |
| | | 67 | Modification of the table in 2.6.2 Temperature sensor/internal reference voltage characteristics |
| | | 68 | Modification of the table and note in 2.6.3 POR circuit characteristics |
| | | 70 | Modification of the table of LVD Detection Voltage of Interrupt & Reset Mode |
| | | 70 | Modification from $V_{DD}$ rise slope to Power supply voltage rising slope in 2.6.5 Supply voltage rise time |
| | | 75 | Modification of description in 2.10 Dedicated Flash Memory Programmer Communication (UART) |
| | | 76 | Modification of the figure in 2.11 Timing Specifications for Switching Flash Memory Programming Modes |
| | | 77 to 126 | Addition of products for industrial applications (G: $T_A$ = -40 to +105°C) |
| | | 127 to 133 | Addition of product names for industrial applications (G: $T_A$ = -40 to +105°C) |
| 2.10 | Sep 30, 2016 | 5 | Modification of pin configuration in 1.3.1 32-pin products |
| | | 6 | Modification of pin configuration in 1.3.2 44-pin products |
| | | 7 | Modification of pin configuration in 1.3.3 48-pin products |
| | | 8 | Modification of pin configuration in 1.3.4 52-pin products |
| | | 9, 10 | Modification of pin configuration in 1.3.5 64-pin products |
| | | 17 | Modification of description of main system clock in 1.6 Outline of Functions |
| | | 74 | Modification of title of 2.8 RAM Data Retention Characteristics, Note, and figure |
| | | 74 | Modification of table of 2.9 Flash Memory Programming Characteristics |
| | | 123 | Modification of title of 3.8 RAM Data Retention Characteristics, Note, and figure |
| | | 123 | Modification of table of 3.9 Flash Memory Programming Characteristics and addition of Note 4 |
| | | 131 | Modification of 4.5 64-pin Products |