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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

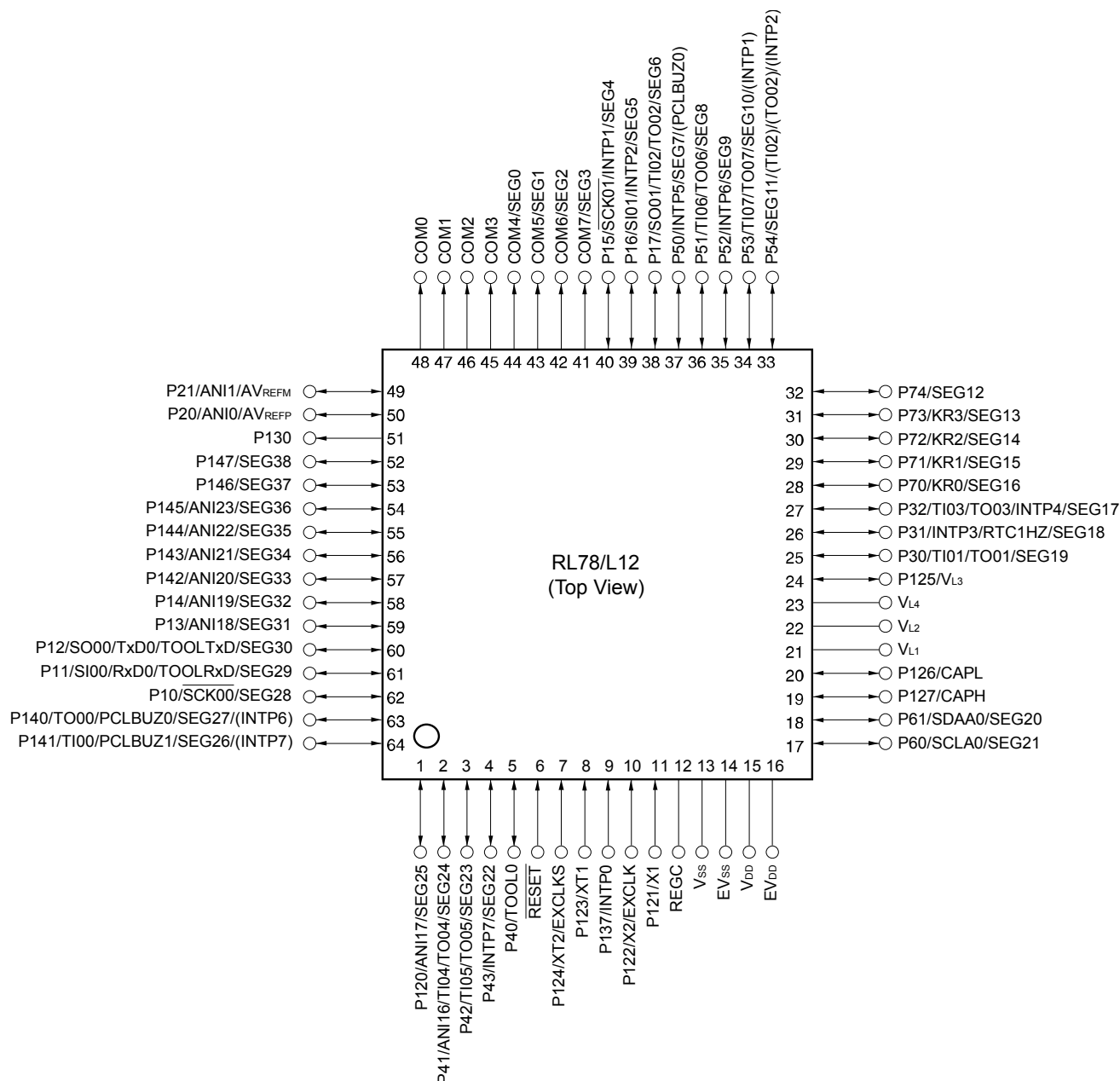
Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	RL78
Core Size	16-Bit
Speed	24MHz
Connectivity	CSI, I ² C, LINbus, UART/USART
Peripherals	DMA, LCD, LVD, POR, PWM, WDT
Number of I/O	37
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 10x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	52-LQFP
Supplier Device Package	52-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f10rjagfa-v0

- 64-pin plastic LQFP (fine pitch) (10 × 10)
- 64-pin plastic LQFP (12 × 12)

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- Cautions**
1. Make EV_{ss} pin the same potential as V_{ss} pin.
 2. Make V_{DD} pin the same potential as EV_{DD} pin.
 3. Connect the REGC pin to V_{ss} via a capacitor (0.47 to 1 μ F).

- Remarks**
1. For pin identification, see 1.4 Pin Identification.
 2. When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the V_{DD} and EV_{DD} pins and connect the V_{ss} and EV_{ss} pins to separate ground lines.
 3. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

1.6 Outline of Functions

Caution This outline describes the functions at the time when Peripheral I/O redirection register (PIOR) is set to 00H.

(1/2)

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Item		32-pin	44-pin	48-pin	52-pin	64-pin
		R5F10RBx	R5F10RFx	R5F10RGx	R5F10RJx	R5F10RLx
Code flash memory (KB)		8 to 32	8 to 32	8 to 32	8 to 32	16, 32
Data flash memory (KB)		2	2	2	2	2
RAM (KB)		1, 1.5 ^{Note 1}	1, 1.5 ^{Note 1}	1, 1.5 ^{Note 1}	1, 1.5 ^{Note 1}	1, 1.5 ^{Note 1}
Memory space		1 MB				
Main system clock	High-speed system clock	X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK) HS (high-speed main) operation: 1 to 20 MHz (V _{DD} = 2.7 to 5.5 V), HS (high-speed main) operation: 1 to 16 MHz (V _{DD} = 2.4 to 5.5 V), LS (low-speed main) operation: 1 to 8 MHz (V _{DD} = 1.8 to 5.5 V), LV (low-voltage main) operation: 1 to 4 MHz (V _{DD} = 1.6 to 5.5 V)				
	High-speed on-chip oscillator clock	HS (high-speed main) operation: 1 to 24 MHz (V _{DD} = 2.7 to 5.5 V), HS (high-speed main) operation: 1 to 16 MHz (V _{DD} = 2.4 to 5.5 V), LS (low-speed main) operation: 1 to 8 MHz (V _{DD} = 1.8 to 5.5 V), LV (low-voltage main) operation: 1 to 4 MHz (V _{DD} = 1.6 to 5.5 V)				
Subsystem clock		–	XT1 (crystal) oscillation , external subsystem clock input (EXCLKS) 32.768 kHz (TYP.): V _{DD} = 1.6 to 5.5 V			
Low-speed on-chip oscillator clock		Internal oscillation 15 kHz (TYP.): V _{DD} = 1.6 to 5.5 V				
General-purpose register		8 bits × 32 registers (8 bits × 8 registers × 4 banks)				
Minimum instruction execution time		0.04167 μs (High-speed on-chip oscillator clock: f _{IH} = 24 MHz operation)				
		0.05 μs (High-speed system clock: f _{MX} = 20 MHz operation)				
		30.5 μs (Subsystem clock: f _{SUB} = 32.768 kHz operation)				
Instruction set		<ul style="list-style-type: none">• Data transfer (8/16 bits)• Adder and subtractor/logical operation (8/16 bits)• Multiplication (8 bits × 8 bits)• Rotate, barrel shift, and bit manipulation (Set, reset, test, and Boolean operation), etc.				
Total number of I/O port pins and pins dedicated to drive an LCD		28	40	44	48	58
I/O port	Total	20	29	33	37	47
	CMOS I/O	15	22	26	30	39
	CMOS input	3	5	5	5	5
	CMOS output	–	–	–	–	1
	N-ch open-drain I/O (EV _{DD} tolerance)	2	2	2	2	2
Pins dedicated to drive an LCD		8	11	11	11	11
LCD controller/driver		Internal voltage boosting method, capacitor split method, and external resistance division method are switchable.				
Segment signal output		13	22 (18) ^{Note 2}	26 (22) ^{Note 2}	30 (26) ^{Note 2}	39 (35) ^{Note 2}
Common signal output		4	4 (8) ^{Note 2}			

Notes 1. In the case of the 1 KB, and 1.5 KB, this is 630 bytes when the self-programming function and data flash function is used.

2. The values in parentheses are the number of signal outputs when 8 com is used.

(2/2)

Item		32-pin	44-pin	48-pin	52-pin	64-pin
		R5F10RBx	R5F10RFx	R5F10RGx	R5F10RJx	R5F10RLx
Timer	16-bit timer	8 channels	8 channels (with 1 channel remote control output function)			
	Watchdog timer	1 channel				
	Real-time clock (RTC)	1 channel				
	12-bit interval timer (IT)	1 channel				
	Timer output	4 channels (PWM outputs: 3 ^{Note 1})	5 channels (PWM outputs: 4 ^{Note 1})	6 channels (PWM outputs: 5 ^{Note 1})	8 channels (PWM outputs: 7 ^{Note 1})	
	RTC output	–	1 • 1 Hz (subsystem clock: f _{SUB} = 32.768 kHz or)			
Clock output/buzzer output		1	2			
		• 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: f _{MAIN} = 20 MHz operation) • 256 Hz, 512 Hz, 1.024 kHz, 2.048 kHz, 4.096 kHz, 8.192 kHz, 16.384 kHz, 32.768 kHz (Subsystem clock: f _{SUB} = 32.768 kHz operation)				
8/10-bit resolution A/D converter		4 channels	7 channels	9 channels	10 channels	10 channels
Serial interface		• CSI: 2 channel/UART (LIN-bus supported): 1 channel				
	I ² C bus	1 channel	1 channel	1 channel	1 channel	1 channel
Multiplier and divider/multiply-accumulator		• 16 bits × 16 bits = 32 bits (Unsigned or signed) • 32 bits ÷ 32 bits = 32 bits (Unsigned) • 16 bits × 16 bits + 32 bits = 32 bits (Unsigned or signed)				
DMA controller		2 channels				
Vectored interrupt sources	Internal	23	23	23	23	23
	External	4	6	7	7	9
Key interrupt		4				
Reset		• Reset by $\overline{\text{RESET}}$ pin • Internal reset by watchdog timer • Internal reset by power-on-reset • Internal reset by voltage detector • Internal reset by illegal instruction execution ^{Note 2} • Internal reset by RAM parity error • Internal reset by illegal-memory access				
Power-on-reset circuit		• Power-on-reset: 1.51 ±0.04 V • Power-down-reset: 1.50 ±0.04 V				
Voltage detector		• Rising edge : 1.67 V to 4.06 V (14 stages) • Falling edge : 1.63 V to 3.98 V (14 stages)				
On-chip debug function		Provided				
Power supply voltage		V _{DD} = 1.6 to 5.5 V				
Operating ambient temperature		T _A = –40 to +85 °C				

Notes 1. The number of PWM outputs varies depending on the setting of channels in use (the number of masters and slaves).

2. The illegal instruction is generated when instruction code FFH is executed.

Reset by the illegal instruction execution not issued by emulation with the in-circuit emulator or on-chip debug emulator.

2.1 Absolute Maximum Ratings

Absolute Maximum Ratings (T_A = 25°C)

(1/3)

Parameter	Symbols	Conditions	Ratings	Unit
Supply voltage	V _{DD}	V _{DD} = EV _{DD}	-0.5 to +6.5	V
	EV _{DD}	V _{DD} = EV _{DD}	-0.5 to +6.5	V
	EV _{SS}		-0.5 to +0.3	V
REGC pin input voltage	V _{IREGC}	REGC	-0.3 to +2.8 and -0.3 to V _{DD} + 0.3 ^{Note 1}	V
Input voltage	V _{I1}	P10 to P17, P30 to P32, P40 to P43, P50 to P54, P70 to P74, P120, P125 to P127, P140 to P147	-0.3 to EV _{DD} + 0.3 and -0.3 to V _{DD} + 0.3 ^{Note 2}	V
	V _{I2}	P60, P61 (N-ch open-drain)	-0.3 to EV _{DD} + 0.3 and -0.3 to V _{DD} + 0.3 ^{Note 2}	V
	V _{I3}	P20, P21, P121 to P124, P137, EXCLK, EXCLKS, RESET	-0.3 to V _{DD} + 0.3 ^{Note 2}	V
Output voltage	V _{O1}	P10 to P17, P30 to P32, P40 to P43, P50 to P54, P60, P61, P70 to P74, P120, P125 to P127, P130, P140 to P147	-0.3 to EV _{DD} + 0.3 and -0.3 to V _{DD} + 0.3 ^{Note 2}	V
	V _{O2}	P20, P21	-0.3 to V _{DD} + 0.3 ^{Note 2}	V
Analog input voltage	V _{AI1}	ANI16 to ANI23	-0.3 to EV _{DD} + 0.3 and -0.3 to AV _{REF(+)} + 0.3 Notes 2, 3	V
	V _{AI2}	ANI0, ANI1	-0.3 to V _{DD} + 0.3 and -0.3 to AV _{REF(+)} + 0.3 Notes 2, 3	V

- Notes**
1. Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μF). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.
 2. Must be 6.5 V or lower.
 3. Do not exceed AV_{REF(+)} + 0.3 V in case of A/D conversion target pin.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

- Remarks**
1. Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.
 2. AV_{REF(+)} : + side reference voltage of the A/D converter.
 3. V_{SS} : Reference voltage

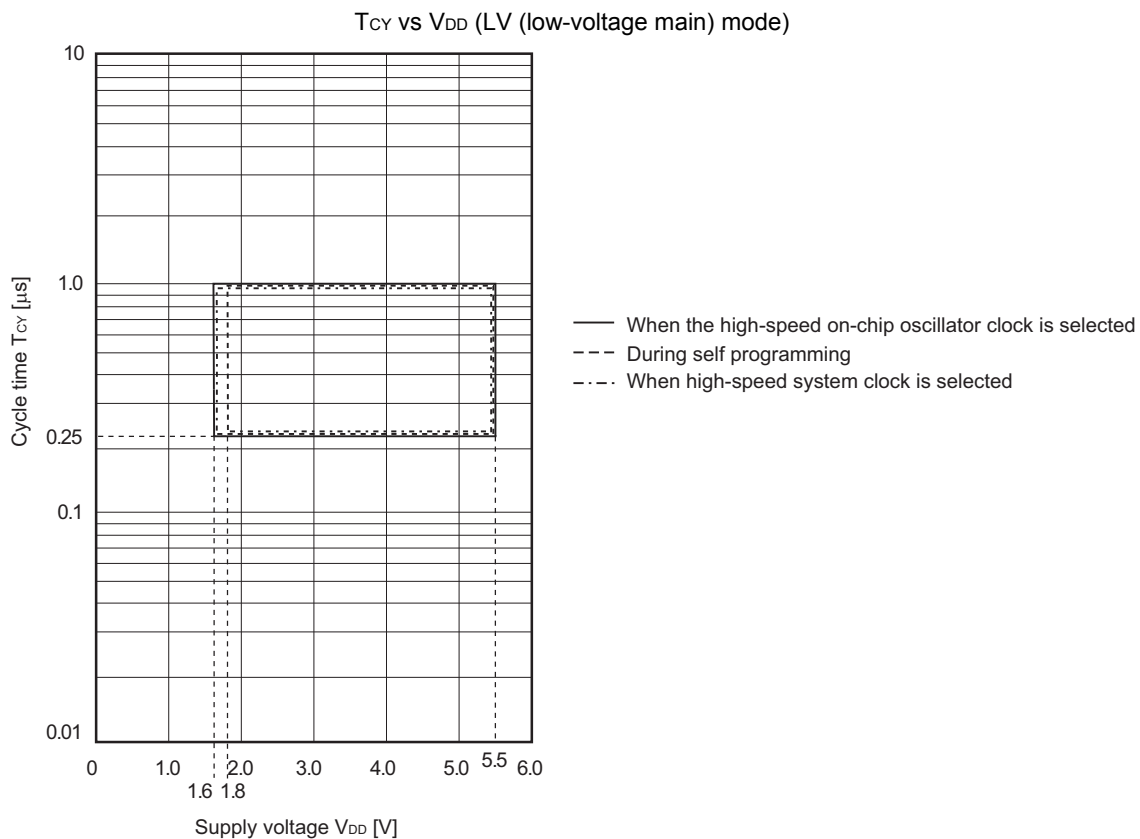
(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

(3/5)

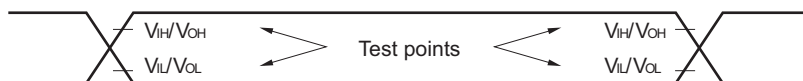
Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V _{IH1}	P10 to P17, P30 to P32, P40 to P43, P50 to P54, P70 to P74, P120, P125 to P127, P140 to P147	Normal input buffer	0.8EV _{DD}		EV _{DD}	V
	V _{IH2}	P10, P11, P15, P16	TTL input buffer 4.0 V ≤ EV _{DD} ≤ 5.5 V	2.2		EV _{DD}	V
			TTL input buffer 3.3 V ≤ EV _{DD} < 4.0 V	2.0		EV _{DD}	V
			TTL input buffer 1.6 V ≤ EV _{DD} < 3.3 V	1.50		EV _{DD}	V
	V _{IH3}	P20, P21		0.7V _{DD}		V _{DD}	V
	V _{IH4}	P60, P61		0.7EV _{DD}		EV _{DD}	V
	V _{IH5}	P121 to P124, P137, EXCLK, EXCLKS, RESET		0.8V _{DD}		V _{DD}	V
Input voltage, low	V _{IL1}	P10 to P17, P30 to P32, P40 to P43, P50 to P54, P70 to P74, P120, P125 to P127, P140 to P147	Normal input buffer	0		0.2EV _{DD}	V
	V _{IL2}	P10, P11, P15, P16	TTL input buffer 4.0 V ≤ EV _{DD} ≤ 5.5 V	0		0.8	V
			TTL input buffer 3.3 V ≤ EV _{DD} < 4.0 V	0		0.5	V
			TTL input buffer 1.6 V ≤ EV _{DD} < 3.3 V	0		0.32	V
	V _{IL3}	P20, P21		0		0.3V _{DD}	V
	V _{IL4}	P60, P61		0		0.3EV _{DD}	V
	V _{IL5}	P121 to P124, P137, EXCLK, EXCLKS, RESET		0		0.2V _{DD}	V

Caution The maximum value of V_{IH} of P10, P12, P15, P17 is EV_{DD}, even in the N-ch open-drain mode.

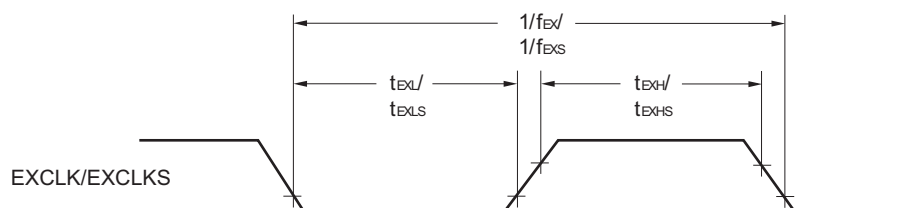
Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.



AC Timing Test Points



External System Clock Timing



(2) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output)
(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t _{KCY1}	2.7 V ≤ EV _{DD} ≤ 5.5 V	167 Note 1		500 Note 1		1000 Note 1		ns
		2.4 V ≤ EV _{DD} ≤ 5.5 V	250 Note 1		500 Note 1		1000 Note 1		ns
		1.8 V ≤ EV _{DD} ≤ 5.5 V			500 Note 1		1000 Note 1		ns
		1.6 V ≤ EV _{DD} ≤ 5.5 V					1000 Note 1		ns
SCKp high-/low-level width	t _{KH1} , t _{KL1}	4.0 V ≤ EV _{DD} ≤ 5.5 V	t _{KCY1} /2 – 12		t _{KCY1} /2 – 50		t _{KCY1} /2 – 50		ns
		2.7 V ≤ EV _{DD} ≤ 5.5 V	t _{KCY1} /2 – 18		t _{KCY1} /2 – 50		t _{KCY1} /2 – 50		ns
		2.4 V ≤ EV _{DD} ≤ 5.5 V	t _{KCY1} /2 – 38		t _{KCY1} /2 – 50		t _{KCY1} /2 – 50		ns
		1.8 V ≤ EV _{DD} ≤ 5.5 V			t _{KCY1} /2 – 50		t _{KCY1} /2 – 50		ns
		1.6 V ≤ EV _{DD} ≤ 5.5 V					t _{KCY1} /2 – 100		ns
Slp setup time (to SCKp↑) Note 2	t _{SIK1}	2.7 V ≤ EV _{DD} ≤ 5.5 V	44		110		110		ns
		2.4 V ≤ EV _{DD} ≤ 5.5 V	75		110		110		ns
		1.8 V ≤ EV _{DD} ≤ 5.5 V			110		110		ns
		1.6 V ≤ EV _{DD} ≤ 5.5 V					220		ns
Slp hold time (from SCKp↑) Note 3	t _{KSH1}	2.4 V ≤ EV _{DD} ≤ 5.5 V	19		19		19		ns
		1.8 V ≤ EV _{DD} ≤ 5.5 V			19		19		
		1.6 V ≤ EV _{DD} ≤ 5.5 V					19		
Delay time from SCKp↓ to SOp output Note 4	t _{KSO1}	C = 30 pF Note 5	2.4 V ≤ EV _{DD} ≤ 5.5 V	25		25		25	ns
			1.8 V ≤ EV _{DD} ≤ 5.5 V			25		25	
			1.6 V ≤ EV _{DD} ≤ 5.5 V					25	

Notes 1. For CSI00, set a cycle of 2/f_{MCK} or longer. For CSI01, set a cycle of 4/f_{MCK} or longer.

2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

4. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

5. C is the load capacitance of the SCKp and SOp output lines.

Caution Select the normal input buffer for the Slp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

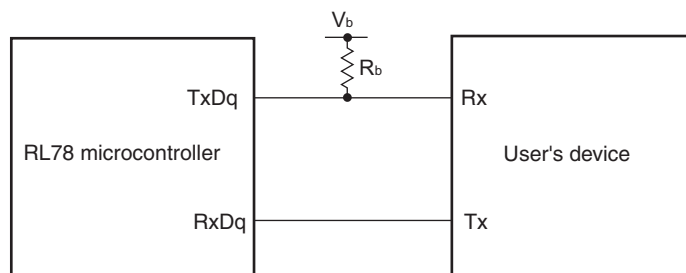
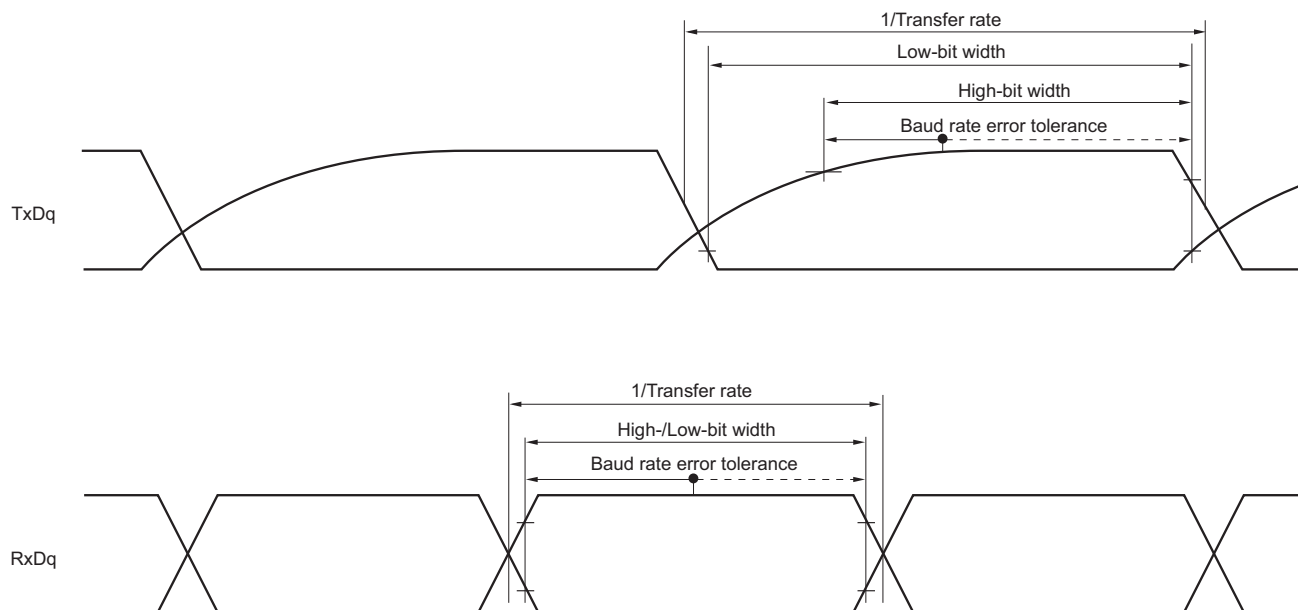
(Remarks are listed on the next page.)

- Remarks 1.** p: CSI number (p = 00, 01), m: Unit number (m = 0), n: Channel number (n = 0, 1),
g: PIM and POM numbers (g = 1)
- 2.** f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the serial clock select register m (SPSM) and the CKSMn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00, 01))

(3) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input) (1/2)
(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time ^{Note 5}	t _{KCY2}	4.0 V ≤ EV _{DD} ≤ 5.5 V	20 MHz < f _{MCK}	8/f _{MCK}						ns
			f _{MCK} ≤ 20 MHz	6/f _{MCK}		6/f _{MCK}		6/f _{MCK}		ns
		2.7 V ≤ EV _{DD} < 4.0 V	16 MHz < f _{MCK}	8/f _{MCK}						ns
			f _{MCK} ≤ 16 MHz	6/f _{MCK}		6/f _{MCK}		6/f _{MCK}		ns
		2.4 V ≤ EV _{DD} ≤ 5.5 V		6/f _{MCK} and 500		6/f _{MCK}		6/f _{MCK}		ns
		1.8 V ≤ EV _{DD} < 2.4 V				6/f _{MCK}		6/f _{MCK}		ns
		1.6 V ≤ EV _{DD} < 1.8 V						6/f _{MCK}		ns
SCKp high-/low-level width	t _{KH2} , t _{KL2}	4.0 V ≤ EV _{DD} ≤ 5.5 V		t _{KCY2} /2 – 7		t _{KCY2} /2 – 7		t _{KCY2} /2 – 7		ns
		2.7 V ≤ EV _{DD} < 4.0 V		t _{KCY2} /2 – 8		t _{KCY2} /2 – 8		t _{KCY2} /2 – 8		ns
		2.4 V ≤ EV _{DD} < 2.7 V		t _{KCY2} /2 – 18		t _{KCY2} /2 – 18		t _{KCY2} /2 – 18		ns
		1.8 V ≤ EV _{DD} < 2.4 V				t _{KCY2} /2 – 18		t _{KCY2} /2 – 18		ns
		1.6 V ≤ EV _{DD} < 1.8 V						t _{KCY2} /2 – 66		ns
Slp setup time (to SCKp↑) ^{Note 1}	t _{SIK2}	2.7 V ≤ EV _{DD} ≤ 5.5 V		1/f _{MCK} + 20		1/f _{MCK} + 30		1/f _{MCK} + 30		ns
		2.4 V ≤ EV _{DD} < 2.7 V		1/f _{MCK} + 30		1/f _{MCK} + 30		1/f _{MCK} + 30		
		1.8 V ≤ EV _{DD} < 2.4 V				1/f _{MCK} + 30		1/f _{MCK} + 30		ns
		1.6 V ≤ EV _{DD} < 1.8 V						1/f _{MCK} + 40		ns
Slp hold time (from SCKp↑) ^{Note 2}	t _{SI2}	2.4 V ≤ EV _{DD} ≤ 5.5 V		1/f _{MCK} + 31		1/f _{MCK} + 31		1/f _{MCK} + 31		ns
		1.8 V ≤ EV _{DD} < 2.4 V				1/f _{MCK} + 31		1/f _{MCK} + 31		ns
		1.6 V ≤ EV _{DD} < 1.8 V						1/f _{MCK} + 250		ns

(Notes, Caution, and Remarks are listed on the next page.)

UART mode connection diagram (during communication at different potential)**UART mode bit width (during communication at different potential) (reference)**

- Remarks**
1. $R_b[\Omega]$: Communication line (TxDq) pull-up resistance,
 $C_b[\text{F}]$: Communication line (TxDq) load capacitance, $V_b[\text{V}]$: Communication line voltage
 2. q: UART number (q = 0, 1), g: PIM and POM number (g = 1)
 3. f_{MCK} : Serial array unit operation clock frequency
 (Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 01))

(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output) (2/3)
(T_A = -40 to +85°C, 1.8 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Slp setup time (to SCKp↑) ^{Note 1}	t _{SIK1}	4.0 V ≤ EV _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 30 pF, R _b = 1.4 kΩ	81		479		479		ns
		2.7 V ≤ EV _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ	177		479		479		ns
		2.4 V ≤ EV _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V, C _b = 30 pF, R _b = 5.5 kΩ	479		479		479		ns
		1.8 V ≤ EV _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 3} , C _b = 30 pF, R _b = 5.5 kΩ			479		479		ns
Slp hold time (from SCKp↑) ^{Note 1}	t _{KSI1}	4.0 V ≤ EV _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 30 pF, R _b = 1.4 kΩ	19		19		19		ns
		2.7 V ≤ EV _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ	19		19		19		ns
		2.4 V ≤ EV _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V, C _b = 30 pF, R _b = 5.5 kΩ	19		19		19		ns
		1.8 V ≤ EV _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 3} , C _b = 30 pF, R _b = 5.5 kΩ			19		19		ns
Delay time from SCKp↓ to SOp output ^{Note 1}	t _{KSO1}	4.0 V ≤ EV _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 30 pF, R _b = 1.4 kΩ		100		100		100	ns
		2.7 V ≤ EV _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ		195		195		195	ns
		2.4 V ≤ EV _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ		483		483		483	ns
		1.8 V ≤ EV _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 3} , C _b = 30 pF, R _b = 5.5 kΩ				483		483	ns
Slp setup time (to SCKp↓) ^{Note 2}	t _{SIK1}	4.0 V ≤ EV _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 30 pF, R _b = 1.4 kΩ	44		110		110		ns
		2.7 V ≤ EV _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ	44		110		110		ns
		2.4 V ≤ EV _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ	110		110		110		ns
		1.8 V ≤ EV _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 3} , C _b = 30 pF, R _b = 5.5 kΩ			110		110		ns

- Notes**
1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.
 2. When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
 3. Use it with EV_{DD} ≥ V_b.

Caution Select the TTL input buffer for the Slp pin and the N-ch open drain output (V_{DD} tolerance (32-pin to 52-pin products)/EV_{DD} tolerance (64-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

(7) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (slave mode, SCKp... external clock input)
(T_A = -40 to +85°C, 1.8 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V) (1/2)

Parameter	Symbol	Conditions		HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time ^{Note 1}	t _{KCY2}	4.0 V ≤ EV _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V	20 MHz < f _{MCK} ≤ 24 MHz	12/f _{MCK}						ns
			8 MHz < f _{MCK} ≤ 20 MHz	10/f _{MCK}						ns
			4 MHz < f _{MCK} ≤ 8 MHz	8/f _{MCK}		16/f _{MCK}				ns
			f _{MCK} ≤ 4 MHz	6/f _{MCK}		10/f _{MCK}		10/f _{MCK}		ns
		2.7 V ≤ EV _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V	20 MHz < f _{MCK} ≤ 24 MHz	16/f _{MCK}						ns
			16 MHz < f _{MCK} ≤ 20 MHz	14/f _{MCK}						ns
			8 MHz < f _{MCK} ≤ 16 MHz	12/f _{MCK}						ns
			4 MHz < f _{MCK} ≤ 8 MHz	8/f _{MCK}		16/f _{MCK}				ns
			f _{MCK} ≤ 4 MHz	6/f _{MCK}		10/f _{MCK}		10/f _{MCK}		ns
		2.4 V ≤ EV _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V	20 MHz < f _{MCK} ≤ 24 MHz	36/f _{MCK}						ns
			16 MHz < f _{MCK} ≤ 20 MHz	32/f _{MCK}						ns
			8 MHz < f _{MCK} ≤ 16 MHz	26/f _{MCK}						ns
			4 MHz < f _{MCK} ≤ 8 MHz	16/f _{MCK}		16/f _{MCK}				ns
SCKp high-/low-level width	t _{KH2} , t _{KL2}	4.0 V ≤ EV _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V	f _{MCK} ≤ 4 MHz	10/f _{MCK}		10/f _{MCK}		10/f _{MCK}		ns
			4 MHz < f _{MCK} ≤ 8 MHz			16/f _{MCK}				ns
			8 MHz < f _{MCK} ≤ 16 MHz							ns
		1.8 V ≤ EV _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 2}	4 MHz < f _{MCK} ≤ 8 MHz			16/f _{MCK}				ns
Slp setup time (to SCKp↑) ^{Note 3}	t _{SIK2}	4.0 V ≤ EV _{DD} < 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V	4.0 V ≤ EV _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V	t _{KCY2} /2 - 12		t _{KCY2} /2 - 50		t _{KCY2} /2 - 50		ns
			2.7 V ≤ EV _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V	t _{KCY2} /2 - 18		t _{KCY2} /2 - 50		t _{KCY2} /2 - 50		ns
			2.4 V ≤ EV _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V	t _{KCY2} /2 - 50		t _{KCY2} /2 - 50		t _{KCY2} /2 - 50		ns
		1.8 V ≤ EV _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 2}	1.8 V ≤ EV _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V			t _{KCY2} /2 - 50		t _{KCY2} /2 - 50		ns
Slp hold time (from SCKp↑) ^{Note 4}	t _{SIK2}	4.0 V ≤ EV _{DD} < 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V	4.0 V ≤ EV _{DD} < 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V	1/f _{MCK} + 20		1/f _{MCK} + 30		1/f _{MCK} + 30		ns
			2.7 V ≤ EV _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V	1/f _{MCK} + 20		1/f _{MCK} + 30		1/f _{MCK} + 30		ns
			2.4 V ≤ EV _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V	1/f _{MCK} + 30		1/f _{MCK} + 30		1/f _{MCK} + 30		ns
		1.8 V ≤ EV _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 2}	1.8 V ≤ EV _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V			1/f _{MCK} + 30		1/f _{MCK} + 30		ns
Slp hold time (from SCKp↑) ^{Note 4}	t _{SIK2}	4.0 V ≤ EV _{DD} < 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V	4.0 V ≤ EV _{DD} < 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V	1/f _{MCK} + 31		1/f _{MCK} + 31		1/f _{MCK} + 31		ns
			2.7 V ≤ EV _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V	1/f _{MCK} + 31		1/f _{MCK} + 31		1/f _{MCK} + 31		ns
			2.4 V ≤ EV _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V	1/f _{MCK} + 31		1/f _{MCK} + 31		1/f _{MCK} + 31		ns
		1.8 V ≤ EV _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 2}	1.8 V ≤ EV _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V			1/f _{MCK} + 31		1/f _{MCK} + 31		ns

(Notes, Caution and Remarks are listed on the next page.)

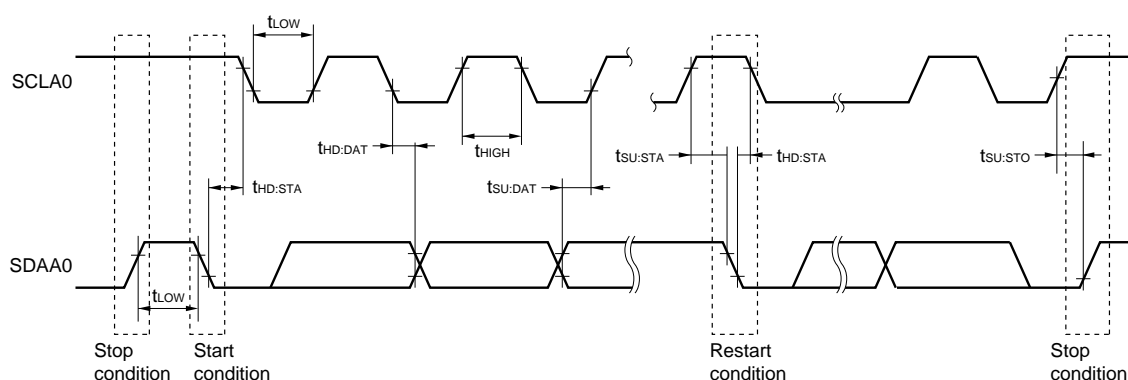
(3) I²C fast mode plus(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f _{SCL}	Fast mode plus: f _{CLK} ≥ 10 MHz 2.7 V ≤ EV _{DD} ≤ 5.5 V	0	1000	—	—	—	—	kHz
Setup time of restart condition	t _{SU:STA}	2.7 V ≤ EV _{DD} ≤ 5.5 V	0.26		—	—	—	—	μs
Hold time ^{Note 1}	t _{HD:STA}	2.7 V ≤ EV _{DD} ≤ 5.5 V	0.26		—	—	—	—	μs
Hold time when SCLA0 = "L"	t _{LOW}	2.7 V ≤ EV _{DD} ≤ 5.5 V	0.5		—	—	—	—	μs
Hold time when SCLA0 = "H"	t _{HIGH}	2.7 V ≤ EV _{DD} ≤ 5.5 V	0.26		—	—	—	—	μs
Data setup time (reception)	t _{SU:DAT}	2.7 V ≤ EV _{DD} ≤ 5.5 V	50		—	—	—	—	μs
Data hold time (transmission) ^{Note 2}	t _{HD:DAT}	2.7 V ≤ EV _{DD} ≤ 5.5 V	0	0.45	—	—	—	—	μs
Setup time of stop condition	t _{SU:STO}	2.7 V ≤ EV _{DD} ≤ 5.5 V	0.26		—	—	—	—	μs
Bus-free time	t _{BUF}	2.7 V ≤ EV _{DD} ≤ 5.5 V	0.5		—	—	—	—	μs

Notes 1. The first clock pulse is generated after this period when the start/restart condition is detected.2. The maximum value (MAX.) of t_{HD:DAT} is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

Caution The values in the above table are applied even when bit 2 (PIOR2) in the peripheral I/O redirection register (PIOR) is 1. At this time, the pin characteristics (I_{OH1}, I_{OL1}, V_{OH1}, V_{OL1}) must satisfy the values in the redirect destination.

Remark The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.

Fast mode plus: C_b = 120 pF, R_b = 1.1 kΩ**IICA serial transfer timing**

3.3 DC Characteristics

3.3.1 Pin characteristics

(T_A = -40 to +105°C, 2.4 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

(1/5)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, high ^{Note 1}	I _{OH1}	Per pin for P10 to P17, P30 to P32, P40 to P43, P50 to P54, P70 to P74, P120, P125 to P127, P130, P140 to P147				-3.0 ^{Note 2}	mA
		Total of P10 to P14, P40 to P43, P120, P130, P140 to P147 (When duty = 70% ^{Note 3})	4.0 V ≤ EV _{DD} ≤ 5.5 V			-30.0	mA
			2.7 V ≤ EV _{DD} < 4.0 V			-8.0	mA
			2.4 V ≤ EV _{DD} < 2.7 V			-4.0	mA
		Total of P15 to P17, P30 to P32, P50 to P54, P70 to P74, P125 to P127 (When duty = 70% ^{Note 3})	4.0 V ≤ EV _{DD} ≤ 5.5 V			-30.0	mA
			2.7 V ≤ EV _{DD} < 4.0 V			-15.0	mA
			2.4 V ≤ EV _{DD} < 2.7 V			-8.0	mA
		Total of all pins (When duty = 70% ^{Note 3})				-60.0	mA
	I _{OH2}	P20, P21	Per pin			-0.1	mA
			Total of all pins	2.4 V ≤ V _{DD} ≤ 5.5 V		-0.2	mA

Notes 1. Value of current at which the device operation is guaranteed even if the current flows from the V_{DD} and EV_{DD} pins to an output pin.

2. Do not exceed the total current value.

3. Specification under conditions where the duty factor ≤ 70%.

The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (I_{OH} × 0.7)/(n × 0.01)

<Example> Where n = 80% and I_{OH} = -30.0 mA

$$\text{Total output current of pins} = (-30.0 \times 0.7) / (80 \times 0.01) \approx -26.25 \text{ mA}$$

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

Caution P10, P12, P15, and P17 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

- Notes**
1. Total current flowing into V_{DD} and EV_{DD}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, EV_{DD} or V_{SS}, EV_{SS}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
 2. When high-speed on-chip oscillator and subsystem clock are stopped.
 3. When high-speed system clock and subsystem clock are stopped.
 4. When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). However, not including the current flowing into the RTC, 12-bit interval timer, watchdog timer, and LCD controller/driver.
 5. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
HS (high-speed main) mode: $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }24\text{ MHz}$
 $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }16\text{ MHz}$

- Remarks**
1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
 2. f_{IH}: High-speed on-chip oscillator clock frequency
 3. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)
 4. Except subsystem clock operation, temperature condition of the TYP. value is T_A = 25°C

3.4 AC Characteristics

3.4.1 Basic operation

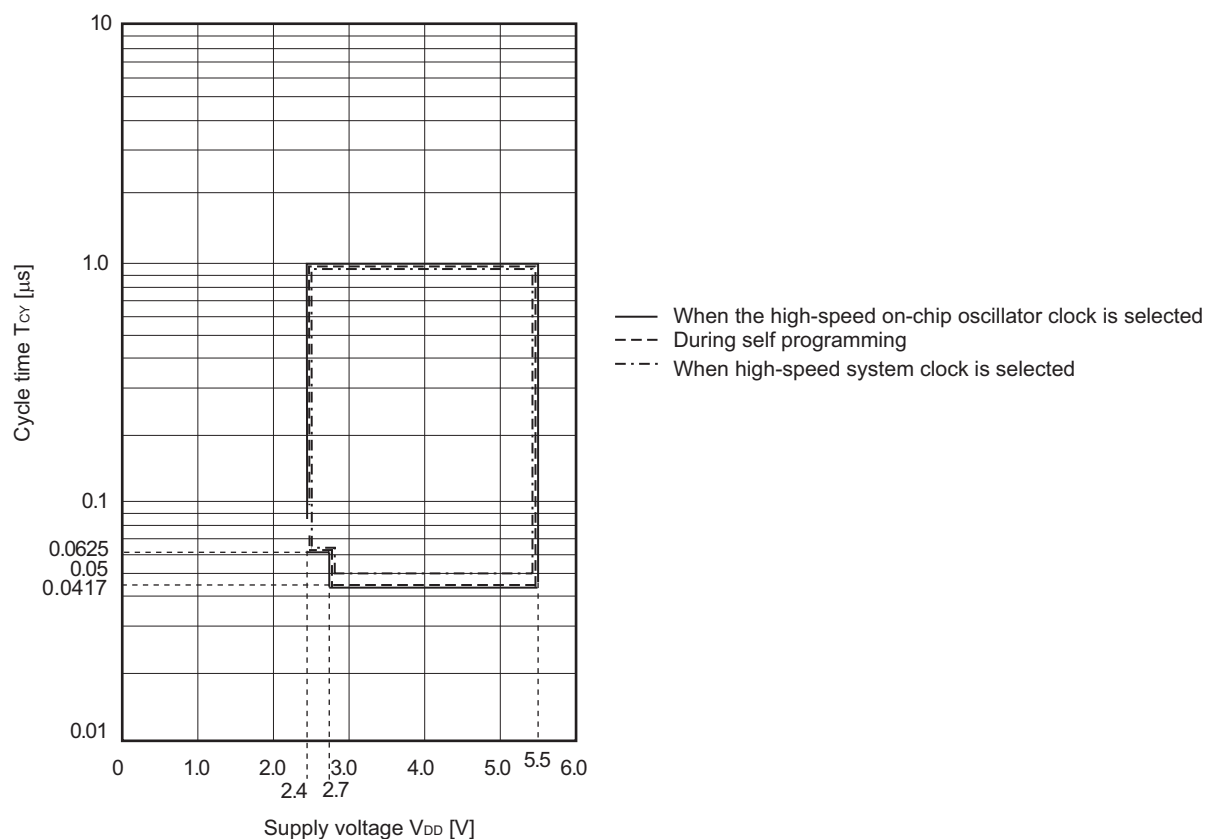
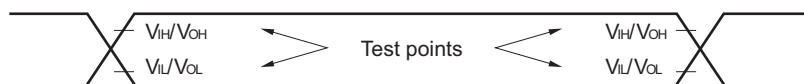
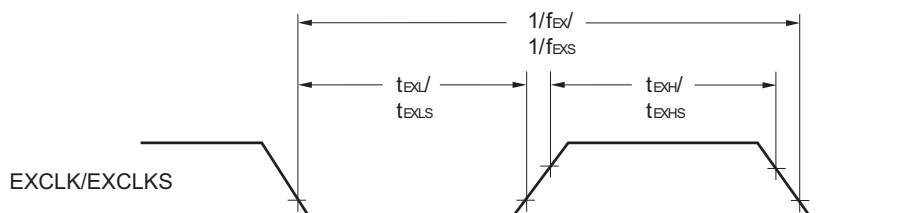
(T_A = -40 to +105°C, 2.4 V ≤ E_{VDD} = V_{DD} ≤ 5.5 V, V_{SS} = E_{VSS} = 0 V)

Items	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Instruction cycle (minimum instruction execution time)	T _{CY}	Main system clock (f _{MAIN}) operation	HS (high-speed main) mode	2.7 V ≤ V _{DD} ≤ 5.5 V	0.04167		1	μs
				2.4 V ≤ V _{DD} < 2.7 V	0.0625		1	μs
		Subsystem clock (f _{SUB}) operation		2.4 V ≤ V _{DD} ≤ 5.5 V	28.5	30.5	31.3	μs
		In the self programming mode	HS (high-speed main) mode	2.7 V ≤ V _{DD} ≤ 5.5 V	0.04167		1	μs
				2.4 V ≤ V _{DD} < 2.7 V	0.0625		1	μs
External system clock frequency	f _{EX}	2.7 V ≤ V _{DD} ≤ 5.5 V			1.0		20.0	MHz
		2.4 V ≤ V _{DD} < 2.7 V			1.0		16.0	MHz
	f _{EXS}				32		35	kHz
External system clock input high-level width, low-level width	t _{EXH} , t _{EXL}	2.7 V ≤ V _{DD} ≤ 5.5 V			24			ns
		2.4 V ≤ V _{DD} < 2.7 V			30			ns
	t _{EXHS} , t _{EXLS}				13.7			μs
TI00 to TI07 input high-level width, low-level width	t _{TIH} , t _{TIL}				1/f _{MCK} +10			ns
TO00 to TO07 output frequency	f _{TO}	HS (high-speed main) mode	4.0 V ≤ EV _{DD} ≤ 5.5 V				16	MHz
			2.7 V ≤ EV _{DD} < 4.0 V				8	MHz
			2.4 V ≤ EV _{DD} < 2.7 V				4	MHz
PCLBUZ0, PCLBUZ1 output frequency	f _{PCL}	HS (high-speed main) mode	4.0 V ≤ EV _{DD} ≤ 5.5 V				16	MHz
			2.7 V ≤ EV _{DD} < 4.0 V				8	MHz
			2.4 V ≤ EV _{DD} < 2.7 V				4	MHz
Interrupt input high-level width, low-level width	t _{INTH} , t _{INTL}	INTP0	2.4 V ≤ V _{DD} ≤ 5.5 V		1			μs
		INTP1 to INTP7	2.4 V ≤ EV _{DD} ≤ 5.5 V		1			μs
Key interrupt input low-level width	t _{KR}	KR0 to KR3	2.4 V ≤ EV _{DD} ≤ 5.5 V		250			ns
RESET low-level width	t _{RSL}				10			μs

Remark f_{MCK}: Timer array unit operation clock frequency

(Operation clock to be set by the CKS0n bit of timer mode register 0n (TMR0n).

n: Channel number (n = 0 to 7))

Minimum Instruction Execution Time during Main System Clock Operation T_{CY} vs V_{DD} (HS (high-speed main) mode)**AC Timing Test Points****External System Clock Timing**

(2) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output)**(T_A = -40 to +105°C, 2.4 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)**

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
SCKp cycle time	t _{KCY1}	2.7 V ≤ EV _{DD} ≤ 5.5 V	334 ^{Note 1}		ns
		2.4 V ≤ EV _{DD} ≤ 5.5 V	500 ^{Note 1}		ns
SCKp high-/low-level width	t _{KH1} , t _{KL1}	4.0 V ≤ EV _{DD} ≤ 5.5 V	t _{KCY1} /2 – 24		ns
		2.7 V ≤ EV _{DD} ≤ 5.5 V	t _{KCY1} /2 – 36		ns
		2.4 V ≤ EV _{DD} ≤ 5.5 V	t _{KCY1} /2 – 76		ns
Slp setup time (to SCKp↑) ^{Note 2}	t _{SIK1}	2.7 V ≤ EV _{DD} ≤ 5.5 V	66		ns
		2.4 V ≤ EV _{DD} ≤ 5.5 V	113		ns
Slp hold time (from SCKp↑) ^{Note 3}	t _{KSI1}	2.4 V ≤ EV _{DD} ≤ 5.5 V	38		ns
Delay time from SCKp↓ to SOp output ^{Note 4}	t _{KSO1}	C = 30 pF ^{Note 5}	2.4 V ≤ EV _{DD} ≤ 5.5 V	50	ns

Notes 1. Set a cycle of 4/f_{MCK} or longer.

2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

4. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

5. C is the load capacitance of the SCKp and SOp output lines.

Caution Select the normal input buffer for the Slp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).**Remarks** 1. p: CSI number (p = 00, 01), m: Unit number (m = 0), n: Channel number (n = 0, 1),
g: PIM and POM numbers (g = 1)2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 01))

(4) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (1/2)**(T_A = -40 to +105°C, 2.4 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = 0 V)**

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
Transfer rate		Reception		f _{MCK} /12 ^{Note 1}	bps
				2.0	Mbps
			4.0 V ≤ EV _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V		
			Theoretical value of the maximum transfer rate f _{MCK} = f _{CLK} ^{Note 2}		
				f _{MCK} /12 ^{Note 1}	bps
				2.0	Mbps
			2.7 V ≤ EV _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V		
			Theoretical value of the maximum transfer rate f _{MCK} = f _{CLK} ^{Note 2}		
				f _{MCK} /12 ^{Note 1}	bps
				2.0	Mbps
			2.4 V ≤ EV _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V		
			Theoretical value of the maximum transfer rate f _{MCK} = f _{CLK} ^{Note 2}		

Notes 1. Transfer rate in the SNOOZE mode is 4800 bps only.**2.** The maximum operating frequencies of the CPU/peripheral hardware clock (f_{CLK}) are:HS (high-speed main) mode: 24 MHz (2.7 V ≤ V_{DD} ≤ 5.5 V)16 MHz (2.4 V ≤ V_{DD} ≤ 5.5 V)

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance (32- to 52-pin products)/EV_{DD} tolerance (64-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

Remarks 1. V_b[V]: Communication line voltage**2.** q: UART number (q = 0), g: PIM and POM number (g = 1)**3.** f_{MCK}: Serial array unit operation clock frequency

(Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 01))

(4) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode)

(2/2)

(T_A = -40 to +105°C, 2.4 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
Transfer rate		Transmission	4.0 V ≤ EV _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V	Note 1	bps
			Theoretical value of the maximum transfer rate C _b = 50 pF, R _b = 1.4 kΩ, V _b = 2.7 V	2.0 ^{Note 2}	Mbps
			2.7 V ≤ EV _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V	Note 3	bps
			Theoretical value of the maximum transfer rate C _b = 50 pF, R _b = 2.7 kΩ, V _b = 2.3 V	1.2 ^{Note 4}	Mbps
			2.4 V ≤ EV _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V	Note 5	bps
			Theoretical value of the maximum transfer rate C _b = 50 pF, R _b = 5.5 kΩ, V _b = 1.6 V	0.43 ^{Note 6}	Mbps

Notes 1. The smaller maximum transfer rate derived by using f_{MCK}/6 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 4.0 V ≤ EV_{DD} ≤ 5.5 V and 2.7 V ≤ V_b ≤ 4.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

2. This value as an example is calculated when the conditions described in the "Conditions" column are met. Refer to Note 1 above to calculate the maximum transfer rate under conditions of the customer.

3. The smaller maximum transfer rate derived by using f_{MCK}/6 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 2.7 V ≤ EV_{DD} < 4.0 V and 2.3 V ≤ V_b ≤ 2.7 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

4. This value as an example is calculated when the conditions described in the "Conditions" column are met. Refer to Note 3 above to calculate the maximum transfer rate under conditions of the customer.

3.6.4 LVD circuit characteristics

(T_A = -40 to +105°C, V_{PDR} ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	Supply voltage level	VLVD0	Power supply rise time	3.90	4.06	4.22	V
			Power supply fall time	3.83	3.98	4.13	V
		VLVD1	Power supply rise time	3.60	3.75	3.90	V
			Power supply fall time	3.53	3.67	3.81	V
		VLVD2	Power supply rise time	3.01	3.13	3.25	V
			Power supply fall time	2.94	3.06	3.18	V
		VLVD3	Power supply rise time	2.90	3.02	3.14	V
			Power supply fall time	2.85	2.96	3.07	V
		VLVD4	Power supply rise time	2.81	2.92	3.03	V
			Power supply fall time	2.75	2.86	2.97	V
		VLVD5	Power supply rise time	2.70	2.81	2.92	V
			Power supply fall time	2.64	2.75	2.86	V
		VLVD6	Power supply rise time	2.61	2.71	2.81	V
			Power supply fall time	2.55	2.65	2.75	V
		VLVD7	Power supply rise time	2.51	2.61	2.71	V
			Power supply fall time	2.45	2.55	2.65	V
Minimum pulse width		tLW		300			μs
Detection delay time						300	μs

LVD Detection Voltage of Interrupt & Reset Mode

(T_A = -40 to +105°C, V_{PDR} ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Interrupt and reset mode	V _{LVDD0}	V _{POC2} , V _{POC1} , V _{POC0} = 0, 1, 1, falling reset voltage		2.64	2.75	2.86	V
	V _{LVDD1}	LVIS1, LVIS0 = 1, 0	Rising release reset voltage	2.81	2.92	3.03	V
			Falling interrupt voltage	2.75	2.86	2.97	V
	V _{LVDD2}	LVIS1, LVIS0 = 0, 1	Rising release reset voltage	2.90	3.02	3.14	V
			Falling interrupt voltage	2.85	2.96	3.07	V
	V _{LVDD3}	LVIS1, LVIS0 = 0, 0	Rising release reset voltage	3.90	4.06	4.22	V
			Falling interrupt voltage	3.83	3.98	4.13	V

3.6.5 Power supply voltage rising slope characteristics

(T_A = -40 to +105°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power supply voltage rising slope	S _{VDD}				54	V/ms

Caution Make sure to keep the internal reset state by the LVD circuit or an external reset until V_{DD} reaches the operating voltage range shown in 31.4 AC Characteristics.