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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	RL78
Core Size	16-Bit
Speed	24MHz
Connectivity	CSI, I ² C, LINbus, UART/USART
Peripherals	DMA, LCD, LVD, POR, PWM, WDT
Number of I/O	37
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	1.5K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 10x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	52-LQFP
Supplier Device Package	52-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f10rjcgfa-50

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Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

1.2 List of Part Numbers



Figure 1-1 Part Number, Memory Size, and Package of RL78/L12



TI/TO Timing





UART mode connection diagram (during communication at same potential)



UART mode bit width (during communication at same potential) (reference)



Remarks 1. q: UART number (q = 0), g: PIM and POM number (g = 1)

 fMCK: Serial array unit operation clock frequency (Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 01))



- **Remarks 1.** p: CSI number (p = 00, 01), m: Unit number (m = 0), n: Channel number (n = 0, 1), g: PIM and POM numbers (g = 1)
 - fMCK: Serial array unit operation clock frequency (Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn).

m: Unit number, n: Channel number (mn = 00, 01))

(3) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input) (1/2) ($T_A = -40$ to +85°C, 1.6 V $\leq EV_{DD} = V_{DD} \leq 5.5$ V, Vss = EVss = 0 V)

Parameter	Symbol	Cond	itions	HS (high main)	n-speed Mode	LS (low- main)	-speed Mode	LV (low main)	-voltage Mode	Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time ^{Note}	t ксү2	$4.0~V \leq EV_{DD} \leq 5.5~V$	20 MHz < fмск	8/fмск						ns
5			fмск ≤ 20 MHz	6/fмск		6/fмск		6/ f мск		ns
		$2.7~V \leq EV_{DD} < 4.0~V$	16 MHz < fмск	8/f мск						ns
			$f_{MCK} \le 16 \; MHz$	6/fмск		6/fмск		6/fмск		ns
		$2.4~V \leq EV_{\text{DD}} \leq 5.5~V$		6/fмск		6/ f мск		6/fмск		ns
				and 500						
		$1.8 \text{ V} \leq \text{EV}_{\text{DD}} < 2.4 \text{ V}$				6/ f мск		6/fмск		ns
		$1.6~V \leq EV_{\text{DD}} < 1.8~V$						6/fмск		ns
SCKp high-/low-	tкн2,	$4.0~V \leq EV_{\text{DD}} \leq 5.5~V$		tксү2/2		tксү2/2		tксү2/2		ns
level width	IKL2			- /		- /		- /		20
		$2.7 V \leq EVDD \leq 4.0 V$		- 8		- 8		- 8		ns
		$2.4 \text{ V} \le \text{EV}_{\text{DD}} \le 2.7 \text{ V}$		tксү2/2 – 18		t _{ксү2} /2 – 18		t _{ксү2} /2 – 18		ns
		$1.8 \text{ V} \le \text{EV}_{\text{DD}} \le 2.4 \text{ V}$				tксү2/2 – 18		tксү2/2 – 18		ns
		$1.6 \text{ V} \le \text{EV}_{\text{DD}} < 1.8 \text{ V}$						tксү2/2 – 66		ns
SIp setup time (to SCKp↑) ^{Note 1}	tsik2	$2.7~V \leq EV_{\text{DD}} \leq 5.5~V$		1/fмск + 20		1/fмск + 30		1/fмск + 30		ns
		$2.4 \text{ V} \le \text{EV}_{\text{DD}} < 2.7 \text{ V}$		1/fмск + 30		1/fмск + 30		1/fмск + 30		
		$1.8 \text{ V} \le \text{EV}_{\text{DD}} < 2.4 \text{ V}$				1/fмск + 30		1/fмск + 30		ns
		$1.6 \text{ V} \le \text{EV}_{\text{DD}} < 1.8 \text{ V}$						1/fмск + 40		ns
SIp hold time (from SCKp↑) ^{Note 2}	tksi2	$2.4~V \le EV_{\text{DD}} \le 5.5~V$		1/fмск + 31		1/fмск + 31		1/fмск + 31		ns
		$1.8 \text{ V} \le \text{EV}_{\text{DD}} < 2.4 \text{ V}$				1/fмск + 31		1/fмск + 31		ns
		$1.6 \text{ V} \le \text{EV}_{\text{DD}} < 1.8 \text{ V}$						1/fмск + 250		ns

(Notes, Caution, and Remarks are listed on the next page.)

(3) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input) (2/2) ($T_A = -40$ to $+85^{\circ}C$, 1.6 V $\leq EV_{DD} = V_{DD} \leq 5.5$ V, Vss = EVss = 0 V)

Parameter	Symbol	Conditions		HS (high- speed main) Mode	LS (low- speed main) Mode	LV (low- voltage main) Mode	Unit	Para meter	Symbol	Conditions
Delay time from SCKp↓ to SOp	tkso2	C = 30 pF ^{Note 4}	$4.0~V \leq EV_{DD} \leq 5.5~V$		2/fмск + 44		2/f _{мск} + 110		2/fмск + 110	ns
output ^{Note 3}			$2.7 \text{ V} \leq \text{EV}_{\text{DD}} < 4.0 \text{ V}$		2/fмск + 44		2/fмск + 110		2/fмск + 110	ns
			$2.4 \text{ V} \le \text{EV}_{\text{DD}} < 2.7 \text{ V}$		2/fмск + 75		2/fмск + 110		2/fмск + 110	ns
			$1.8 \text{ V} \le \text{EV}_{\text{DD}} < 2.4 \text{ V}$				2/fмск + 110		2/fмск + 110	ns
			$1.6 \text{ V} \le \text{EV}_{\text{DD}} < 1.8 \text{ V}$						2/fмск + 220	ns

- **Notes 1.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
 - **2.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
 - **3.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
 - 4. C is the load capacitance of the SCKp and SOp output lines.
 - 5. Transfer rate in the SNOOZE mode: MAX. 1 Mbps

Caution Select the normal input buffer for the SIp pin and SCKp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

- **Remarks 1.** p: CSI number (p = 00, 01), m: Unit number (m = 0), n: Channel number (n = 0, 1), g: PIM number (g = 1)
 - fMCK: Serial array unit operation clock frequency (Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 01))





CSI mode connection diagram (during communication at same potential)





CSI mode serial transfer timing (during communication at same potential) (When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)





2. m: Unit number, n: Channel number (mn = 00, 01)



CSI mode connection diagram (during communication at different potential)



- **Remarks 1.** R_b[Ω]:Communication line (SCKp, SOp) pull-up resistance, C_b[F]: Communication line (SCKp, SOp) load capacitance, V_b[V]: Communication line voltage
 - 2. p: CSI number (p = 00, 01), m: Unit number (m = 0), n: Channel number (n = 0, 1), g: PIM and POM number (g = 1)
 - 3. fMCK: Serial array unit operation clock frequency

(Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 01)



(T _A = -40 to +85°0	C, 1.8 V ≤	$EV_{DD} = V_{DD} \le 5.5 V, V_{SS} = EV_{SS} = 0$	V)						(2/2)
Parameter	Symbol	Conditions		HS (high- speed main) mode		/-speed mode	LV (voltage mc	low- e main) ode	Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Delay time from SCKp↓ to SOp output ^{Note 5}	tkso2	$\begin{array}{l} 4.0 \; V \leq EV_{\text{DD}} \leq 5.5 \; V, 2.7 \; V \leq V_b \leq 4.0 \; V, \\ C_b = 30 \; pF, \; R_b = 1.4 \; k\Omega \end{array}$		2/fмск + 120		2/fмск + 573		2/fмск + 573	ns
		$\label{eq:VD} \begin{array}{l} 2.7 \ V \leq EV_{\text{DD}} < 4.0 \ V, \ 2.3 \ V \leq V_b \leq 2.7 \ V, \\ C_b = 30 \ pF, \ R_b = 2.7 \ k\Omega \end{array}$		2/fмск + 214		2/fмск + 573		2/fмск + 573	ns
		$\label{eq:V_def} \begin{array}{l} 2.4 \ V \leq EV_{\text{DD}} < 3.3 \ V, \ 1.6 \ V \leq V_b \leq 2.0 \ V, \\ C_b = 30 \ pF, \ R_b = 5.5 \ k\Omega \end{array}$		2/fмск + 573		2/fмск + 573		2/fмск + 573	ns
		$ \begin{split} & 1.8 \ V \leq EV_{DD} < 3.3 \ V, \\ & 1.6 \ V \leq V_b \leq 2.0 \ V^{\text{Note 2}}, \\ & C_b = 30 \ pF, \ R_b = 5.5 \ k\Omega \end{split} $				2/f _{мск} + 573		2/fмск + 573	ns

(7) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (slave mode, SCKp... external clock input)

Notes 1. Transfer rate in the SNOOZE mode : MAX. 1 Mbps

- **2.** Use it with $EV_{DD} \ge V_b$.
- **3.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp \downarrow " when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
- **4.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp \downarrow " when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
- 5. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp[↑]" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
- Caution Select the TTL input buffer for the SIp pin and SCKp pin and the N-ch open drain output (VDD tolerance (32-pin to 52-pin products)/EVDD tolerance (64-pin products)) mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For VIH and VIL, see the DC characteristics with TTL input buffer selected.

CSI mode connection diagram (during communication at different potential)



- **Remarks 1.** R_b[Ω]:Communication line (SOp) pull-up resistance, C_b[F]: Communication line (SOp) load capacitance, V_b[V]: Communication line voltage
 - p: CSI number (p = 00, 01), m: Unit number (m = 0), n: Channel number (n = 0, 1), g: PIM and POM number (g = 1)
 - **3.** fMCK: Serial array unit operation clock frequency

(Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 01))

2.6 Analog Characteristics

2.6.1 A/D converter characteristics

Classification of A/D converter characteristics

		Reference Voltage	
	Reference voltage (+) = AVREFP	Reference voltage (+) = VDD	Reference voltage (+) = VBGR
Input channel	Reference voltage (-) = AVREFM	Reference voltage (-) = Vss	Reference voltage (-) = AVREFM
ANIO, ANI1	-	Refer to 2.6.1 (3).	Refer to 2.6.1 (4).
ANI16 to ANI23	Refer to 2.6.1 (2).		
Internal reference voltage Temperature sensor output voltage	Refer to 2.6.1 (1) .		-

(1) When reference voltage (+) = AV_{REFP}/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (-) = AV_{REFM}/ANI1 (ADREFM = 1), target pin : internal reference voltage, and temperature sensor output voltage

 $(T_A = -40 \text{ to } +85^{\circ}\text{C}, 2.4 \text{ V} \le \text{EV}_{\text{DD}} = \text{V}_{\text{DD}} \le 5.5 \text{ V}, 1.6 \text{ V} \le \text{AV}_{\text{REFP}} \le \text{V}_{\text{DD}} \le 5.5 \text{ V}, \text{V}_{\text{SS}} = \text{EV}_{\text{SS}} = 0 \text{ V}, \text{Reference voltage (+)} = \text{AV}_{\text{REFP}}, \text{Reference voltage (-)} = \text{AV}_{\text{REFM}} = 0 \text{ V})$

Parameter	Symbol	Condit	ions	MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error ^{Note 1}	AINL	10-bit resolution	$1.8~V \leq V_{\text{DD}} \leq 5.5~V$		1.2	±3.5	LSB
		AV _{REFP} = V _{DD} ^{Note 3}	$1.6~\text{V} \leq \text{V}_\text{DD} \leq 5.5~\text{V}^{\text{Note 4}}$		1.2	±7.0	LSB
Conversion time	t CONV	10-bit resolution	$3.6~V \leq V_{\text{DD}} \leq 5.5~V$	2.375		39	μs
		Target pin: Internal reference	$2.7~V \leq V_{\text{DD}} \leq 5.5~V$	3.5625		39	μs
		voltage, and temperature sensor output voltage (HS	$2.4~V \leq V_{\text{DD}} \leq 5.5~V$	17		39	μs
		(high-speed main) mode)					
Zero-scale error ^{Notes 1, 2}	E _{zs}	10-bit resolution	$1.8 \text{ V} \le \text{AV}_{\text{REFP}} \le 5.5 \text{ V}$			±0.25	%FSR
		AV _{REFP} = V _{DD} ^{NOLE 3}	$1.6~V \leq AV_{\text{REFP}} \leq 5.5~V^{\text{Note 4}}$			±0.50	%FSR
Full-scale error Notes 1, 2	E _{FS}	10-bit resolution	$1.8~V \leq AV_{\text{REFP}} \leq 5.5~V$			±0.25	%FSR
		$AV_{REFP} = V_{DD}^{Note 3}$	$1.6~V \leq AV_{\text{REFP}} \leq 5.5~V^{\text{Note 4}}$			±0.50	%FSR
Integral linearity	ILE	10-bit resolution	$1.8~V \leq V_{\text{DD}} \leq 5.5~V$			±2.5	LSB
error ^{Note 1}		AV _{REFP} = V _{DD} ^{Note 3}	$1.6~V \leq V_{\text{DD}} \leq 5.5~V^{\text{Note 4}}$			±5.0	LSB
Differential linearity	DLE	10-bit resolution	$1.8~V \leq V_{\text{DD}} \leq 5.5~V$			±1.5	LSB
error ^{Note 1}		AV _{REFP} = V _{DD} ^{Note 3}	$1.6~V \leq V_{\text{DD}} \leq 5.5~V^{\text{Note 4}}$			±2.0	LSB
Analog input voltage	VAIN	Internal reference voltage			$V_{\text{BGR}}^{\text{Note 5}}$		V
		(2.4 V \leq V_{DD} \leq 5.5 V, HS (high-					
	VBGR	Temperature sensor output vol (2.4 V \leq V _{DD} \leq 5.5 V, HS (high-	V _{TMPS25} Note 5			V	

Notes 1. Excludes quantization error ($\pm 1/2$ LSB).

- 2. This value is indicated as a ratio (%FSR) to the full-scale value.
- **3.** When AV_{REFP} < V_{DD}, the MAX. values are as follows.
 - Overall error: Add ± 1.0 LSB to the MAX. value when AV_{REFP} = V_{DD}.

Zero-scale error/Full-scale error: Add $\pm 0.05\%$ FSR to the MAX. value when AV_{REFP} = V_{DD}.

Integral linearity error/Differential linearity error: Add ±0.5 LSB to the MAX. value when AVREFP = VDD.

- 4. Values when the conversion time is set to 57 μ s (min.) and 95 μ s (max.).
- 5. Refer to 2.6.2 Temperature sensor/internal reference voltage characteristics.

(2) When reference voltage (+) = AV_{REFP}/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (-) = AV_{REFM}/ANI1 (ADREFM = 1), target pin : ANI16 to ANI23

$T_A = -40$ to +85°C, 1.6 V \leq EV _{DD} = V _{DD} \leq 5.5 V, 1.6 V \leq AV _{REFP} \leq V _{DD} \leq 5.5 V, V _{SS} = EV _{SS} = 0 V, Reference voltage (+) = 0.05	=
AVREFP, Reference voltage (–) = AVREFM = 0 V)	

Parameter	Symbol	Cond	itions	MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error ^{Note 1}	AINL	10-bit resolution	$1.8~V \leq AV_{\text{REFP}} \leq 5.5~V$		1.2	±5.0	LSB
		$AV_{REFP} = EV_{DD} = V_{DD}$ Note 3	$1.6 \text{ V} \leq \text{AV}_{\text{REFP}} \leq 5.5 \text{ V}$ Note 4		1.2	±8.5	LSB
Conversion time	t CONV	10-bit resolution	$3.6 \text{ V} \leq \text{V}_{\text{DD}} \leq 5.5 \text{ V}$	2.125		39	μs
		AV _{REFP} = EV _{DD} = V _{DD} Note 3	$2.7~V \leq V \text{DD} \leq 5.5~V$	3.1875		39	μs
			$1.8~V \leq V \text{DD} \leq 5.5~V$	17		39	μs
			$1.6~V \leq V \text{DD} \leq 5.5~V$	57		95	μs
Zero-scale error ^{Notes 1, 2}	E _{zs}	10-bit resolution $AV_{REFP} = EV_{DD} = V_{DD}^{Note}$ 3	$1.8~V \leq AV_{\text{REFP}} \leq 5.5~V$			±0.35	%FSR
			$1.6 \text{ V} \leq AV_{\text{REFP}} \leq 5.5 \text{ V}$ Note 4			±0.60	%FSR
Full-scale error ^{Notes 1, 2}	I-scale error ^{Notes 1, 2} E _{FS} 10-bit	10-bit resolution AV _{REFP} = EV _{DD} = V_{DD} ^{Note} 3	$1.8 \text{ V} \leq AV_{\text{REFP}} \leq 5.5 \text{ V}$			±0.35	%FSR
			$1.6 \text{ V} \leq AV_{\text{REFP}} \leq 5.5 \text{ V}$ Note 4			±0.60	%FSR
Integral linearity error ^{Note 1}	ILE	10-bit resolution	$1.8 \text{ V} \leq AV_{\text{REFP}} \leq 5.5 \text{ V}$			±3.5	LSB
		$AV_{REFP} = EV_{DD} = V_{DD}$ Note 3	$1.6 \text{ V} \le \text{AV}_{\text{REFP}} \le 5.5 \text{ V}$ Note 4			±6.0	LSB
Differential linearity error	DLE	10-bit resolution	$1.8 \text{ V} \leq AV_{\text{REFP}} \leq 5.5 \text{ V}$			±2.0	LSB
Note 1	Note 1 AVREFP = Note 3	$AV_{REFP} = EV_{DD} = V_{DD}$ Note 3	$1.6 \text{ V} \le \text{AV}_{\text{REFP}} \le 5.5 \text{ V}$ Note 4			±2.5	LSB
Analog input voltage	VAIN		·	0		AV _{REFP} and EVDD	V

Notes 1. Excludes quantization error ($\pm 1/2$ LSB).

- 2. This value is indicated as a ratio (%FSR) to the full-scale value.
- 3. When AV_{REFP} < EV_{DD} = V_{DD}, the MAX. values are as follows. Overall error: Add ±4.0 LSB to the MAX. value when AV_{REFP} = V_{DD}. Zero-scale error/Full-scale error: Add ±0.20%FSR to the MAX. value when AV_{REFP} = V_{DD}. Integral linearity error/Differential linearity error: Add ±2.0 LSB to the MAX. value when AV_{REFP} = V_{DD}.
- 4. When the conversion time is set to 57 μ s (min.) and 95 μ s (max.).

(2) 1/4 bias method

 $(T_A = -40 \text{ to } +85^{\circ}\text{C}, 1.8 \text{ V} \le \text{V}_{DD} \le 5.5 \text{ V}, \text{ V}_{SS} = 0 \text{ V})$

Parameter	Symbol	Cor	nditions	MIN.	TYP.	MAX.	Unit
LCD output voltage variation range	VL1 Note 4	C1 to C5 ^{Note 1}	VLCD = 04H	0.90	1.00	1.08	V
		= 0.47 <i>µ</i> F	VLCD = 05H	0.95	1.05	1.13	V
			VLCD = 06H	1.00	1.10	1.18	V
			VLCD = 07H	1.05	1.15	1.23	V
			VLCD = 08H	1.10	1.20	1.28	V
			VLCD = 09H	1.15	1.25	1.33	V
			VLCD = 0AH	1.20	1.30	1.38	V
			VLCD = 0BH	1.25	1.35	1.43	V
			VLCD = 0CH	1.30	1.40	1.48	V
			VLCD = 0DH	1.35	1.45	1.53	V
			VLCD = 0EH	1.40	1.50	1.58	V
			VLCD = 0FH	1.45	1.55	1.63	V
			VLCD = 10H	1.50	1.60	1.68	V
			VLCD = 11H	1.55	1.65	1.73	V
			VLCD = 12H	1.60	1.70	1.78	V
			VLCD = 13H	1.65	1.75	1.83	V
Doubler output voltage	VL2	C1 to C5 ^{Note 1} =	0.47 <i>μ</i> F	$2 V_{L1} - 0.08$	2 VL1	2 VL1	V
Tripler output voltage	VL3	C1 to C5 ^{Note 1} =	0.47 <i>μ</i> F	3 VL1-0.12	3 VL1	3 VL1	V
Quadruply output voltage	VL4 Note 4	C1 to C5 ^{Note 1} =	0.47 μF	4 VL1-0.16	4 VL1	4 VL1	V
Reference voltage setup time Note 2	tvwait1			5			ms
Voltage boost wait time ^{Note 3}	tvwait2	C1 to C5 ^{Note 1} =	0.47 μF	500			ms

Notes 1. This is a capacitor that is connected between voltage pins used to drive the LCD.

C1: A capacitor connected between CAPH and CAPL

- C2: A capacitor connected between VL1 and GND
- C3: A capacitor connected between V_{L2} and GND
- C4: A capacitor connected between VL3 and GND

C5: A capacitor connected between $V_{{\scriptscriptstyle L4}}$ and GND

- C1 = C2 = C3 = C4 = C5 = 0.47 µF±30%
- 2. This is the time required to wait from when the reference voltage is specified by using the VLCD register (or when the internal voltage boosting method is selected [by setting the MDSET1 and MDSET0 bits of the LCDM0 register to 01B] if the default value reference voltage is used) until voltage boosting starts (VLCON = 1).
- 3. This is the wait time from when voltage boosting is started (VLCON = 1) until display is enabled (LCDON = 1).
- 4. VL4 must be 5.5 V or lower.

2.7.3 Capacitor split method

1/3 bias method

(TA = -40 to +85°C, 2.2 V \leq VDD \leq 5.5 V, Vss = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
VL4 voltage	VL4	C1 to C4 = 0.47 μ F ^{Note 2}		VDD		V
VL2 voltage	VL2	C1 to C4 = 0.47 μ F ^{Note 2}	2/3 VL4	2/3 VL4	2/3 VL4	V
			- 0.1		+ 0.1	
V _{L1} voltage	VL1	C1 to C4 = 0.47 μ F ^{Note 2}	1/3 VL4	1/3 VL4	1/3 VL4	V
			- 0.1		+ 0.1	
Capacitor split wait time ^{Note 1}	towait		100			ms



- **Notes 1.** Total current flowing into V_{DD} and EV_{DD}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, EV_{DD} or V_{SS}, EV_{SS}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
 - 2. During HALT instruction execution by flash memory.
 - **3.** When high-speed on-chip oscillator and subsystem clock are stopped.
 - 4. When high-speed system clock and subsystem clock are stopped.
 - 5. When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1). The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer, watchdog timer, and LCD controller/driver.
 - 6. Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.
 - 7. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below. HS (high-speed main) mode: $2.7 \text{ V} \le V_{\text{DD}} \le 5.5 \text{ V}$ @1 MHz to 24 MHz
 - $2.4~V \leq V_{\text{DD}} \leq 5.5~V@1~\text{MHz}$ to 16 MHz
 - 8. Regarding the value for current operate the subsystem clock in STOP mode, refer to that in HALT mode.
- Remarks 1. fmx: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
 - 2. fin: High-speed on-chip oscillator clock frequency
 - **3.** fsub: Subsystem clock frequency (XT1 clock oscillation frequency)
 - 4. Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is TA = 25°C



(1A40 t0 +	105 C, Z.		$0 \leq 3.5 \text{ V}, \text{ Vss}$	- EVSS - UV)	1	1	1	(3/3)
Parameter	Symbol		Conditions		MIN.	TYP.	MAX.	Unit
Low-speed on- chip oscillator operating current	_{FIL} Note 1					0.20		μA
RTC operating current	IRTC Notes 1, 2, 3	fmain is stopped				0.08		μA
12-bit interval timer current	i⊤ Notes 1, 2, 4					0.08		μA
Watchdog timer operating current	I _{WDT} Notes 1, 2, 5	f⊩ = 15 kHz				0.24		μA
A/D converter operating current	IADC Notes 1, 6	When conversion at maximum speed	Normal mode, A	$V_{REFP} = V_{DD} = 5.0 V$ de, AV _{REFP} = V _{DD} = 3.0 V		1.3 0.5	1.7 0.7	mA mA
A/D converter reference voltage current	IADREF Note 1					75.0		μA
Temperature sensor operating current	ITMPS Note 1					75.0		μA
LVD operating current	ILVD Notes 1, 7							μA
Self- programming operating current	IFSP Notes 1, 9					2.50	12.20	mA
BGO operating current	IBGO Notes 1, 8					2.50	12.20	mA
LCD operating current	ILCD1 Notes 11, 12	External resistance	e division method	$V_{DD} = EV_{DD} = 5.0 V$ $V_{L4} = 5.0 V$		0.04	0.20	μA
	ILCD2 Note 11	Internal voltage bo	osting method	V _{DD} = EV _{DD} = 5.0 V V _{L4} = 5.1 V (VLCD = 12H)		1.12	3.70	μA
				V _{DD} = EV _{DD} = 3.0 V V _{L4} = 3.0 V (VLCD = 04H)		0.63	2.20	μA
	ILCD3 Note 11	Capacitor split met	hod	$V_{DD} = EV_{DD} = 3.0 V$ $V_{L4} = 3.0 V$		0.12	0.50	μA
SNOOZE	ISNOZ Note 1	ADC operation	The mode is perfo	rmed Note 10		0.50	1.10	mA
operating current			The A/D conversion performed, Low vote = 3.0 V	n operations are litage mode, AV _{REFP} = V _{DD}		1.20	2.04	mA
		CSI/UART operation	on			0.70	1.54	mA

$(T_A = -40 \text{ to } +105^{\circ}\text{C}, 2.4 \text{ V} \le \text{EV}_{\text{DD}} = \text{V}_{\text{DD}} \le 5.5 \text{ V}, \text{V}_{\text{SS}} = \text{EV}_{\text{SS}} = 0 \text{ V})$

(3/3)

(Notes and Remarks are listed on the next page.)



Minimum Instruction Execution Time during Main System Clock Operation

TCY VS VDD (HS (high-speed main) mode)



AC Timing Test Points



External System Clock Timing



TI/TO Timing







UART mode bit width (during communication at different potential) (reference)



 $Cb[F]: \ Communication \ line \ (TxDq) \ load \ capacitance, \ Vb[V]: \ Communication \ line \ voltage$

- **2.** q: UART number (q = 0, 1), g: PIM and POM number (g = 1)
- fMCK: Serial array unit operation clock frequency (Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 01))



3.7.2 Internal voltage boosting method

(1) 1/3 bias method

(T_A = -40 to +105°C, 2.4 V \leq V_DD \leq 5.5 V, Vss = 0 V)

Parameter	Symbol	Cond	itions	MIN.	TYP.	MAX.	Unit
LCD output voltage variation range	VL1	C1 to C4 ^{Note 1}	VLCD = 04H	0.90	1.00	1.08	V
		= 0.47 <i>µ</i> F	VLCD = 05H	0.95	1.05	1.13	V
			VLCD = 06H	1.00	1.10	1.18	V
			VLCD = 07H	1.05	1.15	1.23	V
			VLCD = 08H	1.10	1.20	1.28	V
			VLCD = 09H	1.15	1.25	1.33	V
			VLCD = 0AH	1.20	1.30	1.38	V
			VLCD = 0BH	1.25	1.35	1.43	V
			VLCD = 0CH	1.30	1.40	1.48	V
			VLCD = 0DH	1.35	1.45	1.53	V
			VLCD = 0EH	1.40	1.50	1.58	V
			VLCD = 0FH	1.45	1.55	1.63	V
			VLCD = 10H	1.50	1.60	1.68	V
			VLCD = 11H	1.55	1.65	1.73	V
			VLCD = 12H	1.60	1.70	1.78	V
			VLCD = 13H	1.65	1.75	1.83	V
Doubler output voltage	VL2	C1 to C4 ^{Note 1} =	0.47 <i>μ</i> F	2 V∟1 –0.1	2 VL1	2 V _{L1}	V
Tripler output voltage	VL4	C1 to C4 ^{Note 1} = 0.47 µF		3 V∟1 –0.15	3 VL1	3 VL1	V
Reference voltage setup time Note 2	tvwait1			5			ms
Voltage boost wait time ^{Note 3}	tvwait2	C1 to C4 ^{Note 1} =	0.47 <i>μ</i> F	500			ms

Notes 1. This is a capacitor that is connected between voltage pins used to drive the LCD.

C1: A capacitor connected between CAPH and CAPL

C2: A capacitor connected between $V_{\mbox{\tiny L1}}$ and GND

C3: A capacitor connected between $V_{\mbox{\tiny L2}}$ and GND

C4: A capacitor connected between $V_{{\mbox{\tiny L4}}}$ and GND

C1 = C2 = C3 = C4 = 0.47 μ F \pm 30%

2. This is the time required to wait from when the reference voltage is specified by using the VLCD register (or when the internal voltage boosting method is selected [by setting the MDSET1 and MDSET0 bits of the LCDM0 register to 01B] if the default value reference voltage is used) until voltage boosting starts (VLCON = 1).

3. This is the wait time from when voltage boosting is started (VLCON = 1) until display is enabled (LCDON = 1).

4. PACKAGE DRAWINGS

4.1 32-pin Products

R5F10RB8AFP, R5F10RBAAFP, R5F10RBCAFP R5F10RB8GFP, R5F10RBAGFP, R5F10RBCGFP

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LQFP32-7x7-0.80	PLQP0032GB-A	P32GA-80-GBT-1	0.2



NOTE

- 1.Dimensions "%1" and "%2" do not include mold flash.
- 2.Dimension "%3" does not include trim offset.

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е

х

у

0.80

0.20

0.10



R5F10RLAANB, R5F10RLCANB R5F10RLAGNB, R5F10RLCGNB

<r></r>	JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
	P-HWQFN64-8x8-0.40	PWQN0064LA-A	P64K8-40-9B5-4	0.16

Unit: mm









Reference	Dimensions in millimeters			
Symbol	Min	Nom	Max	
D	7.95	8.00	8.05	
E	7.95	8.00	8.05	
A	_	_	0.80	
A ₁	0.00		_	
b	0.17	0.20	0.23	
е	_	0.40	—	
Lp	0.30	0.40	0.50	
х	—	_	0.05	
у	_		0.05	
ZD	_	1.00	—	
ZE	_	1.00	—	
C2	0.15	0.20	0.25	
D ₂	_	6.50	_	
E ₂	—	6.50	_	

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