What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.
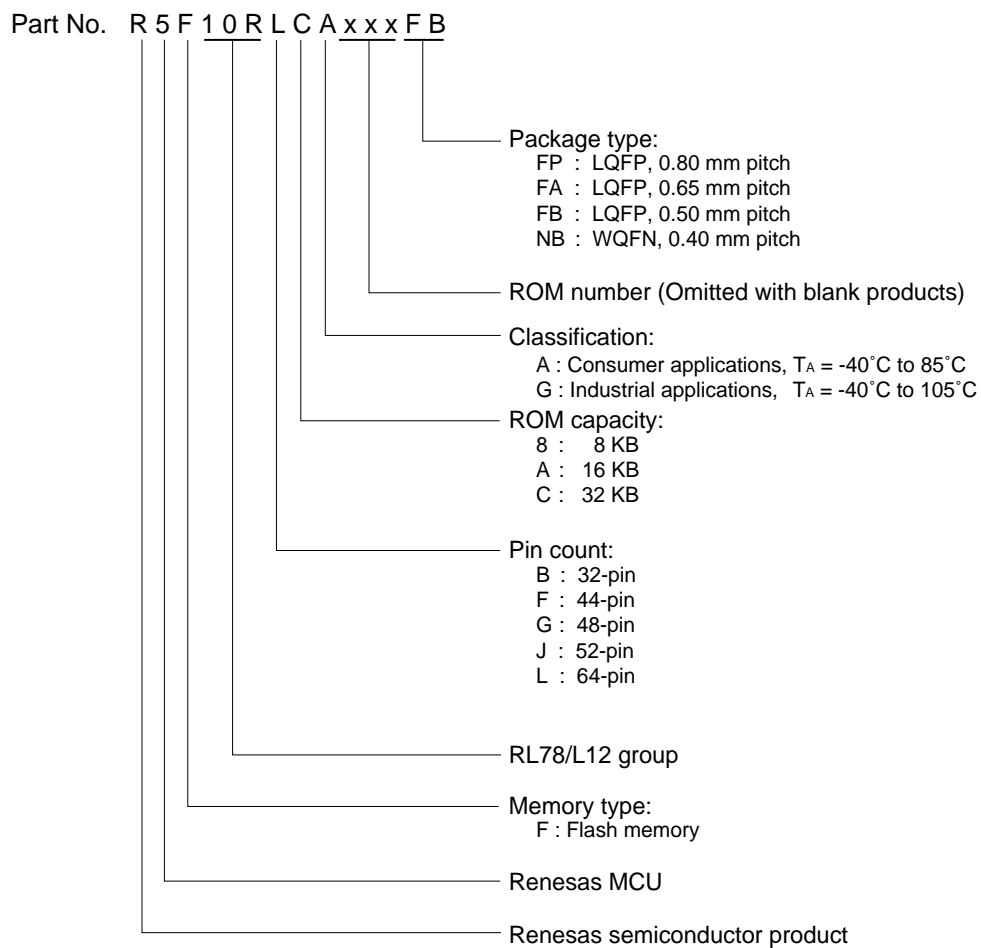
Applications of "Embedded - Microcontrollers"

Details

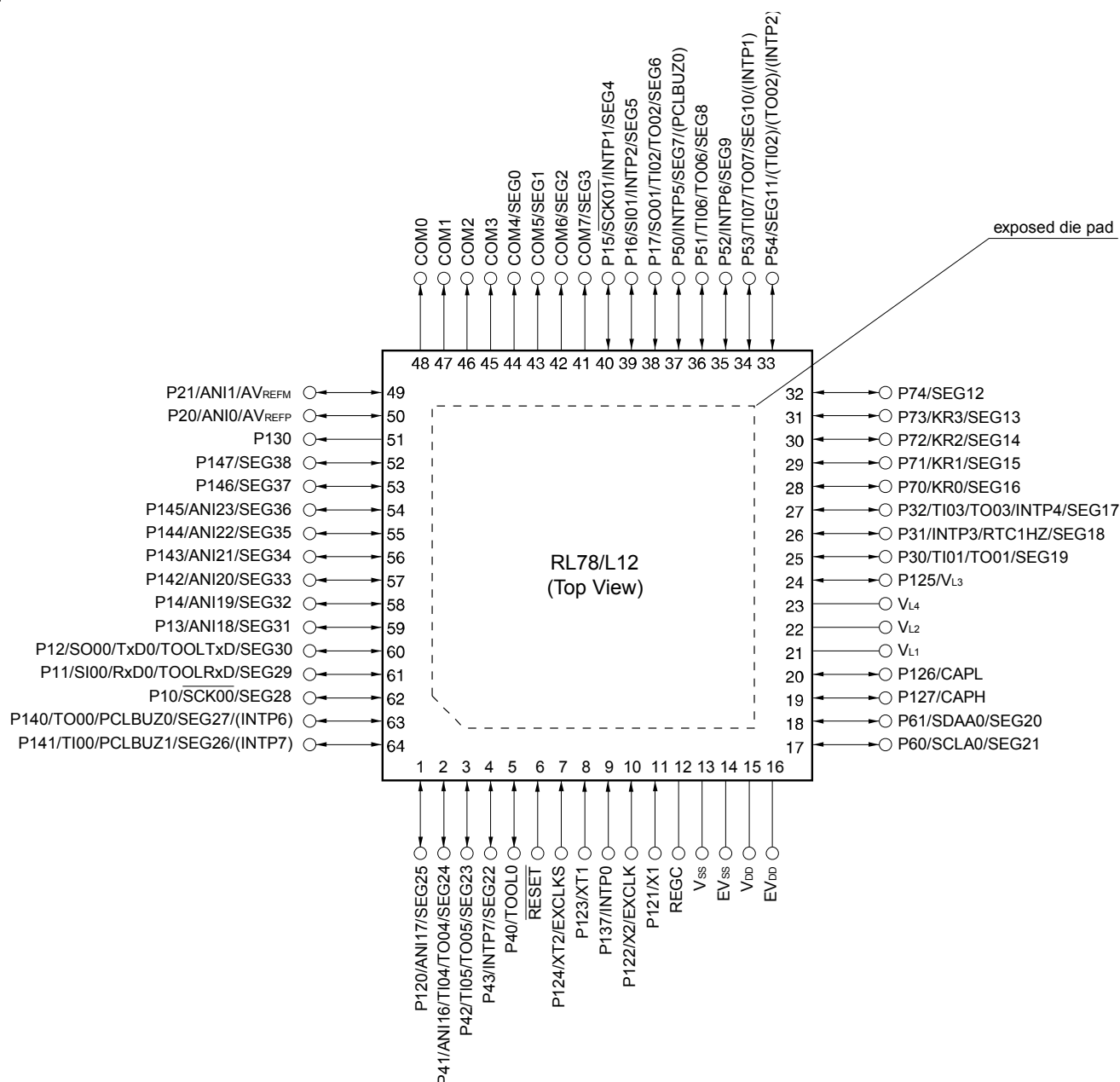|	
Product Status	Obsolete
Core Processor	RL78
Core Size	16-Bit
Speed	24MHz
Connectivity	CSI, I²C, LINbus, UART/USART
Peripherals	DMA, LCD, LVD, POR, PWM, WDT
Number of I/O	47
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	1.5K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 10x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-WFQFN Exposed Pad
Supplier Device Package	64-HWQFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f10rlcanb-u0

1.2 List of Part Numbers

Figure 1-1 Part Number, Memory Size, and Package of RL78/L12

Part No.   R 5 F 1 0 R L C A x x x F B

Package type:
FP ： LQFP, 0.80 mm pitch
FA ： LQFP, 0.65 mm pitch
FB ： LQFP, 0.50 mm pitch
NB ： WQFN, 0.40 mm pitch

ROM number (Omitted with blank products)

Classification:
A : Consumer applications, T_A = -40˚C to 85˚C
G : Industrial applications, T_A = -40˚C to 105˚C

ROM capacity:
8 ：   8 KB
A ：   16 KB
C ：   32 KB

Pin count:
B ： 32-pin
F ： 44-pin
G ： 48-pin
J ： 52-pin
L ： 64-pin

RL78/L12 group

Memory type:
F : Flash memory

Renesas MCU

Renesas semiconductor product

1.3.5 64-pin products

- 64-pin plastic WQFN (8 × 8)

<R>

Pin layout (Top View) — RL78/L12 64-pin:

Top side pins (48–33):
- 48 COM0
- 47 COM1
- 46 COM2
- 45 COM3
- 44 COM4/SEG0
- 43 COM5/SEG1
- 42 COM6/SEG2
- 41 COM7/SEG3
- 40 P15/$\overline{\text{SCK01}}$/INTP1/SEG4
- 39 P16/SI01/INTP2/SEG5
- 38 P17/SO01/TI02/TO02/SEG6
- 37 P50/INTP5/SEG7/(PCLBUZ0)
- 36 P51/TI06/TO06/SEG8
- 35 P52/INTP6/SEG9
- 34 P53/TI07/TO07/SEG10/(INTP1)
- 33 P54/SEG11/(TI02)/(TO02)/(INTP2)

exposed die pad

Left side pins (49–64):
- 49 P21/ANI1/AV$_{REFM}$
- 50 P20/ANI0/AV$_{REFP}$
- 51 P130
- 52 P147/SEG38
- 53 P146/SEG37
- 54 P145/ANI23/SEG36
- 55 P144/ANI22/SEG35
- 56 P143/ANI21/SEG34
- 57 P142/ANI20/SEG33
- 58 P14/ANI19/SEG32
- 59 P13/ANI18/SEG31
- 60 P12/SO00/TxD0/TOOLTxD/SEG30
- 61 P11/SI00/RxD0/TOOLRxD/SEG29
- 62 P10/SCK00/SEG28
- 63 P140/TO00/PCLBUZ0/SEG27/(INTP6)
- 64 P141/TI00/PCLBUZ1/SEG26/(INTP7)

Right side pins (32–17):
- 32 P74/SEG12
- 31 P73/KR3/SEG13
- 30 P72/KR2/SEG14
- 29 P71/KR1/SEG15
- 28 P70/KR0/SEG16
- 27 P32/TI03/TO03/INTP4/SEG17
- 26 P31/INTP3/RTC1HZ/SEG18
- 25 P30/TI01/TO01/SEG19
- 24 P125/V$_{L3}$
- 23 V$_{L4}$
- 22 V$_{L2}$
- 21 V$_{L1}$
- 20 P126/CAPL
- 19 P127/CAPH
- 18 P61/SDAA0/SEG20
- 17 P60/SCLA0/SEG21

Bottom side pins (1–16):
- 1 P120/ANI17/SEG25
- 2 P41/ANI16/TI04/TO04/SEG24
- 3 P42/TI05/TO05/SEG23
- 4 P43/INTP7/SEG22
- 5 P40/TOOL0
- 6 $\overline{\text{RESET}}$
- 7 P124/XT2/EXCLKS
- 8 P123/XT1
- 9 P137/INTP0
- 10 P122/X2/EXCLK
- 11 P121/X1
- 12 REGC
- 13 V$_{SS}$
- 14 EV$_{SS}$
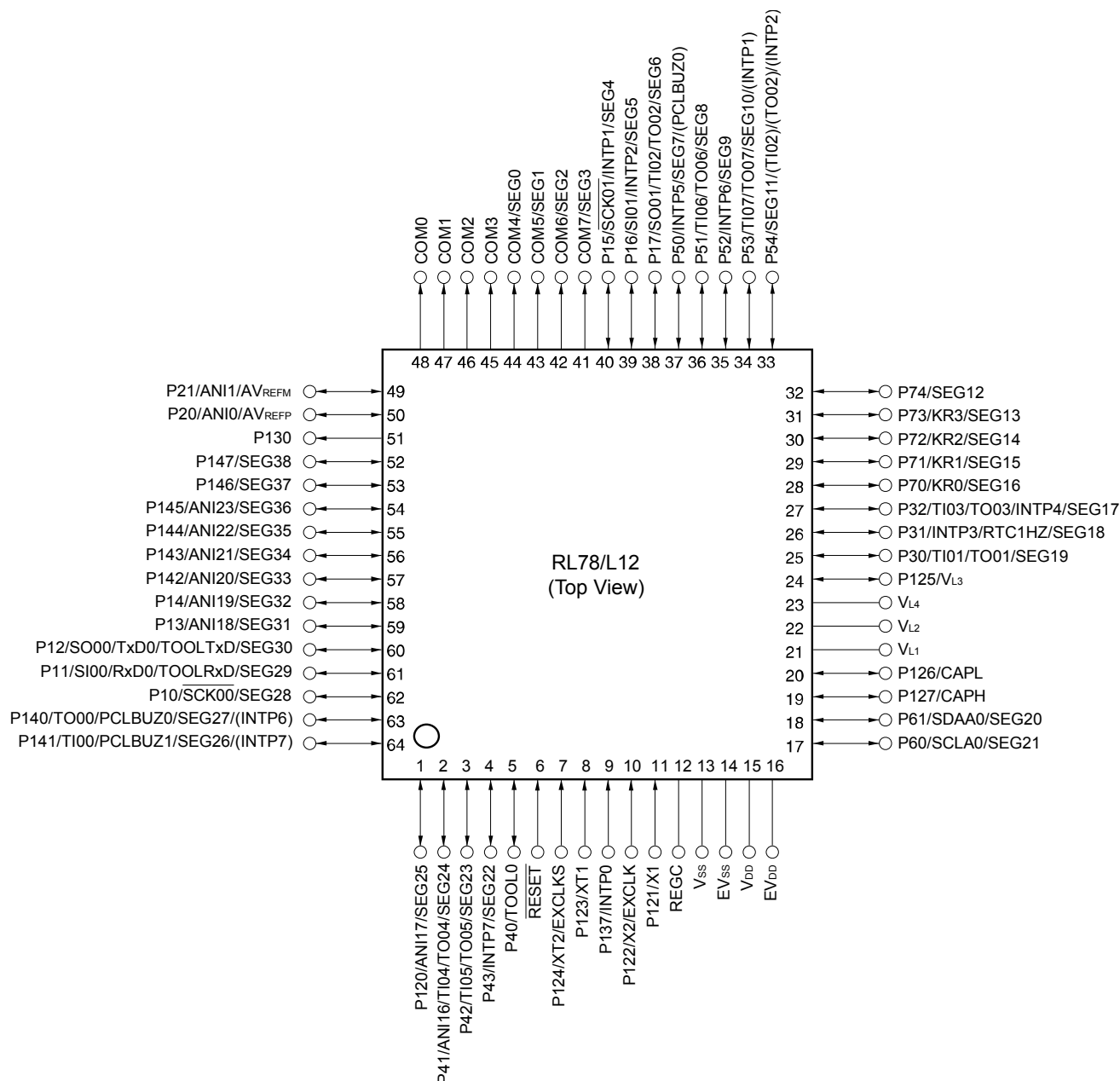- 15 V$_{DD}$
- 16 EV$_{DD}$

RL78/L12 (Top View)

Cautions 1. Make EV$_{SS}$ pin the same potential as V$_{SS}$ pin.

2. Make V$_{DD}$ pin the same potential as EV$_{DD}$ pin.

3. Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).

Remarks 1. For pin identification, see **1.4 Pin Identification.**

2. When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the V$_{DD}$ and EV$_{DD}$ pins and connect the Vss and EVss pins to separate ground lines.

3. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

- 64-pin plastic LQFP (fine pitch) (10 × 10)
- 64-pin plastic LQFP (12 × 12)

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Cautions 1. Make EVss pin the same potential as Vss pin.

　　　　　　2. Make VDD pin the same potential as EVDD pin.

　　　　　　3. Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).

Remarks 1. For pin identification, see **1.4 Pin Identification.**

　　　　　　2. When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the VDD and EVDD pins and connect the Vss and EVss pins to separate ground lines.

　　　　　　3. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

(T_A = –40 to +85°C, 1.6 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)　　　　　　　　　　　　　**(2/5)**

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, low[Note 1]	I_{OL1}	Per pin for P10 to P17, P30 to P32, P40 to P43, P50 to P54, P70 to P74, P120, P125 to P127, P130, P140 to P147				20.0 [Note 2]	mA
		Per pin for P60, P61				15.0 [Note 2]	mA
		Total of P10 to P14, P40 to P43, P120, P130, P140 to P147 (When duty = 70%[Note 3])	4.0 V ≤ EV_{DD} ≤ 5.5 V			70.0	mA
			2.7 V ≤ EV_{DD} < 4.0 V			15.0	mA
			1.8 V ≤ EV_{DD} < 2.7 V			9.0	mA
			1.6 V ≤ EV_{DD} < 1.8 V			4.5	mA
		Total of P15 to P17, P30 to P32, P50 to P54, P60, P61, P70 to P74, P125 to P127 (When duty = 70%[Note 3])	4.0 V ≤ EV_{DD} ≤ 5.5 V			80.0	mA
			2.7 V ≤ EV_{DD} < 4.0 V			35.0	mA
			1.8 V ≤ EV_{DD} < 2.7 V			20.0	mA
			1.6 V ≤ EV_{DD} < 1.8 V			10.0	mA
		Total of all pins (When duty = 70%[Note 3])				150.0	mA
	I_{OL2}	P20, P21	Per pin			0.4	mA
			Total of all pins	1.6 V ≤ V_{DD} ≤ 5.5 V		0.8	mA

Notes 1. Value of current at which the device operation is guaranteed even if the current flows from the V_{DD} and EV_{DD} pins to an output pin.

2. Do not exceed the total current value.

3. Specification under conditions where the duty factor ≤ 70%.

The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (I_{OH} × 0.7)/(n × 0.01)

<Example> Where n = 80% and I_{OL} = 70.0 mA

Total output current of pins = (70.0 × 0.7)/(80 × 0.01) ≅ 61.25 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.
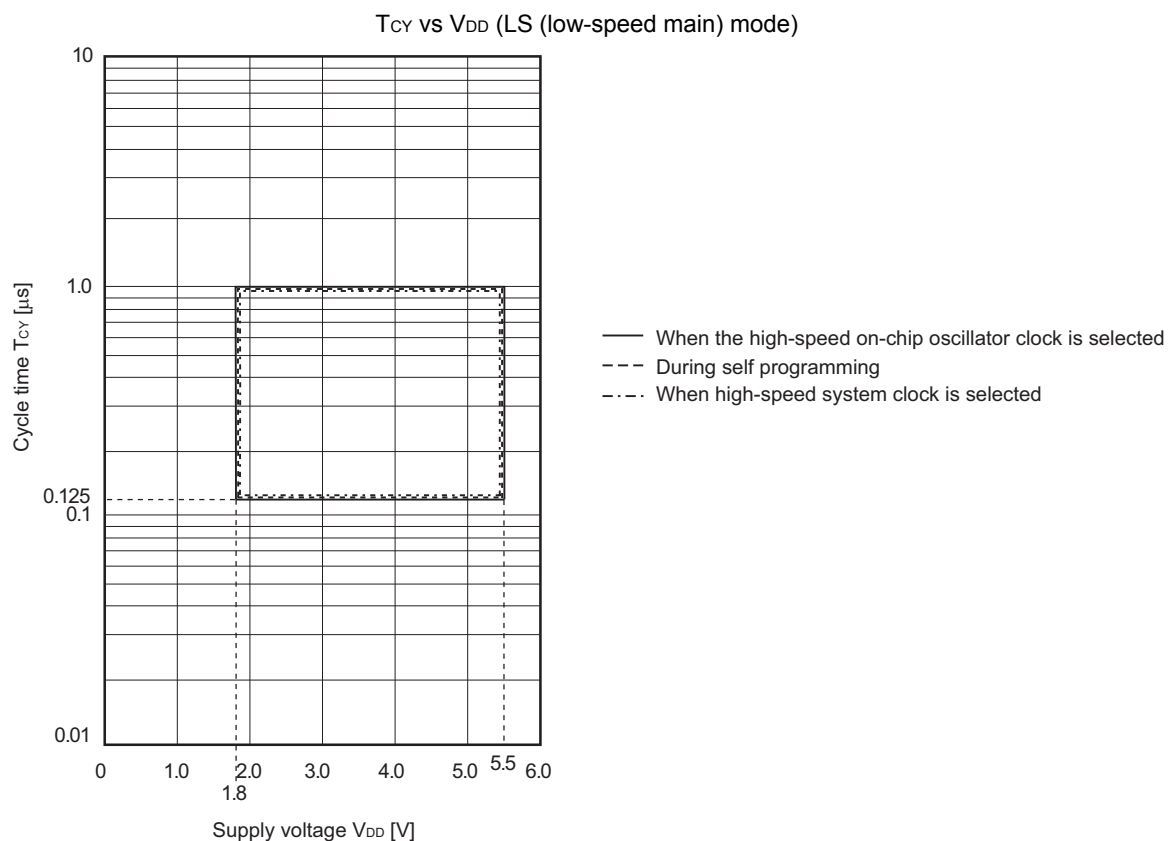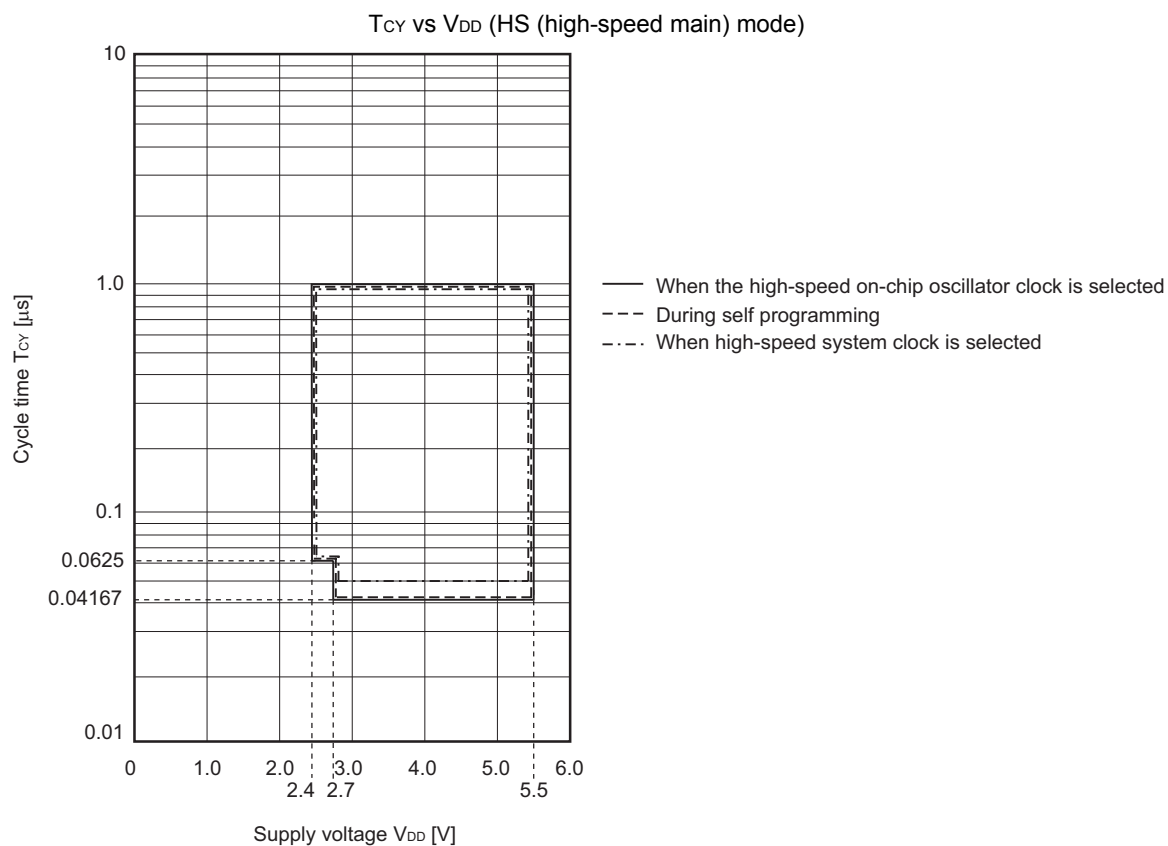
(T$_A$ = –40 to +85°C, 1.6 V ≤ EV$_{DD}$ = V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS}$ = 0 V)   **(3/5)**

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V$_{IH1}$	P10 to P17, P30 to P32, P40 to P43, P50 to P54, P70 to P74, P120, P125 to P127, P140 to P147	Normal input buffer	0.8EV$_{DD}$		EV$_{DD}$	V
	V$_{IH2}$	P10, P11, P15, P16	TTL input buffer 4.0 V ≤ EV$_{DD}$ ≤ 5.5 V	2.2		EV$_{DD}$	V
			TTL input buffer 3.3 V ≤ EV$_{DD}$ < 4.0 V	2.0		EV$_{DD}$	V
			TTL input buffer 1.6 V ≤ EV$_{DD}$ < 3.3 V	1.50		EV$_{DD}$	V
	V$_{IH3}$	P20, P21		0.7V$_{DD}$		V$_{DD}$	V
	V$_{IH4}$	P60, P61		0.7EV$_{DD}$		EV$_{DD}$	V
	V$_{IH5}$	P121 to P124, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$		0.8V$_{DD}$		V$_{DD}$	V
Input voltage, low	V$_{IL1}$	P10 to P17, P30 to P32, P40 to P43, P50 to P54, P70 to P74, P120, P125 to P127, P140 to P147	Normal input buffer	0		0.2EV$_{DD}$	V
	V$_{IL2}$	P10, P11, P15, P16	TTL input buffer 4.0 V ≤ EV$_{DD}$ ≤ 5.5 V	0		0.8	V
			TTL input buffer 3.3 V ≤ EV$_{DD}$ < 4.0 V	0		0.5	V
			TTL input buffer 1.6 V ≤ EV$_{DD}$ < 3.3 V	0		0.32	V
	V$_{IL3}$	P20, P21		0		0.3V$_{DD}$	V
	V$_{IL4}$	P60, P61		0		0.3EV$_{DD}$	V
	V$_{IL5}$	P121 to P124, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$		0		0.2V$_{DD}$	V

Caution   The maximum value of V$_{IH}$ of P10, P12, P15, P17 is EV$_{DD}$, even in the N-ch open-drain mode.

Remark   Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

Minimum Instruction Execution Time during Main System Clock Operation

T$_{CY}$ vs V$_{DD}$ (HS (high-speed main) mode)

—— When the high-speed on-chip oscillator clock is selected
--- During self programming
-·-· When high-speed system clock is selected

T$_{CY}$ vs V$_{DD}$ (LS (low-speed main) mode)

—— When the high-speed on-chip oscillator clock is selected
--- During self programming
-·-· When high-speed system clock is selected

2.7.2 Internal voltage boosting method

(1) 1/3 bias method

(T$_A$ = –40 to +85°C, 1.8 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
LCD output voltage variation range	V$_{L1}$	C1 to C4$^{Note 1}$ = 0.47 μF	VLCD = 04H	0.90	1.00	1.08	V
			VLCD = 05H	0.95	1.05	1.13	V
			VLCD = 06H	1.00	1.10	1.18	V
			VLCD = 07H	1.05	1.15	1.23	V
			VLCD = 08H	1.10	1.20	1.28	V
			VLCD = 09H	1.15	1.25	1.33	V
			VLCD = 0AH	1.20	1.30	1.38	V
			VLCD = 0BH	1.25	1.35	1.43	V
			VLCD = 0CH	1.30	1.40	1.48	V
			VLCD = 0DH	1.35	1.45	1.53	V
			VLCD = 0EH	1.40	1.50	1.58	V
			VLCD = 0FH	1.45	1.55	1.63	V
			VLCD = 10H	1.50	1.60	1.68	V
			VLCD = 11H	1.55	1.65	1.73	V
			VLCD = 12H	1.60	1.70	1.78	V
			VLCD = 13H	1.65	1.75	1.83	V
Doubler output voltage	V$_{L2}$	C1 to C4$^{Note 1}$ = 0.47 μF		2 V$_{L1}$ − 0.1	2 V$_{L1}$	2 V$_{L1}$	V
Tripler output voltage	V$_{L4}$	C1 to C4$^{Note 1}$ = 0.47 μF		3 V$_{L1}$ − 0.15	3 V$_{L1}$	3 V$_{L1}$	V
Reference voltage setup time $^{Note 2}$	t$_{VWAIT1}$			5			ms
Voltage boost wait time$^{Note 3}$	t$_{VWAIT2}$	C1 to C4$^{Note 1}$ = 0.47 μF		500			ms

Notes 1. This is a capacitor that is connected between voltage pins used to drive the LCD.

  C1: A capacitor connected between CAPH and CAPL

  C2: A capacitor connected between V$_{L1}$ and GND

  C3: A capacitor connected between V$_{L2}$ and GND

  C4: A capacitor connected between V$_{L4}$ and GND

  C1 = C2 = C3 = C4 = 0.47 μF±30%

2. This is the time required to wait from when the reference voltage is specified by using the VLCD register (or when the internal voltage boosting method is selected [by setting the MDSET1 and MDSET0 bits of the LCDM0 register to 01B] if the default value reference voltage is used) until voltage boosting starts (VLCON = 1).

3. This is the wait time from when voltage boosting is started (VLCON = 1) until display is enabled (LCDON = 1).

3. ELECTRICAL SPECIFICATIONS (G: T$_A$ = -40 to +105°C)

This chapter describes the electrical specifications for the products "G: Industrial applications (T$_A$ = -40 to +105°C)".

Cautions 1. The RL78 microcontrollers have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.

2. With products not provided with an EV$_{DD}$ or EV$_{SS}$ pin, replace EV$_{DD}$ with V$_{DD}$, or replace EV$_{SS}$ with V$_{SS}$.

3. For derating with T$_A$ = +85 to +105°C, contact our Sales Division or the vender's sales division. Derating means the specified reduction in an operating parameter to improve reliability.

Absolute Maximum Ratings (T$_A$ = 25°C) (3/3)

Parameter	Symbols	Conditions		Ratings	Unit
Output current, high	I$_{OH1}$	Per pin	P10 to P17, P30 to P32, P40 to P43, P50 to P54, P70 to P74, P120, P125 to P127, P130, P140 to P147	−40	mA
		Total of all pins −170 mA	P10 to P14, P40 to P43, P120, P130, P140 to P147	−70	mA
			P15 to P17, P30 to P32, P50 to P54, P70 to P74, P125 to P127	−100	mA
	I$_{OH2}$	Per pin	P20, P21	−0.5	mA
		Total of all pins		−1	mA
Output current, low	I$_{OL1}$	Per pin	P10 to P17, P30 to P32, P40 to P43, P50 to P54, P60, P61, P70 to P74, P120, P125 to P127, P130, P140 to P147	40	mA
		Total of all pins 170 mA	P10 to P14, P40 to P43, P120, P130, P140 to P147	70	mA
			P15 to P17, P30 to P32, P50 to P54, P60, P61, P70 to P74, P125 to P127	100	mA
	I$_{OL2}$	Per pin	P20, P21	1	mA
		Total of all pins		2	mA
Operating ambient temperature	T$_A$	In normal operation mode		−40 to +105	°C
		In flash memory programming mode			
Storage temperature	T$_{stg}$			−65 to +150	°C

Caution **Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.**

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.
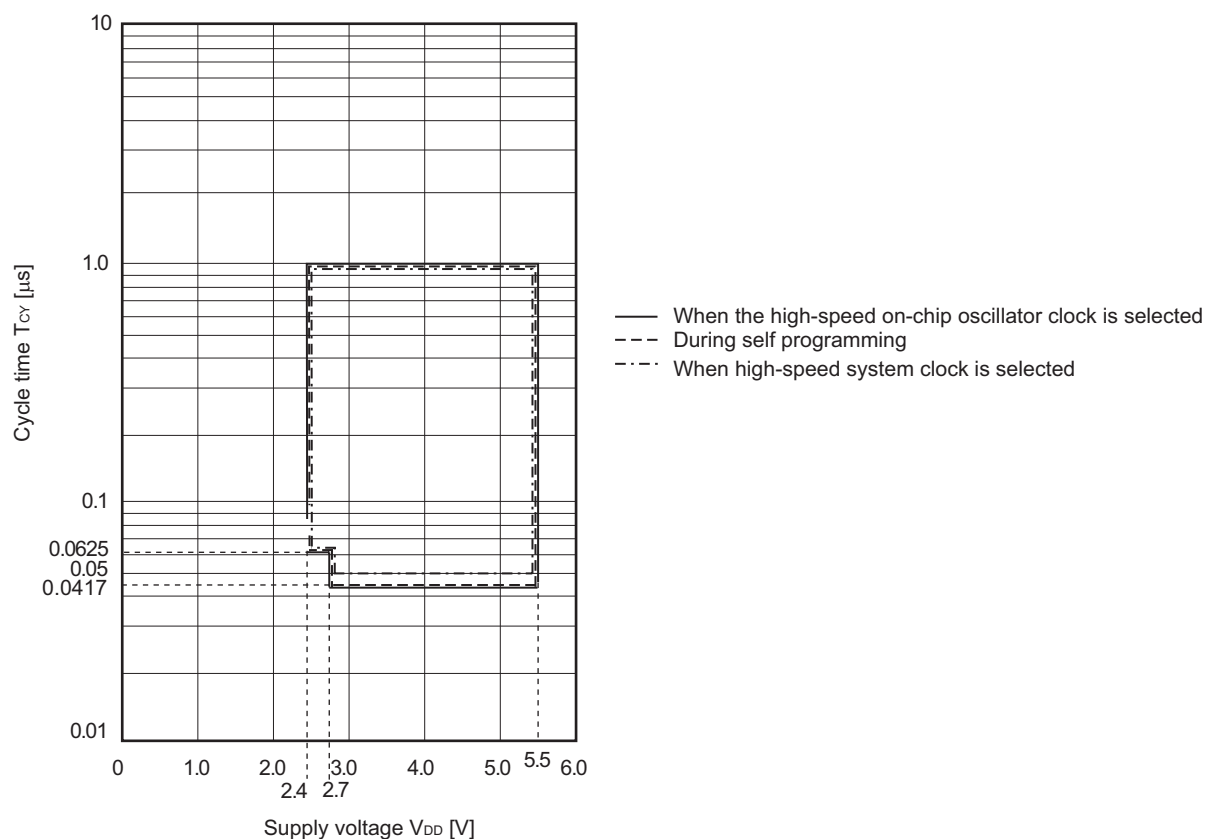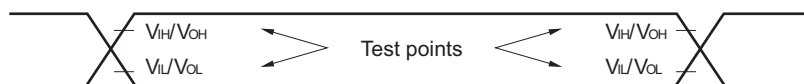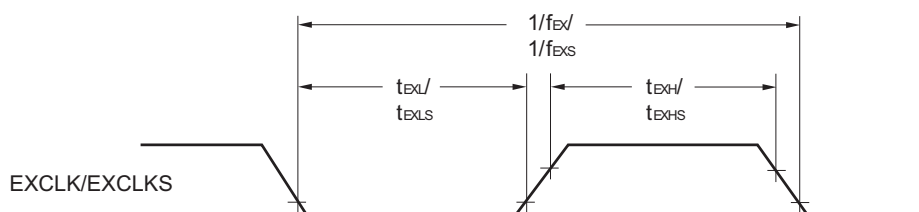
3.4 AC Characteristics

3.4.1 Basic operation

(T$_A$ = –40 to +105°C, 2.4 V ≤ EV$_{DD}$ = V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS}$ = 0 V)

Items	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Instruction cycle (minimum instruction execution time)	T$_{CY}$	Main system clock (f$_{MAIN}$) operation	HS (high-speed main) mode	2.7 V ≤ V$_{DD}$ ≤ 5.5 V	0.04167		1	μs
				2.4 V ≤ V$_{DD}$ < 2.7 V	0.0625		1	μs
		Subsystem clock (f$_{SUB}$) operation		2.4 V ≤ V$_{DD}$ ≤ 5.5 V	28.5	30.5	31.3	μs
		In the self programming mode	HS (high-speed main) mode	2.7 V ≤ V$_{DD}$ ≤ 5.5 V	0.04167		1	μs
				2.4 V ≤ V$_{DD}$ < 2.7 V	0.0625		1	μs
External system clock frequency	f$_{EX}$	2.7 V ≤ V$_{DD}$ ≤ 5.5 V			1.0		20.0	MHz
		2.4 V ≤ V$_{DD}$ < 2.7 V			1.0		16.0	MHz
	f$_{EXS}$				32		35	kHz
External system clock input high-level width, low-level width	t$_{EXH}$, t$_{EXL}$	2.7 V ≤ V$_{DD}$ ≤ 5.5 V			24			ns
		2.4 V ≤ V$_{DD}$ < 2.7 V			30			ns
	t$_{EXHS}$, t$_{EXLS}$				13.7			μs
TI00 to TI07 input high-level width, low-level width	t$_{TIH}$, t$_{TIL}$				1/f$_{MCK}$+10			ns
TO00 to TO07 output frequency	f$_{TO}$	HS (high-speed main) mode	4.0 V ≤ EV$_{DD}$ ≤ 5.5 V				16	MHz
			2.7 V ≤ EV$_{DD}$ < 4.0 V				8	MHz
			2.4 V ≤ EV$_{DD}$ < 2.7 V				4	MHz
PCLBUZ0, PCLBUZ1 output frequency	f$_{PCL}$	HS (high-speed main) mode	4.0 V ≤ EV$_{DD}$ ≤ 5.5 V				16	MHz
			2.7 V ≤ EV$_{DD}$ < 4.0 V				8	MHz
			2.4 V ≤ EV$_{DD}$ < 2.7 V				4	MHz
Interrupt input high-level width, low-level width	t$_{INTH}$, t$_{INTL}$	INTP0	2.4 V ≤ V$_{DD}$ ≤ 5.5 V		1			μs
		INTP1 to INTP7	2.4 V ≤ EV$_{DD}$ ≤ 5.5 V		1			μs
Key interrupt input low-level width	t$_{KR}$	KR0 to KR3	2.4 V ≤ EV$_{DD}$ ≤ 5.5 V		250			ns
$\overline{RESET}$ low-level width	t$_{RSL}$				10			μs

Remark f$_{MCK}$: Timer array unit operation clock frequency

(Operation clock to be set by the CKS0n bit of timer mode register 0n (TMR0n).

n: Channel number (n = 0 to 7))

Minimum Instruction Execution Time during Main System Clock Operation

T$_{CY}$ vs V$_{DD}$ (HS (high-speed main) mode)

When the high-speed on-chip oscillator clock is selected
- - - During self programming
-·-· When high-speed system clock is selected

AC Timing Test Points

V$_{IH}$/V$_{OH}$ Test points   V$_{IH}$/V$_{OH}$
V$_{IL}$/V$_{OL}$ V$_{IL}$/V$_{OL}$

External System Clock Timing

1/f$_{EX}$/
1/f$_{EXS}$

t$_{EXL}$/
t$_{EXLS}$ t$_{EXH}$/
                   t$_{EXHS}$

EXCLK/EXCLKS

(2) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output)
(T_A = –40 to +105ºC, 2.4 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		Unit
				MIN.	MAX.	
SCKp cycle time	t_{KCY1}	2.7 V ≤ EV_{DD} ≤ 5.5 V		334 [Note 1]		ns
		2.4 V ≤ EV_{DD} ≤ 5.5 V		500 [Note 1]		ns
SCKp high-/low-level width	t_{KH1},	4.0 V ≤ EV_{DD} ≤ 5.5 V		$t_{KCY1}/2 - 24$		ns
	t_{KL1}	2.7 V ≤ EV_{DD} ≤ 5.5 V		$t_{KCY1}/2 - 36$		ns
		2.4 V ≤ EV_{DD} ≤ 5.5 V		$t_{KCY1}/2 - 76$		ns
SIp setup time (to SCKp↑) [Note 2]	t_{SIK1}	2.7 V ≤ EV_{DD} ≤ 5.5 V		66		ns
		2.4 V ≤ EV_{DD} ≤ 5.5 V		113		ns
SIp hold time (from SCKp↑) [Note 3]	t_{KSI1}	2.4 V ≤ EV_{DD} ≤ 5.5 V		38		ns
Delay time from SCKp↓ to SOp output [Note 4]	t_{KSO1}	C = 30 pF [Note 5]	2.4 V ≤ EV_{DD} ≤ 5.5 V		50	ns

Notes 1. Set a cycle of 4/f_{MCK} or longer.
  2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓"
      when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
  3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓"
      when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
  4. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes
      "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
  5. C is the load capacitance of the SCKp and SOp output lines.

Caution   Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and SCKp pin
by using port input mode register g (PIMg) and port output mode register g (POMg).

Remarks 1.   p: CSI number (p = 00, 01), m: Unit number (m = 0), n: Channel number (n = 0, 1),
        g: PIM and POM numbers (g = 1)
  2. f_{MCK}: Serial array unit operation clock frequency
        (Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode
        register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 01))

(4) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode)   (1/2)

(T_A = –40 to +105°C, 2.4 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Parameter	Symbol	Conditions			HS (high-speed main) Mode		Unit
					MIN.	MAX.	
Transfer rate		Reception	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V			$f_{MCK}/12$ [Note 1]	bps
				Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} [Note 2]		2.0	Mbps
			2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V			$f_{MCK}/12$ [Note 1]	bps
				Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} [Note 2]		2.0	Mbps
			2.4 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V			$f_{MCK}/12$ [Note 1]	bps
				Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} [Note 2]		2.0	Mbps

Notes 1. Transfer rate in the SNOOZE mode is 4800 bps only.

     2. The maximum operating frequencies of the CPU/peripheral hardware clock (f_{CLK}) are:

        HS (high-speed main) mode: 24 MHz (2.7 V ≤ V_{DD} ≤ 5.5 V)

                                 16 MHz (2.4 V ≤ V_{DD} ≤ 5.5 V)

Caution   **Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance (32- to 52-pin products)/EV_{DD} tolerance (64-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.**

Remarks 1. V_b[V]: Communication line voltage

        2.   q: UART number (q = 0), g: PIM and POM number (g = 1)

        3. f_{MCK}: Serial array unit operation clock frequency

            (Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 01)

5. The smaller maximum transfer rate derived by using f_{MCK}/6 or the following expression is the valid maximum transfer rate.

   Expression for calculating the transfer rate when $1.8\ V \leq EV_{DD} < 3.3\ V$ and $1.6\ V \leq V_b \leq 2.0\ V$

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\} \times 3}\ \text{[bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100\ \text{[\%]}$$

   * This value is the theoretical value of the relative difference between the transmission and reception sides.

6. This value as an example is calculated when the conditions described in the "Conditions" column are met. Refer to Note 5 above to calculate the maximum transfer rate under conditions of the customer.

Caution   Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V$_{DD}$ tolerance (32- to 52-pin products)/EV$_{DD}$ tolerance (64-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V$_{IH}$ and V$_{IL}$, see the DC characteristics with TTL input buffer selected.

UART mode connection diagram (during communication at different potential)
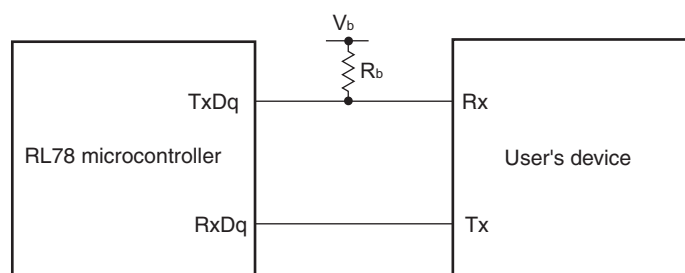
UART mode bit width (during communication at different potential) (reference)
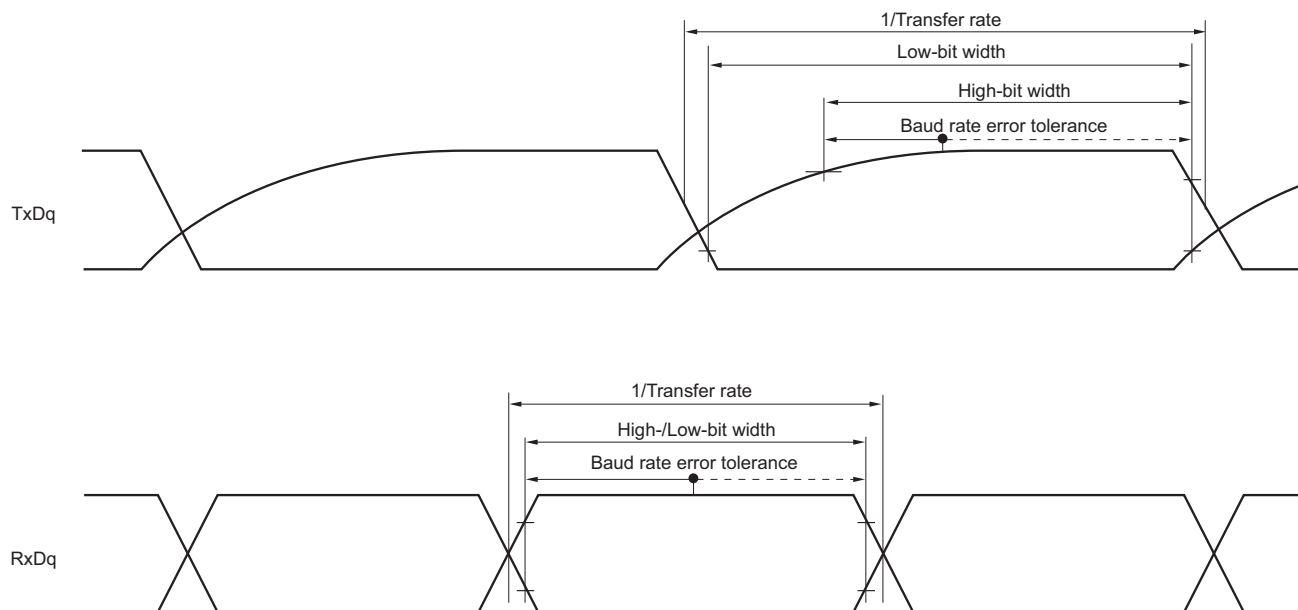
Remarks **1.** R$_b$[Ω]:Communication line (TxDq) pull-up resistance,

C$_b$[F]: Communication line (TxDq) load capacitance, V$_b$[V]: Communication line voltage

2. q: UART number (q = 0, 1), g: PIM and POM number (g = 1)

3. f$_{MCK}$: Serial array unit operation clock frequency

(Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 01))

3.6.4 LVD circuit characteristics

(T_A = –40 to +105°C, $V_{PDR} \leq EV_{DD} = V_{DD} \leq 5.5$ V, $V_{SS} = EV_{SS} = 0$ V)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	Supply voltage level	V_{LVD0}	Power supply rise time	3.90	4.06	4.22	V
			Power supply fall time	3.83	3.98	4.13	V
		V_{LVD1}	Power supply rise time	3.60	3.75	3.90	V
			Power supply fall time	3.53	3.67	3.81	V
		V_{LVD2}	Power supply rise time	3.01	3.13	3.25	V
			Power supply fall time	2.94	3.06	3.18	V
		V_{LVD3}	Power supply rise time	2.90	3.02	3.14	V
			Power supply fall time	2.85	2.96	3.07	V
		V_{LVD4}	Power supply rise time	2.81	2.92	3.03	V
			Power supply fall time	2.75	2.86	2.97	V
		V_{LVD5}	Power supply rise time	2.70	2.81	2.92	V
			Power supply fall time	2.64	2.75	2.86	V
		V_{LVD6}	Power supply rise time	2.61	2.71	2.81	V
			Power supply fall time	2.55	2.65	2.75	V
		V_{LVD7}	Power supply rise time	2.51	2.61	2.71	V
			Power supply fall time	2.45	2.55	2.65	V
Minimum pulse width		t_{LW}		300			μs
Detection delay time						300	μs

LVD Detection Voltage of Interrupt & Reset Mode
(T_A = –40 to +105°C, $V_{PDR} \leq EV_{DD} = V_{DD} \leq 5.5$ V, $V_{SS} = EV_{SS} = 0$ V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Interrupt and reset mode	V_{LVDD0}	V_{POC2}, V_{POC1}, V_{POC0} = 0, 1, 1, falling reset voltage			2.64	2.75	2.86	V
	V_{LVDD1}		LVIS1, LVIS0 = 1, 0	Rising release reset voltage	2.81	2.92	3.03	V
				Falling interrupt voltage	2.75	2.86	2.97	V
	V_{LVDD2}		LVIS1, LVIS0 = 0, 1	Rising release reset voltage	2.90	3.02	3.14	V
				Falling interrupt voltage	2.85	2.96	3.07	V
	V_{LVDD3}		LVIS1, LVIS0 = 0, 0	Rising release reset voltage	3.90	4.06	4.22	V
				Falling interrupt voltage	3.83	3.98	4.13	V

3.6.5 Power supply voltage rising slope characteristics

(T_A = –40 to +105°C, $V_{SS} = 0$ V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power supply voltage rising slope	S_{VDD}				54	V/ms

Caution   **Make sure to keep the internal reset state by the LVD circuit or an external reset until V_{DD} reaches the operating voltage range shown in 31.4 AC Characteristics.**

3.11 Timing Specifications for Switching Flash Memory Programming Modes

(TA = −40 to +105°C, 2.4 V ≤ EVDD = VDD ≤ 5.5 V, VSS = EVSS = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Time to complete the communication for the initial setting after the external reset is released	t_{SUINIT}	POR and LVD reset must be released before the external reset is released.			100	ms
Time to release the external reset after the TOOL0 pin is set to the low level	t_{SU}	POR and LVD reset must be released before the external reset is released.	10			μs
Time to hold the TOOL0 pin at the low level after the external reset is released (excluding the processing time of the firmware to control the flash memory)	t_{HD}	POR and LVD reset must be released before the external reset is released.	1			ms
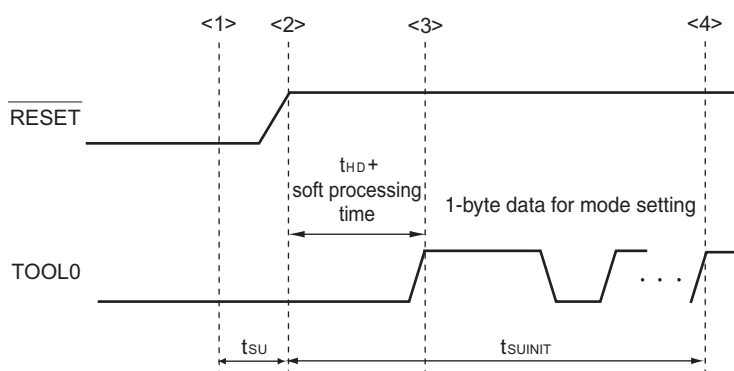
<1> The low level is input to the TOOL0 pin.

<2> The external reset is released (POR and LVD reset must be released before the external reset is released.).

<3> The TOOL0 pin is set to the high level.

<4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

Remark t_{SUINIT}: Communication for the initial setting must be completed within 100 ms after the external reset is released during this period.

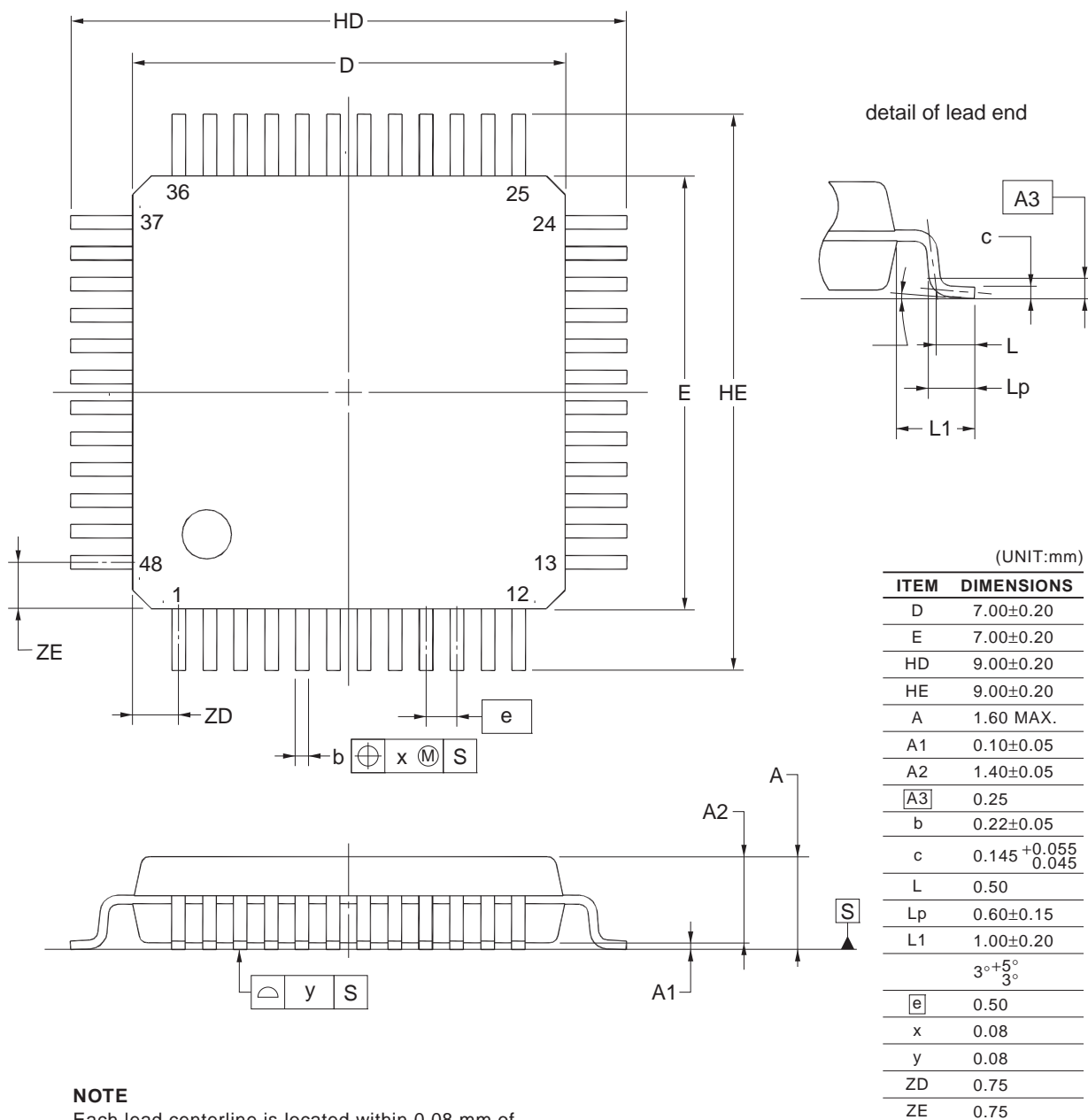t_{SU}:　　Time to release the external reset after the TOOL0 pin is set to the low level

t_{HD}:　　Time to hold the TOOL0 pin at the low level after the external reset is released (excluding the processing time of the firmware to control the flash memory)

4.3 48-pin Products

R5F10RG8AFB, R5F10RGAAFB, R5F10RGCAFB
R5F10RG8GFB, R5F10RGAGFB, R5F10RGCGFB

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LFQFP48-7x7-0.50	PLQP0048KF-A	P48GA-50-8EU-1	0.16

detail of lead end

(UNIT:mm)

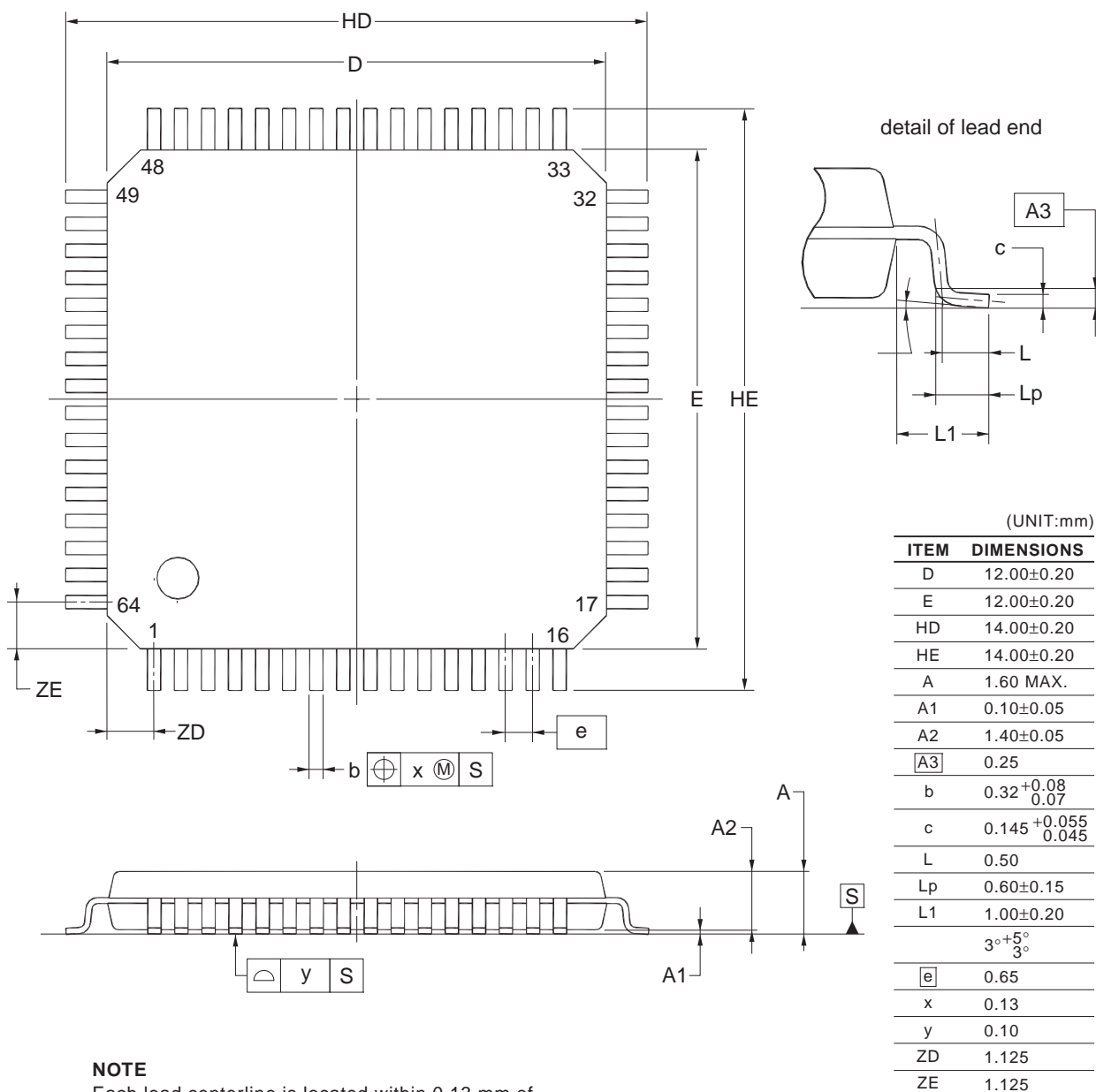| ITEM	DIMENSIONS
D	7.00±0.20
E	7.00±0.20
HD	9.00±0.20
HE	9.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
A3	0.25
b	0.22±0.05
c	$0.145 {\,}^{+0.055}_{-0.045}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
	$3° {\,}^{+5°}_{-3°}$
e	0.50
x	0.08
y	0.08
ZD	0.75
ZE	0.75

NOTE
Each lead centerline is located within 0.08 mm of
its true position at maximum material condition.

4.5 64-pin Products

R5F10RLAAFA, R5F10RLCAFA
R5F10RLAGFA, R5F10RLCGFA

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LQFP64-12x12-0.65	PLQP0064JA-A	P64GK-65-UET-2	0.51

detail of lead end

(UNIT:mm)

ITEM	DIMENSIONS
D	12.00±0.20
E	12.00±0.20
HD	14.00±0.20
HE	14.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
A3	0.25
b	$0.32^{+0.08}_{-0.07}$
c	$0.145^{+0.055}_{-0.045}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
	$3°^{+5°}_{-3°}$
e	0.65
x	0.13
y	0.10
ZD	1.125
ZE	1.125

NOTE
Each lead centerline is located within 0.13 mm of
its true position at maximum material condition.

Rev.	Date	Page	Description
			Summary
0.01	Feb 20, 2012	-	First Edition issued
0.02	Sep 26, 2012	7, 8	Modification of caution 2 in 1.3.5 64-pin products
		15	Modification of I/O port in 1.6 Outline of Functions
		-	Modification of 2. ELECTRICAL SPECIFICATIONS (TARGET)
		-	Update of package drawings in 3. PACKAGE DRAWINGS
1.00	Jan 31, 2013	11 to 15	Modification of 1.5 Block Diagram
		16	Modification of Note 2 in 1.6 Outline of Functions
		17	Modification of 1.6 Outline of Functions
		-	Deletion of target in 2. ELECTRICAL SPECIFICATIONS
		18	Addition of caution 2 to 2. ELECTRICAL SPECIFICATIONS
		19	Addition of description, note 3, and remark 2 to 2.1 Absolute Maximum Ratings
		20	Modification of description and addition of note to 2.1 Absolute Maximum Ratings
		22, 23	Modification of 2.2 Oscillator Characteristics
		30	Modification of notes 1 to 4 in 2.3.2 Supply current characteristics
		32	Modification of notes 1, 3 to 6, 8 in 2.3.2 Supply current characteristics
		34	Modification of notes 7, 9, 11, and addition of notes 8, 12 to 2.3.2 Supply current characteristics
		36	Addition of description to 2.4 AC Characteristics
		38, 40 to 42, 44 to 46, 48 to 52, 54, 55	Modification of 2.5.1 Serial array unit
		57, 58	Modification of 2.5.2 Serial interface IICA
		62	Modification of 2.6.2 Temperature sensor/internal reference voltage characteristics
		64	Addition of note and caution in 2.6.5 Supply voltage rise time
		69	Modification of 2.8 Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics
		69	Modification of conditions in 2.9 Timing Specs for Switching Flash Memory Programming Modes
		70	Modification of 2.10 Timing Specifications for Switching Flash Memory Programming Modes
2.00	Jan 10, 2014	1	Modification of 1.1 Features
		3	Modification of Figure 1-1
		4	Modification of part number, note, and caution
		5 to 10	Deletion of COMEXP pin in 1.3.1 to 1.3.5.
		11	Modification of description in 1.4 Pin Identification
		12 to 16	Deletion of COMEXP pin in 1.5.1 to 1.5.5
		17	Modification of table and note 2 in 1.6 Outline of Functions
		20	Modification of description in Absolute Maximum Ratings (T_A = 25°C) (1/3)
		21	Modification of description and note 2 in Absolute Maximum Ratings (T_A = 25°C) (2/3)
		23	Modification of table, note, caution, and remark in 2.2.1 X1, XT1 oscillator characteristics
		23	Modification of table in 2.2.2 On-chip oscillator characteristics
		24	Modification of table, notes 2 and 3 in 2.3.1 Pin characteristics (1/5)
		25	Modification of notes 1 and 3 in 2.3.1 Pin characteristics (2/5)
		30	Modification of notes 1 and 4 in 2.3.2 Supply current characteristics (1/3)
		31, 32	Modification of table, notes 1, 5, and 6 in 2.3.2 Supply current characteristics (2/3)
		33, 34	Modification of table, notes 1, 3, 4, and 5 to 10 in 2.3.2 Supply current characteristics (3/3)