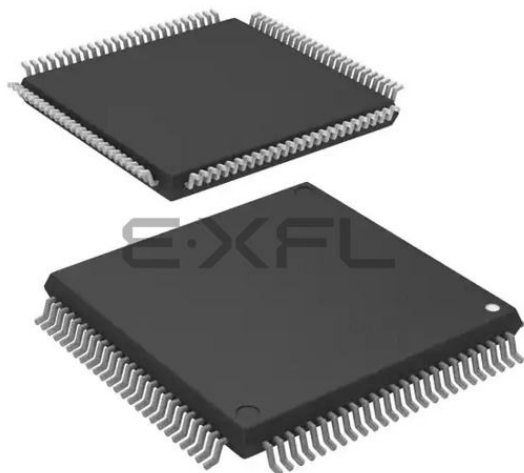




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Details

Product Status	Last Time Buy
Core Processor	R32C/100
Core Size	16/32-Bit
Speed	50MHz
Connectivity	EBI/EMI, I ² C, IEBus, UART/USART
Peripherals	DMA, LVD, PWM, WDT
Number of I/O	84
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	63K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 26x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f64169dfb-u0

1.2 Product Information

Tables 1.5 and 1.6 list the product information and Figure 1.1 shows the details of the part number.

Table 1.5 R32C/116 Group Product List for Normal Speed Version (1/2) As of February, 2013

Part Number	Package Code (1)	ROM Capacity (2)	RAM Capacity	Remarks
R5F64165NFD (P)	PLQP0144KA-A	384 Kbytes + 8 Kbytes	40 Kbytes	-20°C to 85°C (N version)
R5F64165DFD				-40°C to 85°C (D version)
R5F64165PFD				-40°C to 85°C (P version)
R5F64165NFB (P)	PLQP0100KB-A			-20°C to 85°C (N version)
R5F64165DFB				-40°C to 85°C (D version)
R5F64165PFB				-40°C to 85°C (P version)
R5F64166NFD (P)	PLQP0144KA-A	512 Kbytes + 8 Kbytes	40 Kbytes	-20°C to 85°C (N version)
R5F64166DFD				-40°C to 85°C (D version)
R5F64166PFD				-40°C to 85°C (P version)
R5F64166NFB (P)	PLQP0100KB-A			-20°C to 85°C (N version)
R5F64166DFB				-40°C to 85°C (D version)
R5F64166PFB				-40°C to 85°C (P version)
R5F64167NFD (P)	PLQP0144KA-A	640 Kbytes + 8 Kbytes	48 Kbytes	-20°C to 85°C (N version)
R5F64167DFD				-40°C to 85°C (D version)
R5F64167PFD				-40°C to 85°C (P version)
R5F64167NFB (P)	PLQP0100KB-A			-20°C to 85°C (N version)
R5F64167DFB				-40°C to 85°C (D version)
R5F64167PFB				-40°C to 85°C (P version)
R5F64168NFD (P)	PLQP0144KA-A	768 Kbytes + 8 Kbytes	63 Kbytes	-20°C to 85°C (N version)
R5F64168DFD				-40°C to 85°C (D version)
R5F64168PFD				-40°C to 85°C (P version)
R5F64168NFB (P)	PLQP0100KB-A			-20°C to 85°C (N version)
R5F64168DFB				-40°C to 85°C (D version)
R5F64168PFB				-40°C to 85°C (P version)
R5F64169NFD (P)	PLQP0144KA-A	1 Mbyte + 8 Kbytes	63 Kbytes	-20°C to 85°C (N version)
R5F64169DFD				-40°C to 85°C (D version)
R5F64169PFD				-40°C to 85°C (P version)
R5F64169NFB (P)	PLQP0100KB-A			-20°C to 85°C (N version)
R5F64169DFB				-40°C to 85°C (D version)
R5F64169PFB				-40°C to 85°C (P version)

(P): On planning phase

Notes:

- The old package codes are as follows:
PLQP0100KB-A: 100P6Q-A; PLQP0144KA-A: 144P6Q-A
- "8 Kbytes" in the ROM capacity indicates the data flash memory capacity.

Table 1.10 Pin Characteristics for the 144-pin Package (4/4)

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	UART Pin	Intelligent I/O Pin	Analog Pin	Bus Control Pin
115		P11_3			CTS8/RTS8	IIO1_3		CS3/WR2
116		P11_2			RXD8	IIO1_2		CS2
117		P11_1			CLK8	IIO1_1		CS1
118		P11_0			TXD8	IIO1_0		CS0
119		P0_3					AN0_3	D3
120		P0_2					AN0_2	D2
121		P0_1					AN0_1	D1
122		P0_0					AN0_0	D0
123		P15_7			CTS6/RTS6/SS6	IIO0_7	AN15_7	
124		P15_6			CLK6	IIO0_6	AN15_6	
125		P15_5			RXD6/SCL6/STXD6	IIO0_5	AN15_5	
126		P15_4			TXD6/SDA6/SRXD6	IIO0_4	AN15_4	
127		P15_3			CTS7/RTS7	IIO0_3	AN15_3	
128		P15_2			RXD7	IIO0_2	AN15_2	
129		P15_1			CLK7	IIO0_1	AN15_1	
130	VSS							
131		P15_0			TXD7	IIO0_0	AN15_0	
132	VCC							
133		P10_7	KI3				AN_7	
134		P10_6	KI2				AN_6	
135		P10_5	KI1				AN_5	
136		P10_4	KI0				AN_4	
137		P10_3					AN_3	
138		P10_2					AN_2	
139		P10_1					AN_1	
140	AVSS							
141		P10_0					AN_0	
142	VREF							
143	AVCC							
144		P9_7			RXD4/SCL4/STXD4		ADTRG	

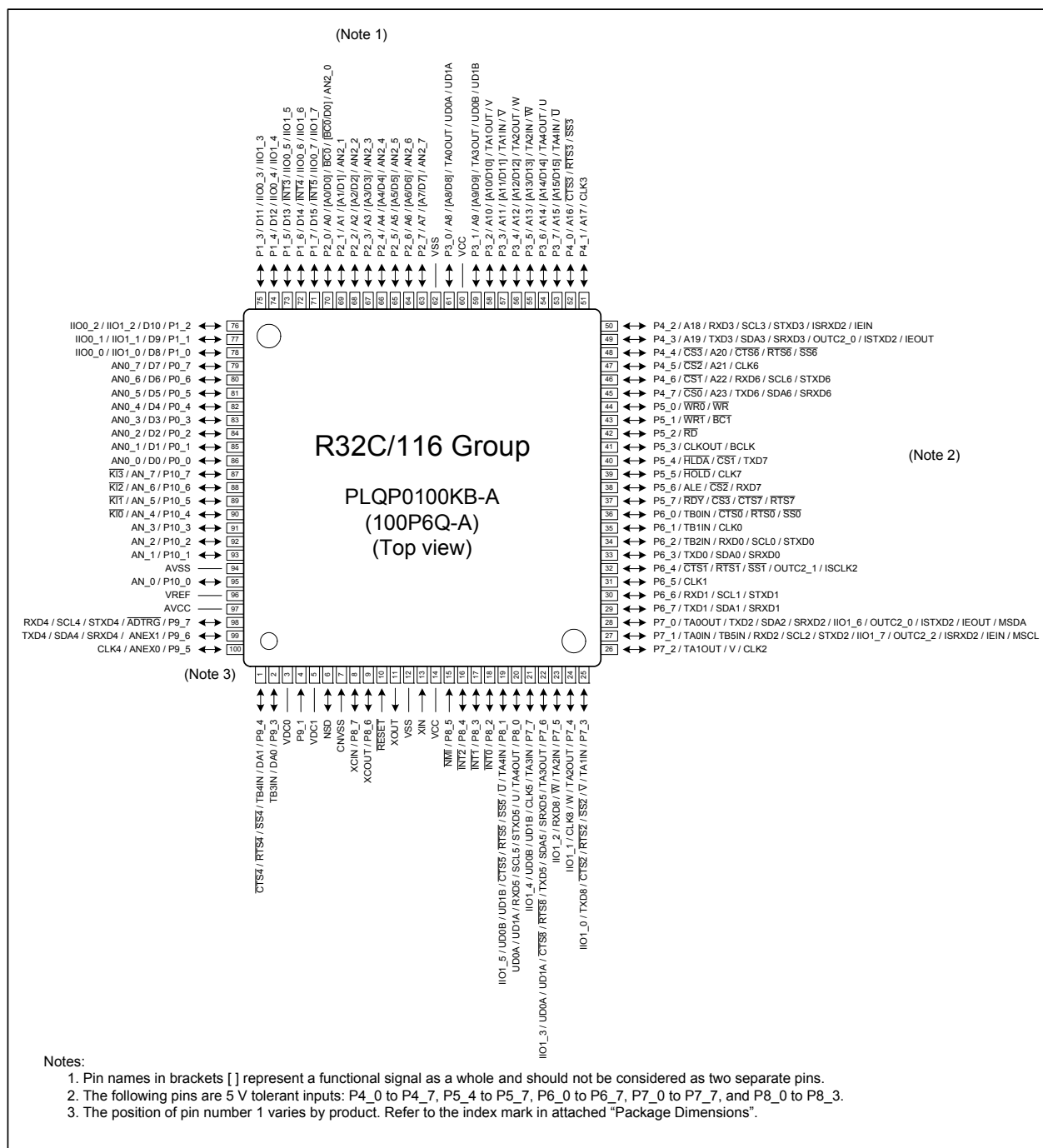


Figure 1.4 Pin Assignment for the 100-pin Package (top view)

1.5 Pin Definitions and Functions

Tables 1.14 to 1.18 list the pin definitions and functions.

Table 1.14 Pin Definitions and Functions (1/4)

Function	Symbol	I/O	Description
Power supply	VCC, VSS	I	Applicable as follows: VCC = 3.0 to 5.5 V, VSS = 0 V
Connecting pins for decoupling capacitor	VDC0, VDC1	—	A decoupling capacitor for internal voltage should be connected between VDC0 and VDC1
Analog power supply	AVCC, AVSS	I	Power supply for the A/D converter. AVCC and AVSS should be connected to VCC and VSS, respectively
Reset input	$\overline{\text{RESET}}$	I	The MCU is reset when this pin is driven low
CNVSS	CNVSS	I	This pin should be connected to VSS via a resistor
Debug port	NSD	I/O	This pin is to communicate with a debugger. It should be connected to VCC via a resistor of 1 to 4.7 k Ω
Main clock input	XIN	I	Input/output for the main clock oscillator. A crystal, or a ceramic resonator should be connected between pins XIN and XOUT. An external clock should be input at the XIN while leaving the XOUT open
Main clock output	XOUT	O	
Sub clock input	XCIN	I	Input/output for the sub clock oscillator. A crystal oscillator should be connected between pins XCIN and XCOU. An external clock should be input at the XCIN while leaving the XCOU open
Sub clock output	XCOU	O	
BCLK output	BCLK	O	BCLK output
Clock output	CLKOUT	O	Output of the clock with the same frequency as low speed clocks, f8, or f32
External interrupt input	$\overline{\text{INT0}}$ to $\overline{\text{INT8}}$ ⁽¹⁾	I	Input for external interrupts
NMI input	P8_5/ $\overline{\text{NMI}}$	I	Input for NMI
Key input interrupt	KI0 to KI3	I	Input for the key input interrupt
Bus control pins	D0 to D7	I/O	Input/output of data (D0 to D7) while accessing an external memory space with a separate bus
	D8 to D15	I/O	Input/output of data (D8 to D15) while accessing an external memory space with 16-bit or 32-bit separate bus
	D16 to D31 ⁽²⁾	I/O	Input/output of data (D16 to D31) while accessing an external memory space with 32-bit separate bus
	A0 to A23	O	Output of address bits A0 to A23
	A0/D0 to A7/D7	I/O	Output of address bits (A0 to A7) and input/output of data (D0 to D7) by time-division while accessing an external memory space with multiplexed bus
	A8/D8 to A15/D15	I/O	Output of address bits (A8 to A15) and input/output of data (D8 to D15) by time-division while accessing an external memory space with 16-bit or 32-bit multiplexed bus

Notes:

1. Pins $\overline{\text{INT6}}$ to $\overline{\text{INT8}}$ are available in the 144-pin package only.
2. Pins D16 to D31 are available in the 144-pin package only.

Table 1.16 Pin Definitions and Functions (3/4)

Function	Symbol	I/O	Description
I/O port (1, 2)	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7, P14_3 to P14_6, P15_0 to P15_7	I/O	I/O ports in CMOS. Each port can be programmed to input or output under the control of the direction register. Some ports are 5 V tolerant inputs. Pull-up resistors and N-channel open drain setting can be enabled on some ports. Refer to Table 1.18 "Pin Specifications" for details
Input port (2)	P9_1 (for 100-pin package) P14_1 (for 144-pin package)	I	Input port in CMOS Pull-up resistor is selectable. Refer to Table 1.18 "Pin Specifications" for details
Timer A	TA0OUT to TA4OUT	I/O	Timers A0 to A4 input/output
	TA0IN to TA4IN	I	Timers A0 to A4 input
Timer B	TB0IN to TB5IN	I	Timers B0 to B5 input
Three-phase motor control timer output	U, $\bar{U}$, V, $\bar{V}$, W, $\bar{W}$	O	Three-phase motor control timer output
Serial interface	CTS0 to CTS8	I	Handshake input
	RTS0 to RTS8	O	Handshake output
	CLK0 to CLK8	I/O	Transmit/receive clock input/output
	RXD0 to RXD8	I	Serial data input
	TXD0 to TXD8	O	Serial data output
I ² C-bus (simplified)	SDA0 to SDA6	I/O	Serial data input/output
	SCL0 to SCL6	I/O	Transmit/receive clock input/output
Serial interface special functions	STXD0 to STXD6	O	Serial data output in slave mode
	SRXD0 to SRXD6	I	Serial data input in slave mode
	SS0 to SS6	I	Input to control serial interface special functions

Notes:

1. Port P9_1 in the 100-pin package is an input-only port.
2. Ports P9_0, P9_2, and P11 to P15 are available in the 144-pin package only.

2.2 Fast Interrupt Registers

The following three registers are provided to minimize the overhead of the interrupt sequence.

2.2.1 Save Flag Register (SVF)

This 32-bit register is used to save the flag register when a fast interrupt occurs.

2.2.2 Save PC Register (SVP)

This 32-bit register is used to save the program counter when a fast interrupt occurs.

2.2.3 Vector Register (VCT)

This 32-bit register is used to indicate a jump address when a fast interrupt occurs.

2.3 DMAC-associated Registers

There are seven types of DMAC-associated registers.

2.3.1 DMA Mode Registers (DMD0, DMD1, DMD2, and DMD3)

These 32-bit registers are used to set DMA transfer mode, bit rate, etc.

2.3.2 DMA Terminal Count Registers (DCT0, DCT1, DCT2, and DCT3)

These 24-bit registers are used to set the number of DMA transfers.

2.3.3 DMA Terminal Count Reload Registers (DCR0, DCR1, DCR2, and DCR3)

These 24-bit registers are used to set the reloaded values for DMA terminal count registers.

2.3.4 DMA Source Address Registers (DSA0, DSA1, DSA2, and DSA3)

These 32-bit registers are used to set DMA source addresses.

2.3.5 DMA Source Address Reload Registers (DSR0, DSR1, DSR2, and DSR3)

These 32-bit registers are used to set the reloaded values for DMA source address registers.

2.3.6 DMA Destination Address Registers (DDA0, DDA1, DDA2, and DDA3)

These 32-bit registers are used to set DMA destination addresses.

2.3.7 DMA Destination Address Reload Registers (DDR0, DDR1, DDR2, and DDR3)

These 32-bit registers are used to set reloaded values for DMA destination address registers.

Table 4.2 SFR List (2)

Address	Register	Symbol	Reset Value
000060h			
000061h	Timer B5 Interrupt Control Register	TB5IC	XXXX X000b
000062h	UART5 Transmit/NACK Interrupt Control Register	S5TIC	XXXX X000b
000063h	UART2 Receive/ACK Interrupt Control Register/I ² C-bus Line Interrupt Control Register	S2RIC/I2CLIC	XXXX X000b
000064h	UART6 Transmit/NACK Interrupt Control Register	S6TIC	XXXX X000b
000065h	UART3 Receive/ACK Interrupt Control Register	S3RIC	XXXX X000b
000066h	UART5/6 Bus Collision, START Condition/STOP Condition Detection Interrupt Control Register	BCN5IC/BCN6IC	XXXX X000b
000067h	UART4 Receive/ACK Interrupt Control Register	S4RIC	XXXX X000b
000068h	DMA0 Transfer Complete Interrupt Control Register	DM0IC	XXXX X000b
000069h	UART0/3 Bus Collision, START Condition/STOP Condition Detection Interrupt Control Register	BCN0IC/BCN3IC	XXXX X000b
00006Ah	DMA2 Transfer Complete Interrupt Control Register	DM2IC	XXXX X000b
00006Bh	A/D Converter 0 Convert Completion Interrupt Control Register	AD0IC	XXXX X000b
00006Ch	Timer A0 Interrupt Control Register	TA0IC	XXXX X000b
00006Dh	Intelligent I/O Interrupt Control Register 0	IIO0IC	XXXX X000b
00006Eh	Timer A2 Interrupt Control Register	TA2IC	XXXX X000b
00006Fh	Intelligent I/O Interrupt Control Register 2	IIO2IC	XXXX X000b
000070h	Timer A4 Interrupt Control Register	TA4IC	XXXX X000b
000071h	Intelligent I/O Interrupt Control Register 4	IIO4IC	XXXX X000b
000072h	UART0 Receive/ACK Interrupt Control Register	S0RIC	XXXX X000b
000073h	Intelligent I/O Interrupt Control Register 6	IIO6IC	XXXX X000b
000074h	UART1 Receive/ACK Interrupt Control Register	S1RIC	XXXX X000b
000075h	Intelligent I/O Interrupt Control Register 8	IIO8IC	XXXX X000b
000076h	Timer B1 Interrupt Control Register	TB1IC	XXXX X000b
000077h	Intelligent I/O Interrupt Control Register 10	IIO10IC	XXXX X000b
000078h	Timer B3 Interrupt Control Register	TB3IC	XXXX X000b
000079h			
00007Ah	INT5 Interrupt Control Register	INT5IC	XX00 X000b
00007Bh			
00007Ch	INT3 Interrupt Control Register	INT3IC	XX00 X000b
00007Dh			
00007Eh	INT1 Interrupt Control Register	INT1IC	XX00 X000b
00007Fh			
000080h			
000081h	UART2 Transmit/NACK Interrupt Control Register/I ² C-bus Interrupt Control Register	S2TIC/I2CIC	XXXX X000b
000082h	UART5 Receive/ACK Interrupt Control Register	S5RIC	XXXX X000b
000083h	UART3 Transmit/NACK Interrupt Control Register	S3TIC	XXXX X000b
000084h	UART6 Receive/ACK Interrupt Control Register	S6RIC	XXXX X000b
000085h	UART4 Transmit/NACK Interrupt Control Register	S4TIC	XXXX X000b
000086h			
000087h	UART2 Bus Collision, START Condition/STOP Condition Detection Interrupt Control Register	BCN2IC	XXXX X000b

X: Undefined

Blanks are reserved. No access is allowed.

Table 4.4 SFR List (4)

Address	Register	Symbol	Reset Value
0000B0h	Intelligent I/O Interrupt Enable Register 0	IIO0IE	00h
0000B1h	Intelligent I/O Interrupt Enable Register 1	IIO1IE	00h
0000B2h	Intelligent I/O Interrupt Enable Register 2	IIO2IE	00h
0000B3h	Intelligent I/O Interrupt Enable Register 3	IIO3IE	00h
0000B4h	Intelligent I/O Interrupt Enable Register 4	IIO4IE	00h
0000B5h	Intelligent I/O Interrupt Enable Register 5	IIO5IE	00h
0000B6h	Intelligent I/O Interrupt Enable Register 6	IIO6IE	00h
0000B7h	Intelligent I/O Interrupt Enable Register 7	IIO7IE	00h
0000B8h	Intelligent I/O Interrupt Enable Register 8	IIO8IE	00h
0000B9h	Intelligent I/O Interrupt Enable Register 9	IIO9IE	00h
0000BAh	Intelligent I/O Interrupt Enable Register 10	IIO10IE	00h
0000BBh	Intelligent I/O Interrupt Enable Register 11	IIO11IE	00h
0000BCh			
0000BDh			
0000BEh			
0000BFh			
0000C0h			
0000C1h			
0000C2h			
0000C3h			
0000C4h			
0000C5h			
0000C6h			
0000C7h			
0000C8h			
0000C9h			
0000CAh			
0000CBh			
0000CCh			
0000CDh			
0000CEh			
0000CFh			
0000D0h			
0000D1h			
0000D2h			
0000D3h			
0000D4h			
0000D5h			
0000D6h			
0000D7h			
0000D8h			
0000D9h			
0000DAh			
0000DBh			
0000DCh			
0000DDh	UART7 Transmit Interrupt Control Register	S7TIC	XXXX X000b
0000DEh	INT7 Interrupt Control Register	INT7IC	XX00 X000b
0000DFh	UART8 Transmit Interrupt Control Register	S8TIC	XXXX X000b

X: Undefined

Blanks are reserved. No access is allowed.

Table 4.8 SFR List (8)

Address	Register	Symbol	Reset Value
000170h	Group 2 IEBus Address Register	IEAR	XXXXh
000171h			
000172h	Group 2 IEBus Control Register	IECR	00XX X000b
000173h	Group 2 IEBus Transmit Interrupt Source Detect Register	IETIF	XXX0 0000b
000174h	Group 2 IEBus Receive Interrupt Source Detect Register	IERIF	XXX0 0000b
000175h			
000176h			
000177h			
000178h			
000179h			
00017Ah			
00017Bh			
00017Ch			
00017Dh			
00017Eh			
00017Fh			
000180h	Group 0 Time Measurement/Waveform Generation Register 0	G0TM0/G0PO0	XXXXh
000181h			
000182h	Group 0 Time Measurement/Waveform Generation Register 1	G0TM1/G0PO1	XXXXh
000183h			
000184h	Group 0 Time Measurement/Waveform Generation Register 2	G0TM2/G0PO2	XXXXh
000185h			
000186h	Group 0 Time Measurement/Waveform Generation Register 3	G0TM3/G0PO3	XXXXh
000187h			
000188h	Group 0 Time Measurement/Waveform Generation Register 4	G0TM4/G0PO4	XXXXh
000189h			
00018Ah	Group 0 Time Measurement/Waveform Generation Register 5	G0TM5/G0PO5	XXXXh
00018Bh			
00018Ch	Group 0 Time Measurement/Waveform Generation Register 6	G0TM6/G0PO6	XXXXh
00018Dh			
00018Eh	Group 0 Time Measurement/Waveform Generation Register 7	G0TM7/G0PO7	XXXXh
00018Fh			
000190h	Group 0 Waveform Generation Control Register 0	G0POCR0	0000 X000b
000191h	Group 0 Waveform Generation Control Register 1	G0POCR1	0X00 X000b
000192h	Group 0 Waveform Generation Control Register 2	G0POCR2	0X00 X000b
000193h	Group 0 Waveform Generation Control Register 3	G0POCR3	0X00 X000b
000194h	Group 0 Waveform Generation Control Register 4	G0POCR4	0X00 X000b
000195h	Group 0 Waveform Generation Control Register 5	G0POCR5	0X00 X000b
000196h	Group 0 Waveform Generation Control Register 6	G0POCR6	0X00 X000b
000197h	Group 0 Waveform Generation Control Register 7	G0POCR7	0X00 X000b
000198h	Group 0 Time Measurement Control Register 0	G0TMCR0	00h
000199h	Group 0 Time Measurement Control Register 1	G0TMCR1	00h
00019Ah	Group 0 Time Measurement Control Register 2	G0TMCR2	00h
00019Bh	Group 0 Time Measurement Control Register 3	G0TMCR3	00h
00019Ch	Group 0 Time Measurement Control Register 4	G0TMCR4	00h
00019Dh	Group 0 Time Measurement Control Register 5	G0TMCR5	00h
00019Eh	Group 0 Time Measurement Control Register 6	G0TMCR6	00h
00019Fh	Group 0 Time Measurement Control Register 7	G0TMCR7	00h

X: Undefined

Blanks are reserved. No access is allowed.

Table 4.11 SFR List (11)

Address	Register	Symbol	Reset Value
000200h to 0002BFh			
0002C0h 0002C1h	X0 Register/Y0 Register	X0R/Y0R	XXXXh
0002C2h 0002C3h	X1 Register/Y1 Register	X1R/Y1R	XXXXh
0002C4h 0002C5h	X2 Register/Y2 Register	X2R/Y2R	XXXXh
0002C6h 0002C7h	X3 Register/Y3 Register	X3R/Y3R	XXXXh
0002C8h 0002C9h	X4 Register/Y4 Register	X4R/Y4R	XXXXh
0002CAh 0002CBh	X5 Register/Y5 Register	X5R/Y5R	XXXXh
0002CCh 0002CDh	X6 Register/Y6 Register	X6R/Y6R	XXXXh
0002CEh 0002CFh	X7 Register/Y7 Register	X7R/Y7R	XXXXh
0002D0h 0002D1h	X8 Register/Y8 Register	X8R/Y8R	XXXXh
0002D2h 0002D3h	X9 Register/Y9 Register	X9R/Y9R	XXXXh
0002D4h 0002D5h	X10 Register/Y10 Register	X10R/Y10R	XXXXh
0002D6h 0002D7h	X11 Register/Y11 Register	X11R/Y11R	XXXXh
0002D8h 0002D9h	X12 Register/Y12 Register	X12R/Y12R	XXXXh
0002DAh 0002DBh	X13 Register/Y13 Register	X13R/Y13R	XXXXh
0002DCh 0002DDh	X14 Register/Y14 Register	X14R/Y14R	XXXXh
0002DEh 0002DFh	X15 Register/Y15 Register	X15R/Y15R	XXXXh
0002E0h	X-Y Control Register	XYC	XXXX XX00b
0002E1h			
0002E2h			
0002E3h			
0002E4h	UART1 Special Mode Register 4	U1SMR4	00h
0002E5h	UART1 Special Mode Register 3	U1SMR3	00h
0002E6h	UART1 Special Mode Register 2	U1SMR2	00h
0002E7h	UART1 Special Mode Register	U1SMR	00h
0002E8h	UART1 Transmit/Receive Mode Register	U1MR	00h
0002E9h	UART1 Bit Rate Register	U1BRG	XXh
0002EAh 0002EBh	UART1 Transmit Buffer Register	U1TB	XXXXh
0002ECh	UART1 Transmit/Receive Control Register 0	U1C0	0000 1000b
0002EDh	UART1 Transmit/Receive Control Register 1	U1C1	0000 0010b
0002EEh 0002EFh	UART1 Receive Buffer Register	U1RB	XXXXh

X: Undefined

Blanks are reserved. No access is allowed.

Table 4.16 SFR List (16)

Address	Register	Symbol	Reset Value
0003B0h			
0003B1h			
0003B2h			
0003B3h			
0003B4h			
0003B5h			
0003B6h			
0003B7h			
0003B8h			
0003B9h			
0003BAh			
0003BBh			
0003BCh			
0003BDh			
0003BEh			
0003BFh			
0003C0h	Port P0 Register	P0	XXh
0003C1h	Port P1 Register	P1	XXh
0003C2h	Port P0 Direction Register	PD0	0000 0000b
0003C3h	Port P1 Direction Register	PD1	0000 0000b
0003C4h	Port P2 Register	P2	XXh
0003C5h	Port P3 Register	P3	XXh
0003C6h	Port P2 Direction Register	PD2	0000 0000b
0003C7h	Port P3 Direction Register	PD3	0000 0000b
0003C8h	Port P4 Register	P4	XXh
0003C9h	Port P5 Register	P5	XXh
0003CAh	Port P4 Direction Register	PD4	0000 0000b
0003CBh	Port P5 Direction Register	PD5	0000 0000b
0003CCh	Port P6 Register	P6	XXh
0003CDh	Port P7 Register	P7	XXh
0003CEh	Port P6 Direction Register	PD6	0000 0000b
0003CFh	Port P7 Direction Register	PD7	0000 0000b
0003D0h	Port P8 Register	P8	XXh
0003D1h	Port P9 Register	P9	XXh
0003D2h	Port P8 Direction Register	PD8	00X0 0000b
0003D3h	Port P9 Direction Register	PD9	0000 0000b
0003D4h	Port P10 Register	P10	XXh
0003D5h	Port P11 Register	P11	XXh
0003D6h	Port P10 Direction Register	PD10	0000 0000b
0003D7h	Port P11 Direction Register	PD11	XXX0 0000b
0003D8h	Port P12 Register	P12	XXh
0003D9h	Port P13 Register	P13	XXh
0003DAh	Port P12 Direction Register	PD12	0000 0000b
0003DBh	Port P13 Direction Register	PD13	0000 0000b
0003DCh	Port P14 Register	P14	XXh
0003DDh	Port P15 Register	P15	XXh
0003DEh	Port P14 Direction Register	PD14	X000 0000b
0003DFh	Port P15 Direction Register	PD15	0000 0000b

X: Undefined

Blanks are reserved. No access is allowed.

Table 4.25 SFR List (25)

Address	Register	Symbol	Reset Value
044090h to 0443FFh			
044400h	I ² C-bus Transmit/Receive Shift Register	I2CTRSR	XXh
044401h			
044402h	I ² C-bus Slave Address Register	I2CSAR	00h
044403h	I ² C-bus Control Register 0	I2CCR0	0000 0000b
044404h	I ² C-bus Clock Control Register	I2CCCR	0000 0000b
044405h	I ² C-bus START and STOP Conditions Control Register	I2CSSCR	0001 1010b
044406h	I ² C-bus Control Register 1	I2CCR1	0011 0000b
044407h	I ² C-bus Control Register 2	I2CCR2	0X00 0000b
044408h	I ² C-bus Status Register	I2CSR	0001 000Xb
044409h			
04440Ah			
04440Bh			
04440Ch			
04440Dh			
04440Eh			
04440Fh			
044410h	I ² C-bus Mode Register	I2CMR	XXXX 0000b
044411h			
044412h			
044413h			
044414h			
044415h			
044416h			
044417h			
044418h			
044419h			
04441Ah			
04441Bh			
04441Ch			
04441Dh			
04441Eh			
04441Fh			
044420h to 04FFFFh			

X: Undefined

Blanks are reserved. No access is allowed.

Table 5.3 Operating Conditions (2/5)
($V_{CC} = 3.0$ to 5.5 V, $V_{SS} = 0$ V, and $T_a = T_{opr}$, unless otherwise noted) ⁽¹⁾

Symbol	Characteristic		Value (2)			Unit
			Min.	Typ.	Max.	
C_{VDC}	Decoupling capacitance for voltage regulator	Inter-pin voltage: 1.5 V	2.4		10.0	μF

Notes:

1. The device is operationally guaranteed under these operating conditions.
2. This value should be met with due consideration to the following conditions: operating temperature, DC bias, aging, etc.

Table 5.7 Electrical Characteristics of RAM
($V_{CC} = 3.0$ to 5.5 V, $V_{SS} = 0$ V, and $T_a = T_{opr}$, unless otherwise noted)

Symbol	Characteristic	Measurement Condition	Value			Unit
			Min.	Typ.	Max.	
V_{RDR}	RAM data retention voltage	In stop mode	2.0			V

Table 5.8 Electrical Characteristics of Flash Memory
($V_{CC} = 3.0$ to 5.5 V, $V_{SS} = 0$ V, and $T_a = T_{opr}$, unless otherwise noted)

Symbol	Characteristic		Value			Unit
			Min.	Typ.	Max.	
—	Program/erase cycles (1)	Program area	1000			Cycles
		Data area	10000			Cycles
—	4-word program time	Program area		150	900	μ s
		Data area		300	1700	μ s
—	Lock bit program time	Program area		70	500	μ s
		Data area		140	1000	μ s
—	Block erasure time	4-Kbyte block		0.12	3.0	s
		32-Kbyte block		0.17	3.0	s
		64-Kbyte block		0.20	3.0	s
—	Data retention (2)	$T_a = 55^\circ\text{C}$ (3)	10			Years

Notes:

1. Program/erase definition

This value represents the number of erasures per block.

When the number of program/erase cycles is n, each block can be erased n times.

For example, if a 4-word write is performed in 512 different addresses in the 4-Kbyte block A and then the block is erased, this is counted as a single program/erase operation.

However, the same address cannot be written to more than once per erasure (overwrite disabled).

2. Data retention includes periods when no supply voltage is applied and no clock is provided.

3. Contact a Renesas Electronics sales office for data retention times other than the above condition.

Timing Requirements ($V_{CC} = 3.0$ to 5.5 V, $V_{SS} = 0$ V, and $T_a = T_{opr}$, unless otherwise noted)

Table 5.14 Flash Memory CPU Rewrite Mode Timing

Symbol	Characteristics	Value		Unit
		Min.	Max.	
t_{cR}	Read cycle time	200		ns
$t_{su(S-R)}$	Chip-select setup time before read	200		ns
$t_{h(R-S)}$	Chip-select hold time after read	0		ns
$t_{su(A-R)}$	Address setup time before read	200		ns
$t_{h(R-A)}$	Address hold time after read	0		ns
$t_{w(R)}$	Read pulse width	100		ns
t_{cW}	Write cycle time	200		ns
$t_{su(S-W)}$	Chip-select setup time before write	0		ns
$t_{h(W-S)}$	Chip-select hold time after write	30		ns
$t_{su(A-W)}$	Address setup time before write	0		ns
$t_{h(W-A)}$	Address hold time after write	30		ns
$t_{w(W)}$	Write pulse width	50		ns

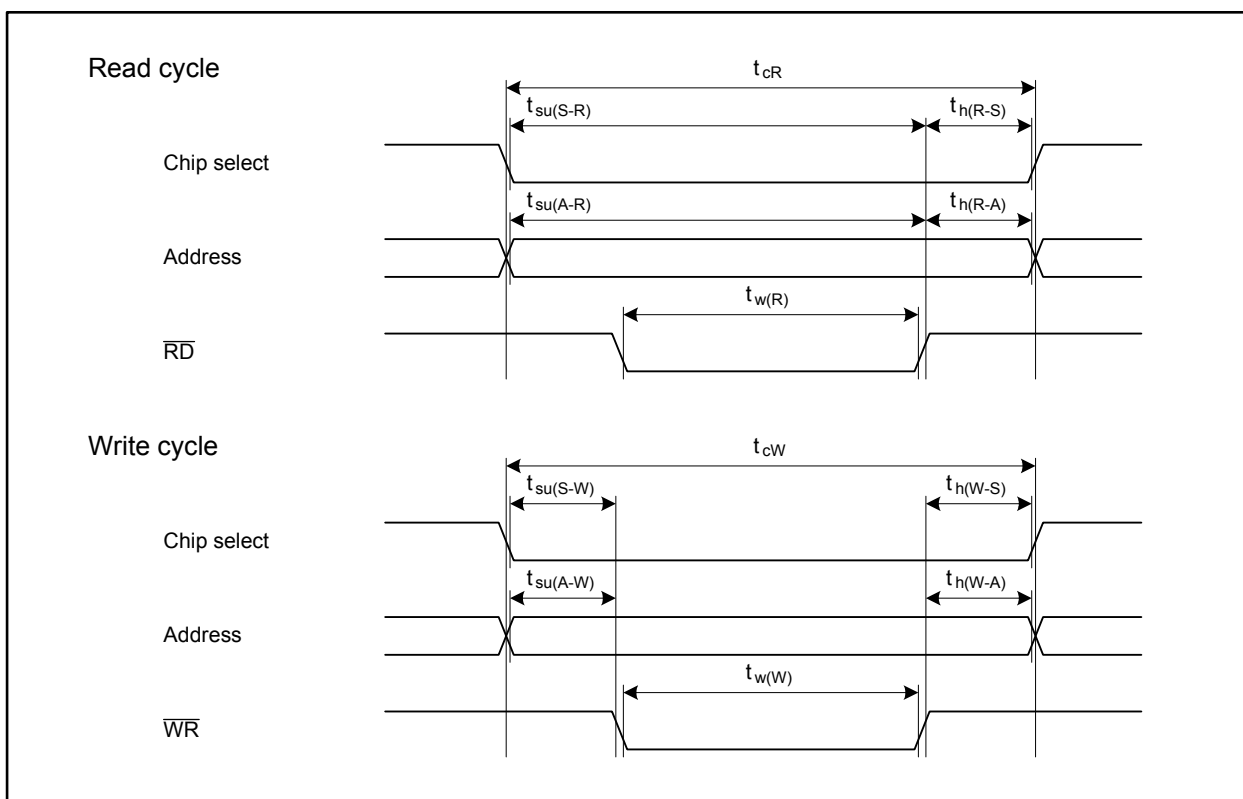


Figure 5.5 Flash Memory CPU Rewrite Mode Timing

$$V_{CC} = 5 \text{ V}$$

Switching Characteristics ($V_{CC} = 4.2$ to 5.5 V , $V_{SS} = 0 \text{ V}$, and $T_a = T_{opr}$, unless otherwise noted)

Table 5.35 External Bus Timing (separate bus)

Symbol	Characteristic	Measurement Condition	Value		Unit
			Min.	Max.	
$t_{su(S-R)}$	Chip-select setup time before read	Refer to Figure 5.6	(1)		ns
$t_{h(R-S)}$	Chip-select hold time after read		$t_{c(Base)} - 15$		ns
$t_{su(A-R)}$	Address setup time before read		(1)		ns
$t_{h(R-A)}$	Address hold time after read		$t_{c(Base)} - 15$		ns
$t_{w(R)}$	Read pulse width		(1)		ns
$t_{su(S-W)}$	Chip-select setup time before write		(1)		ns
$t_{h(W-S)}$	Chip-select hold time after write		$1.5 \times t_{c(Base)} - 15$		ns
$t_{su(A-W)}$	Address setup time before write		(1)		ns
$t_{h(W-A)}$	Address hold time after write		$1.5 \times t_{c(Base)} - 15$		ns
$t_{w(W)}$	Write pulse width		(1)		ns
$t_{su(D-W)}$	Data setup time before write		(1)		ns
$t_{h(W-D)}$	Data hold time after write		0		ns

Note:

1. The value is calculated using the formulas below based on the base clock cycles ($t_{c(Base)}$) and respective cycles of $T_{su(A-R)}$, $T_{w(R)}$, $T_{su(A-W)}$, and $T_{w(W)}$ set by registers EBC0 to EBC3. If the calculation results in a negative value, modify the value to be set. For details on how to set values, refer to the User's manual.

$$t_{su(S-R)} = t_{su(A-R)} = T_{su(A-R)} \times t_{c(Base)} - 15 \text{ [ns]}$$

$$t_{w(R)} = T_{w(R)} \times t_{c(Base)} - 10 \text{ [ns]}$$

$$t_{su(S-W)} = t_{su(A-W)} = T_{su(A-W)} \times t_{c(Base)} - 15 \text{ [ns]}$$

$$t_{w(W)} = t_{su(D-W)} = T_{w(W)} \times t_{c(Base)} - 10 \text{ [ns]}$$

$$V_{CC} = 3.3 \text{ V}$$

Table 5.41 Electrical Characteristics (1/3) ($V_{CC} = 3.0$ to 3.6 V , $V_{SS} = 0 \text{ V}$, $T_a = T_{opr}$, and $f_{(CPU)} = 64 \text{ MHz}$, unless otherwise noted)

Symbol	Characteristic		Measurement Condition	Value			Unit
				Min.	Typ.	Max.	
V_{OH}	High level output voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7, P14_3 to P14_6, P15_0 to P15_7 ⁽¹⁾	$I_{OH} = -1 \text{ mA}$	$V_{CC} - 0.6$		V_{CC}	V
V_{OL}	Low level output voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7, P14_3 to P14_6, P15_0 to P15_7 ⁽¹⁾	$I_{OL} = 1 \text{ mA}$			0.5	V

Note:

1. Ports P9_0, P9_2, and P11 to P15 are available in the 144-pin package only. Port P9_1 is designated as input pin in the 100-pin package.

$$V_{CC} = 3.3 \text{ V}$$

Table 5.42 Electrical Characteristics (2/3) ($V_{CC} = 3.0$ to 3.6 V , $V_{SS} = 0 \text{ V}$, $T_a = T_{opr}$, and $f_{CPU} = 64 \text{ MHz}$, unless otherwise noted)

Symbol	Characteristic	Measurement Condition	Value			Unit
			Min.	Typ.	Max.	
$V_{T+} - V_{T-}$	Hysteresis	HOLD, RDY, NMI, INT0 to INT8, KI0 to KI3, TA0IN to TA4IN, TA0OUT to TA4OUT, TB0IN to TB5IN, CTS0 to CTS8, CLK0 to CLK8, RXD0 to RXD8, SCL0 to SCL6, SDA0 to SDA6, SS0 to SS6, SRXD0 to SRXD6, ADTRG, IIO0_0 to IIO0_7, IIO1_0 to IIO1_7, UD0A, UD0B, UD1A, UD1B, ISCLK2, ISRXD2, IEIN, MSCL, MSDA ⁽¹⁾	0.2		1.0	V
		RESET	0.2		1.8	V
I_{IH}	High level input current	XIN, RESET, CNVSS, NSD, P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7, P14_1, P14_3 to P14_6, P15_0 to P15_7 ⁽²⁾	$V_I = 3.3 \text{ V}$			4.0 μA
I_{IL}	Low level input current	XIN, RESET, CNVSS, NSD, P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7, P14_1, P14_3 to P14_6, P15_0 to P15_7 ⁽²⁾	$V_I = 0 \text{ V}$			-4.0 μA
R_{PULLUP}	Pull-up resistor	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P5_0 to P5_3, P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7, P14_1, P14_3 to P14_6, P15_0 to P15_7 ⁽²⁾	$V_I = 0 \text{ V}$			50 100 500 $k\Omega$
R_{fXIN}	Feedback resistor	XIN		3		$M\Omega$
R_{fXCIN}	Feedback resistor	XCIN		25		$M\Omega$

Notes:

1. Pins INT6 to INT8 are available in the 144-pin package only.
2. Ports P9_0, P9_2, and P11 to P15 are available in the 144-pin package only. Port P9_1 is designated as input pin in the 100-pin package.

$$V_{CC} = 3.3 \text{ V}$$

Timing Requirements ($V_{CC} = 3.0$ to 3.6 V , $V_{SS} = 0 \text{ V}$, and $T_a = T_{opr}$, unless otherwise noted)

Table 5.56 Serial Interface

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{C(CK)}$	CLKi input clock cycle time	200		ns
$t_{W(CKH)}$	CLKi input high level pulse width	80		ns
$t_{W(CKL)}$	CLKi input low level pulse width	80		ns
$t_{su(D-C)}$	RXDi input setup time	80		ns
$t_{h(C-D)}$	RXDi input hold time	90		ns

Table 5.57 A/D Trigger Input

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{W(ADH)}$	ADTRG input high level pulse width Hardware trigger input high level pulse width	$\frac{3}{\phi_{AD}}$		ns
$t_{W(ADL)}$	ADTRG input low level pulse width Hardware trigger input high level pulse width	125		ns

Table 5.58 External Interrupt $\overline{INTi}$ Input

Symbol	Characteristic		Value		Unit
			Min.	Max.	
$t_{W(INH)}$	$\overline{INTi}$ input high level pulse width	Edge sensitive	250		ns
		Level sensitive	$t_{C(CPU)} + 200$		ns
$t_{W(INL)}$	$\overline{INTi}$ input low level pulse width	Edge sensitive	250		ns
		Level sensitive	$t_{C(CPU)} + 200$		ns

Table 5.59 Intelligent I/O

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{C(ISCLK2)}$	ISCLK2 input clock cycle time	600		ns
$t_{W(ISCLK2H)}$	ISCLK2 input high level pulse width	270		ns
$t_{W(ISCLK2L)}$	ISCLK2 input low level pulse width	270		ns
$t_{su(RXD-ISCLK2)}$	ISRXD2 input setup time	150		ns
$t_{h(ISCLK2-RXD)}$	ISRXD2 input hold time	100		ns

Appendix 1. Package Dimensions

