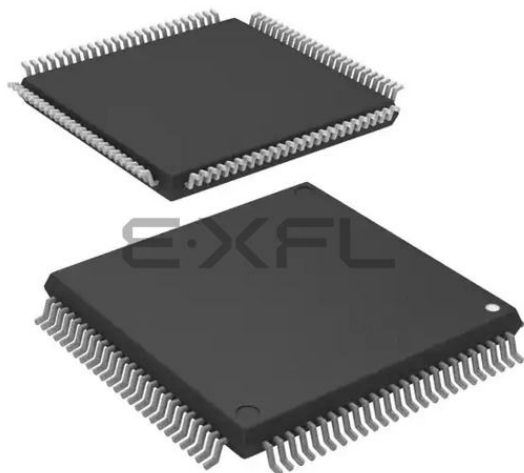




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Details

Product Status	Active
Core Processor	R32C/100
Core Size	16/32-Bit
Speed	50MHz
Connectivity	EBI/EMI, I ² C, IEBus, UART/USART
Peripherals	DMA, LVD, PWM, WDT
Number of I/O	84
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	63K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 26x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f64169dfb-ub

1.2 Product Information

Tables 1.5 and 1.6 list the product information and Figure 1.1 shows the details of the part number.

Table 1.5 R32C/116 Group Product List for Normal Speed Version (1/2) As of February, 2013

Part Number	Package Code (1)	ROM Capacity (2)	RAM Capacity	Remarks
R5F64165NFD (P)	PLQP0144KA-A	384 Kbytes + 8 Kbytes	40 Kbytes	-20°C to 85°C (N version)
R5F64165DFD				-40°C to 85°C (D version)
R5F64165PFD				-40°C to 85°C (P version)
R5F64165NFB (P)	PLQP0100KB-A			-20°C to 85°C (N version)
R5F64165DFB				-40°C to 85°C (D version)
R5F64165PFB				-40°C to 85°C (P version)
R5F64166NFD (P)	PLQP0144KA-A	512 Kbytes + 8 Kbytes	40 Kbytes	-20°C to 85°C (N version)
R5F64166DFD				-40°C to 85°C (D version)
R5F64166PFD				-40°C to 85°C (P version)
R5F64166NFB (P)	PLQP0100KB-A			-20°C to 85°C (N version)
R5F64166DFB				-40°C to 85°C (D version)
R5F64166PFB				-40°C to 85°C (P version)
R5F64167NFD (P)	PLQP0144KA-A	640 Kbytes + 8 Kbytes	48 Kbytes	-20°C to 85°C (N version)
R5F64167DFD				-40°C to 85°C (D version)
R5F64167PFD				-40°C to 85°C (P version)
R5F64167NFB (P)	PLQP0100KB-A			-20°C to 85°C (N version)
R5F64167DFB				-40°C to 85°C (D version)
R5F64167PFB				-40°C to 85°C (P version)
R5F64168NFD (P)	PLQP0144KA-A	768 Kbytes + 8 Kbytes	63 Kbytes	-20°C to 85°C (N version)
R5F64168DFD				-40°C to 85°C (D version)
R5F64168PFD				-40°C to 85°C (P version)
R5F64168NFB (P)	PLQP0100KB-A			-20°C to 85°C (N version)
R5F64168DFB				-40°C to 85°C (D version)
R5F64168PFB				-40°C to 85°C (P version)
R5F64169NFD (P)	PLQP0144KA-A	1 Mbyte + 8 Kbytes	63 Kbytes	-20°C to 85°C (N version)
R5F64169DFD				-40°C to 85°C (D version)
R5F64169PFD				-40°C to 85°C (P version)
R5F64169NFB (P)	PLQP0100KB-A			-20°C to 85°C (N version)
R5F64169DFB				-40°C to 85°C (D version)
R5F64169PFB				-40°C to 85°C (P version)

(P): On planning phase

Notes:

- The old package codes are as follows:
PLQP0100KB-A: 100P6Q-A; PLQP0144KA-A: 144P6Q-A
- "8 Kbytes" in the ROM capacity indicates the data flash memory capacity.

1.4 Pin Assignments

Figures 1.3 and 1.4 show the pin assignments (top view) and Tables 1.7 to 1.13 list the pin characteristics.

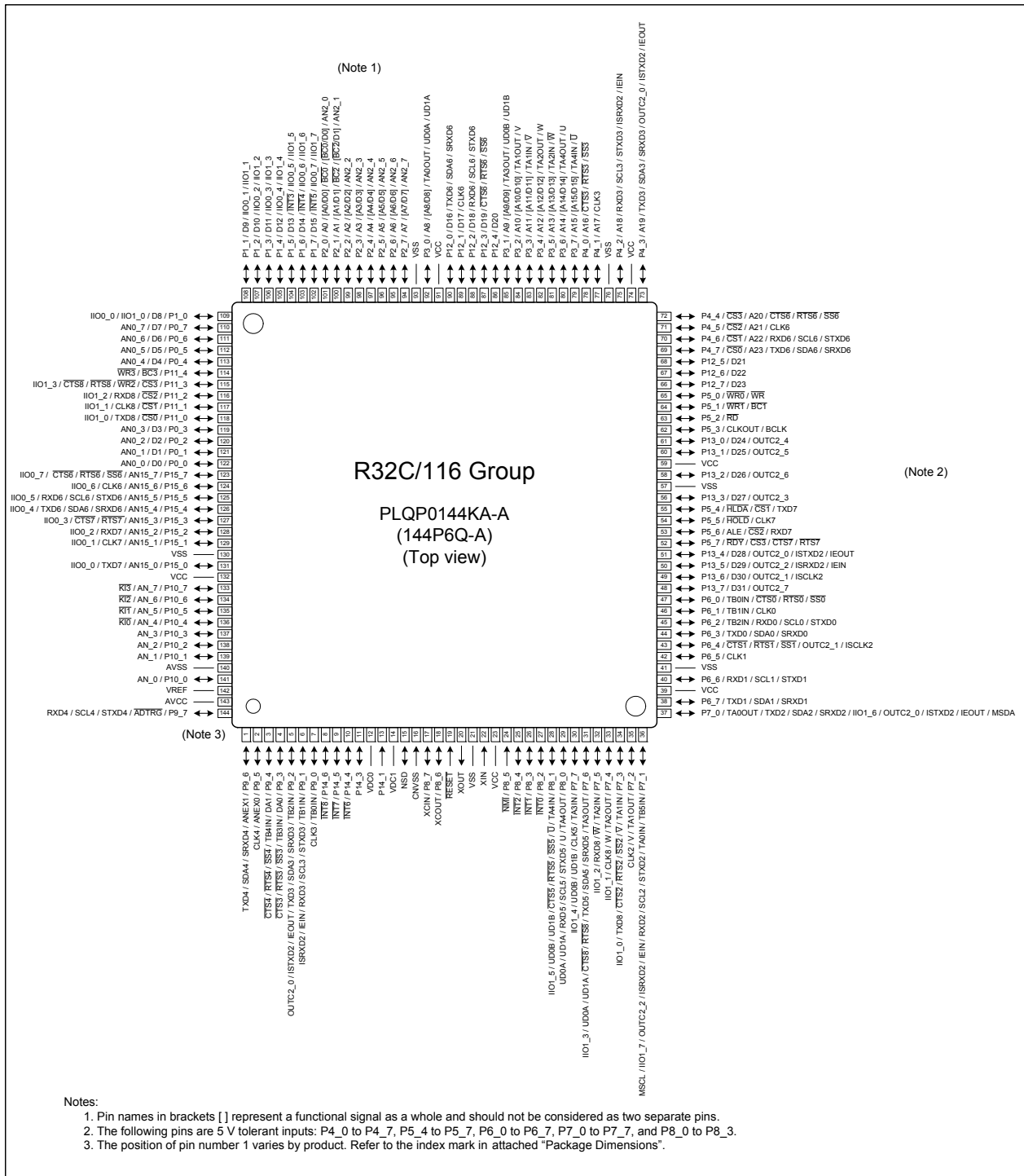


Figure 1.3 Pin Assignment for the 144-pin Package (top view)

Table 1.9 Pin Characteristics for the 144-pin Package (3/4)

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	UART Pin	Intelligent I/O Pin	Analog Pin	Bus Control Pin
75		P4_2			RXD3/SCL3/STXD3	ISRXD2/IEIN		A18
76	VSS							
77		P4_1			CLK3			A17
78		P4_0			CTS3/RTS3/SS3			A16
79		P3_7		TA4IN/U				A15(/D15)
80		P3_6		TA4OUT/U				A14(/D14)
81		P3_5		TA2IN/W				A13(/D13)
82		P3_4		TA2OUT/W				A12(/D12)
83		P3_3		TA1IN/V				A11(/D11)
84		P3_2		TA1OUT/V				A10(/D10)
85		P3_1		TA3OUT		UD0B/UD1B		A9(/D9)
86		P12_4						D20
87		P12_3			CTS6/RTS6/SS6			D19
88		P12_2			RXD6/SCL6/STXD6			D18
89		P12_1			CLK6			D17
90		P12_0			TXD6/SDA6/SRXD6			D16
91	VCC							
92		P3_0		TA0OUT		UD0A/UD1A		A8(/D8)
93	VSS							
94		P2_7					AN2_7	A7(/D7)
95		P2_6					AN2_6	A6(/D6)
96		P2_5					AN2_5	A5(/D5)
97		P2_4					AN2_4	A4(/D4)
98		P2_3					AN2_3	A3(/D3)
99		P2_2					AN2_2	A2(/D2)
100		P2_1					AN2_1	A1(/D1)/ BC2(/D1)
101		P2_0					AN2_0	A0(/D0)/ BC0(/D0)
102		P1_7	INT5			IIO0_7/IIO1_7		D15
103		P1_6	INT4			IIO0_6/IIO1_6		D14
104		P1_5	INT3			IIO0_5/IIO1_5		D13
105		P1_4				IIO0_4/IIO1_4		D12
106		P1_3				IIO0_3/IIO1_3		D11
107		P1_2				IIO0_2/IIO1_2		D10
108		P1_1				IIO0_1/IIO1_1		D9
109		P1_0				IIO0_0/IIO1_0		D8
110		P0_7					AN0_7	D7
111		P0_6					AN0_6	D6
112		P0_5					AN0_5	D5
113		P0_4					AN0_4	D4
114		P11_4						BC3/WR3

Table 1.10 Pin Characteristics for the 144-pin Package (4/4)

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	UART Pin	Intelligent I/O Pin	Analog Pin	Bus Control Pin
115		P11_3			CTS8/RTS8	IIO1_3		CS3/WR2
116		P11_2			RXD8	IIO1_2		CS2
117		P11_1			CLK8	IIO1_1		CS1
118		P11_0			TXD8	IIO1_0		CS0
119		P0_3					AN0_3	D3
120		P0_2					AN0_2	D2
121		P0_1					AN0_1	D1
122		P0_0					AN0_0	D0
123		P15_7			CTS6/RTS6/SS6	IIO0_7	AN15_7	
124		P15_6			CLK6	IIO0_6	AN15_6	
125		P15_5			RXD6/SCL6/STXD6	IIO0_5	AN15_5	
126		P15_4			TXD6/SDA6/SRXD6	IIO0_4	AN15_4	
127		P15_3			CTS7/RTS7	IIO0_3	AN15_3	
128		P15_2			RXD7	IIO0_2	AN15_2	
129		P15_1			CLK7	IIO0_1	AN15_1	
130	VSS							
131		P15_0			TXD7	IIO0_0	AN15_0	
132	VCC							
133		P10_7	KI3				AN_7	
134		P10_6	KI2				AN_6	
135		P10_5	KI1				AN_5	
136		P10_4	KI0				AN_4	
137		P10_3					AN_3	
138		P10_2					AN_2	
139		P10_1					AN_1	
140	AVSS							
141		P10_0					AN_0	
142	VREF							
143	AVCC							
144		P9_7			RXD4/SCL4/STXD4		ADTRG	

Table 1.12 Pin Characteristics for the 100-pin Package (2/3)

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	UART Pin	Intelligent I/O Pin	Analog Pin	Bus Control Pin
39		P5_5			CLK7			HOLD
40		P5_4			TXD7			HLDA/CS1
41		P5_3						CLKOUT/ BCLK
42		P5_2						RD
43		P5_1						WR1/BC1
44		P5_0						WR0/WR
45		P4_7			TXD6/SDA6/SRXD6			CS0/A23
46		P4_6			RXD6/SCL6/STXD6			CS1/A22
47		P4_5			CLK6			CS2/A21
48		P4_4			CTS6/RTS6/SS6			CS3/A20
49		P4_3			TXD3/SDA3/SRXD3	OUTC2_0/ISTXD2/ IEOUT		A19
50		P4_2			RXD3/SCL3/STXD3	ISRXD2/IEIN		A18
51		P4_1			CLK3			A17
52		P4_0			CTS3/RTS3/SS3			A16
53		P3_7		TA4IN/U				A15/(D15)
54		P3_6		TA4OUT/U				A14/(D14)
55		P3_5		TA2IN/W				A13/(D13)
56		P3_4		TA2OUT/W				A12/(D12)
57		P3_3		TA1IN/V				A11/(D11)
58		P3_2		TA1OUT/V				A10/(D10)
59		P3_1		TA3OUT		UD0B/UD1B		A9/(D9)
60	VCC							
61		P3_0		TA0OUT		UD0A/UD1A		A8/(D8)
62	VSS							
63		P2_7					AN2_7	A7/(D7)
64		P2_6					AN2_6	A6/(D6)
65		P2_5					AN2_5	A5/(D5)
66		P2_4					AN2_4	A4/(D4)
67		P2_3					AN2_3	A3/(D3)
68		P2_2					AN2_2	A2/(D2)
69		P2_1					AN2_1	A1/(D1)
70		P2_0					AN2_0	A0/(D0)/ BC0/(D0)
71		P1_7	INT5			IIO0_7/IIO1_7		D15
72		P1_6	INT4			IIO0_6/IIO1_6		D14
73		P1_5	INT3			IIO0_5/IIO1_5		D13
74		P1_4				IIO0_4/IIO1_4		D12
75		P1_3				IIO0_3/IIO1_3		D11

1.5 Pin Definitions and Functions

Tables 1.14 to 1.18 list the pin definitions and functions.

Table 1.14 Pin Definitions and Functions (1/4)

Function	Symbol	I/O	Description
Power supply	VCC, VSS	I	Applicable as follows: VCC = 3.0 to 5.5 V, VSS = 0 V
Connecting pins for decoupling capacitor	VDC0, VDC1	—	A decoupling capacitor for internal voltage should be connected between VDC0 and VDC1
Analog power supply	AVCC, AVSS	I	Power supply for the A/D converter. AVCC and AVSS should be connected to VCC and VSS, respectively
Reset input	$\overline{\text{RESET}}$	I	The MCU is reset when this pin is driven low
CNVSS	CNVSS	I	This pin should be connected to VSS via a resistor
Debug port	NSD	I/O	This pin is to communicate with a debugger. It should be connected to VCC via a resistor of 1 to 4.7 k Ω
Main clock input	XIN	I	Input/output for the main clock oscillator. A crystal, or a ceramic resonator should be connected between pins XIN and XOUT. An external clock should be input at the XIN while leaving the XOUT open
Main clock output	XOUT	O	
Sub clock input	XCIN	I	Input/output for the sub clock oscillator. A crystal oscillator should be connected between pins XCIN and XCOU. An external clock should be input at the XCIN while leaving the XCOU open
Sub clock output	XCOU	O	
BCLK output	BCLK	O	BCLK output
Clock output	CLKOUT	O	Output of the clock with the same frequency as low speed clocks, f8, or f32
External interrupt input	$\overline{\text{INT0}}$ to $\overline{\text{INT8}}$ ⁽¹⁾	I	Input for external interrupts
NMI input	P8_5/ $\overline{\text{NMI}}$	I	Input for NMI
Key input interrupt	KI0 to KI3	I	Input for the key input interrupt
Bus control pins	D0 to D7	I/O	Input/output of data (D0 to D7) while accessing an external memory space with a separate bus
	D8 to D15	I/O	Input/output of data (D8 to D15) while accessing an external memory space with 16-bit or 32-bit separate bus
	D16 to D31 ⁽²⁾	I/O	Input/output of data (D16 to D31) while accessing an external memory space with 32-bit separate bus
	A0 to A23	O	Output of address bits A0 to A23
	A0/D0 to A7/D7	I/O	Output of address bits (A0 to A7) and input/output of data (D0 to D7) by time-division while accessing an external memory space with multiplexed bus
	A8/D8 to A15/D15	I/O	Output of address bits (A8 to A15) and input/output of data (D8 to D15) by time-division while accessing an external memory space with 16-bit or 32-bit multiplexed bus

Notes:

1. Pins $\overline{\text{INT6}}$ to $\overline{\text{INT8}}$ are available in the 144-pin package only.
2. Pins D16 to D31 are available in the 144-pin package only.

Table 1.17 Pin Definitions and Functions (4/4)

Function	Symbol	I/O	Description
A/D converter	AN_0 to AN_7, AN0_0 to AN0_7, AN2_0 to AN2_7, AN15_0 to AN15_7 (1)	I	Analog input for the A/D converter
	ADTRG	I	External trigger input for the A/D converter
	ANEX0	I/O	Expanded analog input for the A/D converter and output in external op-amp connection mode
	ANEX1	I	Expanded analog input for the A/D converter
D/A converter	DA0, DA1	O	Output for the D/A converter
Reference voltage input	VREF	I	Reference voltage input for the A/D converter and D/A converter
Intelligent I/O	IIO0_0 to IIO0_7	I/O	Input/output for Intelligent I/O group 0. Either input capture or output compare is selectable
	IIO1_0 to IIO1_7	I/O	Input/output for Intelligent I/O group 1. Either input capture or output compare is selectable
	UD0A, UD0B, UD1A, UD1B	I	Input for the two-phase encoder
	OUTC2_0 to OUTC2_7 (2)	O	Output for OC (output compare) of Intelligent I/O group 2
	ISCLK2	I/O	Clock input/output for the serial interface
	ISRXD2	I	Receive data input for the serial interface
	ISTXD2	O	Transmit data output for the serial interface
	IEIN	I	Receive data input for the serial interface
	IEOUT	O	Transmit data output for the serial interface
Multi-master I ² C-bus	MSDA	I/O	Serial data input/output
	MSCL	I/O	Transmit/receive clock input/output

Notes:

1. Pins AN15_0 to AN15_7 are available in the 144-pin package only.
2. Pins OUTC2_3 to OUTC2_7 are available in the 144-pin package only.

3. Memory

Figure 3.1 shows the memory map of the R32C/116 Group.

The R32C/116 Group provides a 4-Gbyte address space from 00000000h to FFFFFFFFh.

The internal ROM is mapped from address FFFFFFFFh in the inferior direction. For example, the 1-Mbyte internal ROM is mapped from FFF00000h to FFFFFFFFh.

The fixed interrupt vector table contains the start address of interrupt handlers and is mapped from FFFFFFFDCh to FFFFFFFFh.

The internal RAM is mapped from address 00000400h in the superior direction. For example, the 63-Kbyte internal RAM is mapped from 00000400h to 0000FFFFh. Besides being used for data storage, the internal RAM functions as a stack(s) for subroutine calls and/or interrupt handlers.

Special function registers (SFRs), which are control registers for peripheral functions, are mapped from 00000000h to 000003FFh, and from 00040000h to 0004FFFFh. Unoccupied SFR locations are reserved, and no access is allowed.

In memory expansion mode or microprocessor mode, some spaces are reserved for internal use and should not be accessed.

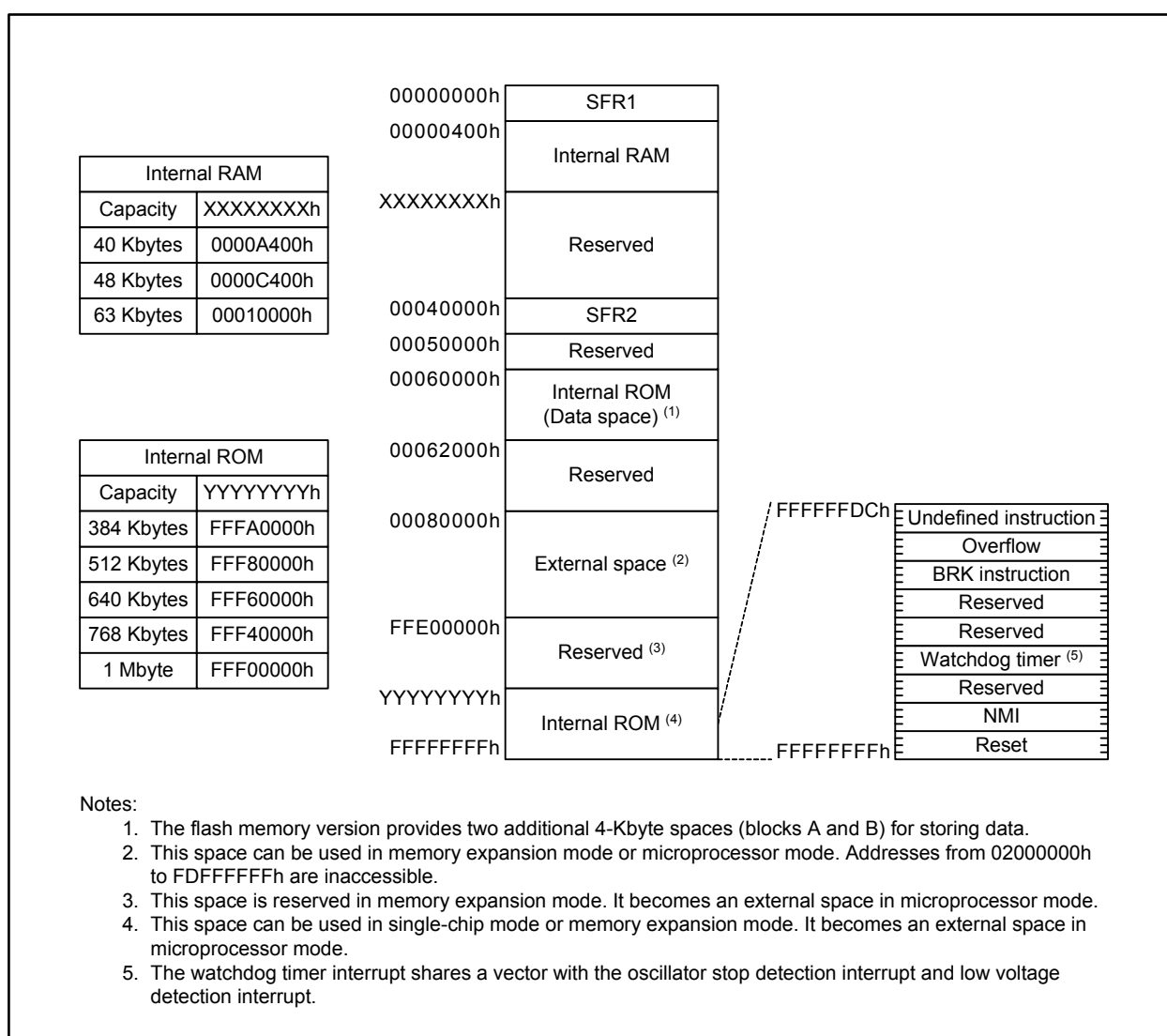


Figure 3.1 Memory Map

Table 4.15 SFR List (15)

Address	Register	Symbol	Reset Value
000380h	A/D0 Register 0	AD00	00XXh
000381h			
000382h	A/D0 Register 1	AD01	00XXh
000383h			
000384h	A/D0 Register 2	AD02	00XXh
000385h			
000386h	A/D0 Register 3	AD03	00XXh
000387h			
000388h	A/D0 Register 4	AD04	00XXh
000389h			
00038Ah	A/D0 Register 5	AD05	00XXh
00038Bh			
00038Ch	A/D0 Register 6	AD06	00XXh
00038Dh			
00038Eh	A/D0 Register 7	AD07	00XXh
00038Fh			
000390h			
000391h			
000392h	A/D0 Control Register 4	AD0CON4	XXXX 00XXb
000393h			
000394h	A/D0 Control Register 2	AD0CON2	XX0X X000b
000395h	A/D0 Control Register 3	AD0CON3	XXXX X000b
000396h	A/D0 Control Register 0	AD0CON0	00h
000397h	A/D0 Control Register 1	AD0CON1	00h
000398h	D/A Register 0	DA0	XXh
000399h			
00039Ah	D/A Register 1	DA1	XXh
00039Bh			
00039Ch	D/A Control Register	DACON	XXXX XX00b
00039Dh			
00039Eh			
00039Fh			
0003A0h			
0003A1h			
0003A2h			
0003A3h			
0003A4h			
0003A5h			
0003A6h			
0003A7h			
0003A8h			
0003A9h			
0003AAh			
0003ABh			
0003ACh			
0003ADh			
0003AEh			
0003AFh			

X: Undefined

Blanks are reserved. No access is allowed.

Table 4.18 SFR List (18)

Address	Register	Symbol	Reset Value
040000h	Flash Memory Control Register 0	FMR0	0X01 XX00b
040001h	Flash Memory Status Register 0	FMSR0	1000 0000b
040002h			
040003h			
040004h			
040005h			
040006h			
040007h			
040008h	Flash Register Protection Unlock Register 0	FPR0	00h
040009h	Flash Memory Control Register 1	FMR1	0000 0010b
04000Ah	Block Protect Bit Monitor Register 0	FBPM0	??X? ???b (1)
04000Bh	Block Protect Bit Monitor Register 1	FBPM1	XXX? ???b (1)
04000Ch			
04000Dh			
04000Eh			
04000Fh			
040010h			
040011h	Block Protect Bit Monitor Register 2	FBPM2	???? ???b (1)
040012h			
040013h			
040014h			
040015h			
040016h			
040017h			
040018h			
040019h			
04001Ah			
04001Bh			
04001Ch			
04001Dh			
04001Eh			
04001Fh			
040020h	PLL Control Register 0	PLC0	0000 0001b
040021h	PLL Control Register 1	PLC1	0001 1111b
040022h			
040023h			
040024h			
040025h			
040026h			
040027h			
040028h			
040029h			
04002Ah			
04002Bh			
04002Ch			
04002Dh			
04002Eh			
04002Fh			

X: Undefined

Blanks are reserved. No access is allowed.

Note:

1. The reset value reflects the value of the protect bit for each block in the flash memory.

Table 5.5 Operating Conditions (4/5)
($V_{CC} = 3.0$ to 5.5 V, $V_{SS} = 0$ V, and $T_a = T_{opr}$, unless otherwise noted) ⁽¹⁾

Symbol	Characteristic		Value			Unit
			Min.	Typ.	Max.	
$f_{(XIN)}$	Main clock oscillator frequency		4		16	MHz
$f_{(XRef)}$	Reference clock frequency		2		4	MHz
$f_{(PLL)}$	PLL clock oscillator frequency		96		128	MHz
$f_{(Base)}$	Base clock frequency	High speed version			64	MHz
		Normal speed version			50	MHz
$t_{c(Base)}$	Base clock cycle time	High speed version	15.625			ns
		Normal speed version	20			ns
$f_{(CPU)}$	CPU operating frequency	High speed version			64	MHz
		Normal speed version			50	MHz
$t_{c(CPU)}$	CPU clock cycle time	High speed version	15.625			ns
		Normal speed version	20			ns
$f_{(BCLK)}$	Peripheral bus clock operating frequency	High speed version			32	MHz
		Normal speed version			25	MHz
$t_{c(BCLK)}$	Peripheral bus clock cycle time	High speed version	31.25			ns
		Normal speed version	40			ns
$f_{(PER)}$	Peripheral clock source frequency				32	MHz
$f_{(XCIN)}$	Sub clock oscillator frequency			32.768	62.5	kHz

Note:

1. The device is operationally guaranteed under these operating conditions.

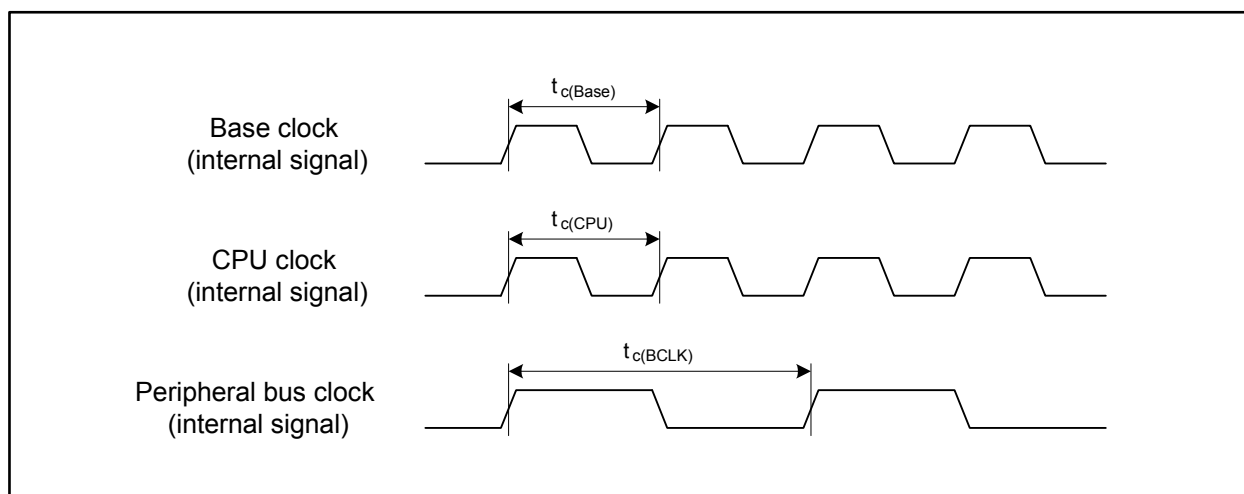


Figure 5.1 Clock Cycle Time

Table 5.12 Electrical Characteristics of Oscillator
($V_{CC} = 3.0$ to 5.5 V, $V_{SS} = 0$ V, and $T_a = T_{opr}$, unless otherwise noted)

Symbol	Characteristics	Measurement Condition	Value			Unit
			Min.	Typ.	Max.	
$f_{SO(PLL)}$	PLL clock self-oscillation frequency		35	50	65	MHz
$t_{LOCK(PLL)}$	PLL lock time ⁽¹⁾				1	ms
$t_{jitter(p-p)}$	PLL jitter period (p-p)				2.0	ns
$f_{(OCO)}$	On-chip oscillator frequency		62.5	125	250	kHz

Note:

1. This value is applicable only when the main clock oscillation is stable.

Table 5.13 Electrical Characteristics of Clock Circuitry
($V_{CC} = 3.0$ to 5.5 V, $V_{SS} = 0$ V, and $T_a = T_{opr}$, unless otherwise noted)

Symbol	Characteristics	Measurement Condition	Value			Unit
			Min.	Typ.	Max.	
$t_{rec(WAIT)}$	Recovery time from wait mode to low power mode				225	μ s
$t_{rec(STOP)}$	Recovery time from stop mode ⁽¹⁾				225	μ s

Note:

1. The recovery time from stop mode does not include the main clock oscillation stabilization time. The CPU starts operating before the oscillator is stabilized.

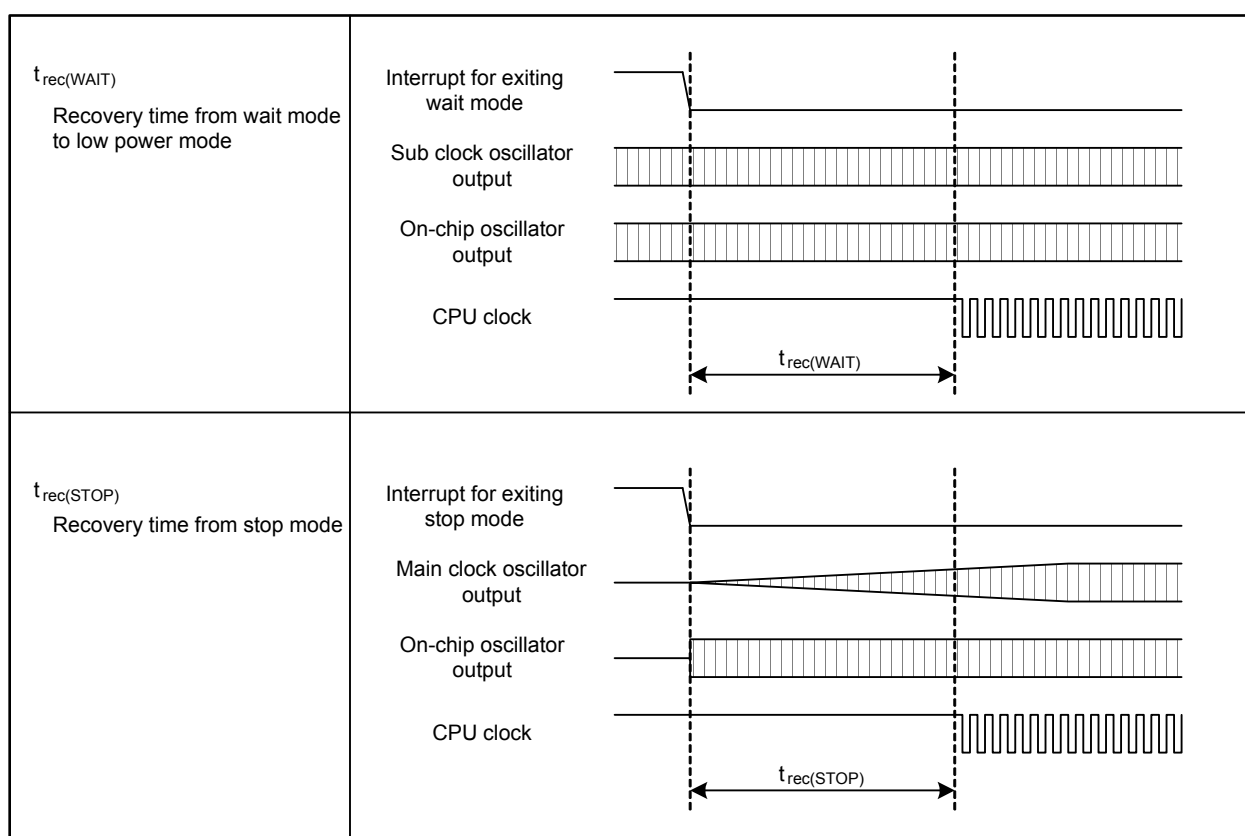


Figure 5.4 Clock Circuit Timing

$$V_{CC} = 5 \text{ V}$$

Table 5.15 Electrical Characteristics (1/3)

($V_{CC} = 4.2$ to 5.5 V , $V_{SS} = 0 \text{ V}$, $T_a = T_{opr}$, and $f_{(CPU)} = 64 \text{ MHz}$, unless otherwise noted)

Symbol	Characteristic		Measurement Condition	Value			Unit
				Min.	Typ.	Max.	
V_{OH}	High level output voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7, P14_3 to P14_6, P15_0 to P15_7 (1)	$I_{OH} = -5 \text{ mA}$	$V_{CC} - 2.0$		V_{CC}	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7, P14_3 to P14_6, P15_0 to P15_7 (1)	$I_{OH} = -200 \mu\text{A}$	$V_{CC} - 0.3$		V_{CC}	V
V_{OL}	Low level output voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7, P14_3 to P14_6, P15_0 to P15_7 (1)	$I_{OL} = 5 \text{ mA}$			2.0	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7, P14_3 to P14_6, P15_0 to P15_7 (1)	$I_{OL} = 200 \mu\text{A}$			0.45	V

Note:

- Ports P9_0, P9_2, and P11 to P15 are available in the 144-pin package only. Port P9_1 is designated as input pin in the 100-pin package.

$$V_{CC} = 5\text{ V}$$

Table 5.17 Electrical Characteristics (3/3)**($V_{CC} = 4.2$ to 5.5 V , $V_{SS} = 0\text{ V}$, and $T_a = T_{opr}$, unless otherwise noted)**

Symbol	Characteristic	Measurement Condition	Value			Unit
			Min.	Typ.	Max.	
I_{CC}	Power supply current	In single-chip mode, output pins are left open and others are connected to V_{SS}		45	60	mA
		XIN-XOUT Drive strength: low		35	50	mA
		XCIN-XCOUT Drive strength: low		12		mA
				1.2		mA
				220		μA
				230		μA
				960	1600	μA
				8	140	μA
				10	150	μA
		Stopped: all clocks, Main regulator: shutdown, $T_a = 25^\circ\text{C}$		5	70	μA

$$V_{CC} = 5 \text{ V}$$

Table 5.18 A/D Conversion Characteristics ($V_{CC} = AV_{CC} = V_{REF} = 4.2 \text{ to } 5.5 \text{ V}$, $V_{SS} = AV_{SS} = 0 \text{ V}$, $T_a = T_{opr}$, and $f_{(BCLK)} = 32 \text{ MHz}$, unless otherwise noted)

Symbol	Characteristic	Measurement Condition	Value			Unit
			Min.	Typ.	Max.	
—	Resolution	$V_{REF} = V_{CC}$			10	Bits
—	Absolute error	$V_{REF} = V_{CC} = 5 \text{ V}$			± 3	LSB
		AN_0 to AN_7, AN0_0 to AN0_7, AN2_0 to AN2_7, AN15_0 to AN15_7, ANEX0, ANEX1 ⁽¹⁾ External op-amp connection mode			± 7	LSB
INL	Integral non-linearity error	$V_{REF} = V_{CC} = 5 \text{ V}$			± 3	LSB
		AN_0 to AN_7, AN0_0 to AN0_7, AN2_0 to AN2_7, AN15_0 to AN15_7, ANEX0, ANEX1 ⁽¹⁾ External op-amp connection mode			± 7	LSB
DNL	Differential non-linearity error				± 1	LSB
—	Offset error				± 3	LSB
—	Gain error				± 3	LSB
R _{LADDER}	Resistor ladder	$V_{REF} = V_{CC}$	4		20	k Ω
t _{CONV}	Conversion time (10 bits)	$\phi_{AD} = 16 \text{ MHz}$, with sample and hold function	2.06			μs
		$\phi_{AD} = 16 \text{ MHz}$, without sample and hold function	3.69			μs
t _{CONV}	Conversion time (8 bits)	$\phi_{AD} = 16 \text{ MHz}$, with sample and hold function	1.75			μs
		$\phi_{AD} = 16 \text{ MHz}$, without sample and hold function	3.06			μs
t _{SAMP}	Sampling time	$\phi_{AD} = 16 \text{ MHz}$	0.188			μs
V _{IA}	Analog input voltage		0		V _{REF}	V
ϕ_{AD}	Operating clock frequency	Without sample and hold function	0.25		16	MHz
		With sample and hold function	1		16	MHz

Note:

1. Pins AN15_0 to AN15_7 are available in the 144-pin package only.

$$V_{CC} = 5\text{ V}$$

Timing Requirements ($V_{CC} = 4.2$ to 5.5 V , $V_{SS} = 0\text{ V}$, and $T_a = T_{opr}$, unless otherwise noted)

Table 5.20 External Clock Input

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{C(X)}$	External clock input period	62.5	250	ns
$t_{W(XH)}$	External clock input high level pulse width	25		ns
$t_{W(XL)}$	External clock input low level pulse width	25		ns
$t_{r(X)}$	External clock input rise time		5	ns
$t_{f(X)}$	External clock input fall time		5	ns
t_W / t_C	External clock input duty	40	60	%

Table 5.21 External Bus Timing

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{SU(D-R)}$	Data setup time before read	40		ns
$t_{h(R-D)}$	Data hold time after read	0		ns
$t_{dis(R-D)}$	Data disable time after read		$0.5 \times t_{C(Base)} + 10$	ns

$$V_{CC} = 5 \text{ V}$$

Switching Characteristics ($V_{CC} = 4.2$ to 5.5 V , $V_{SS} = 0 \text{ V}$, and $T_a = T_{opr}$, unless otherwise noted)

Table 5.36 External Bus Timing (multiplexed bus)

Symbol	Characteristic	Measurement Condition	Value		Unit
			Min.	Max.	
$t_{su(S-ALE)}$	Chip-select setup time before ALE	Refer to Figure 5.6	(1)		ns
$t_{h(R-S)}$	Chip-select hold time after read		$1.5 \times t_{c(Base)} - 15$		ns
$t_{su(A-ALE)}$	Address setup time before ALE		(1)		ns
$t_{h(ALE-A)}$	Address hold time after ALE		$0.5 \times t_{c(Base)} - 5$		ns
$t_{h(R-A)}$	Address hold time after read		$1.5 \times t_{c(Base)} - 15$		ns
$t_{d(ALE-R)}$	ALE-read delay time		$0.5 \times t_{c(Base)} - 5$	$0.5 \times t_{c(Base)} + 10$	ns
$t_{w(ALE)}$	ALE pulse width		(1)		ns
$t_{dis(R-A)}$	Address disable time after read			8	ns
$t_{w(R)}$	Read pulse width		(1)		ns
$t_{h(W-S)}$	Chip-select hold time after write		$1.5 \times t_{c(Base)} - 15$		ns
$t_{h(W-A)}$	Address hold time after write		$1.5 \times t_{c(Base)} - 15$		ns
$t_{d(ALE-W)}$	ALE-write delay time		$0.5 \times t_{c(Base)} - 5$	$0.5 \times t_{c(Base)} + 10$	ns
$t_{w(W)}$	Write pulse width		(1)		ns
$t_{su(D-W)}$	Data setup time before write		(1)		ns
$t_{h(W-D)}$	Data hold time after write		$0.5 \times t_{c(Base)}$		ns

Note:

1. The value is calculated using the formulas below based on the base clock cycles ($t_{c(Base)}$) and respective cycles of $T_{su(A-R)}$, $T_{w(R)}$, $T_{su(A-W)}$, and $T_{w(W)}$ set by registers EBC0 to EBC3. If the calculation results in a negative value, modify the value to be set. For details on how to set values, refer to the User's manual.

$$t_{su(S-ALE)} = t_{su(A-ALE)} = t_{w(ALE)} = (T_{su(A-R)} - 0.5) \times t_{c(Base)} - 15 \text{ [ns]}$$

$$t_{w(R)} = T_{w(R)} \times t_{c(Base)} - 10 \text{ [ns]}$$

$$t_{w(W)} = t_{su(D-W)} = T_{w(W)} \times t_{c(Base)} - 10 \text{ [ns]}$$

$$V_{CC} = 3.3 \text{ V}$$

Table 5.41 Electrical Characteristics (1/3) ($V_{CC} = 3.0$ to 3.6 V , $V_{SS} = 0 \text{ V}$, $T_a = T_{opr}$, and $f_{(CPU)} = 64 \text{ MHz}$, unless otherwise noted)

Symbol	Characteristic		Measurement Condition	Value			Unit
				Min.	Typ.	Max.	
V_{OH}	High level output voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7, P14_3 to P14_6, P15_0 to P15_7 ⁽¹⁾	$I_{OH} = -1 \text{ mA}$	$V_{CC} - 0.6$		V_{CC}	V
V_{OL}	Low level output voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7, P14_3 to P14_6, P15_0 to P15_7 ⁽¹⁾	$I_{OL} = 1 \text{ mA}$			0.5	V

Note:

1. Ports P9_0, P9_2, and P11 to P15 are available in the 144-pin package only. Port P9_1 is designated as input pin in the 100-pin package.

$$V_{CC} = 3.3 \text{ V}$$

Timing Requirements ($V_{CC} = 3.0$ to 3.6 V , $V_{SS} = 0 \text{ V}$, and $T_a = T_{opr}$, unless otherwise noted)

Table 5.56 Serial Interface

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{C(CK)}$	CLKi input clock cycle time	200		ns
$t_{W(CKH)}$	CLKi input high level pulse width	80		ns
$t_{W(CKL)}$	CLKi input low level pulse width	80		ns
$t_{su(D-C)}$	RXDi input setup time	80		ns
$t_{h(C-D)}$	RXDi input hold time	90		ns

Table 5.57 A/D Trigger Input

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{W(ADH)}$	ADTRG input high level pulse width Hardware trigger input high level pulse width	$\frac{3}{\phi_{AD}}$		ns
$t_{W(ADL)}$	ADTRG input low level pulse width Hardware trigger input high level pulse width	125		ns

Table 5.58 External Interrupt $\overline{INTi}$ Input

Symbol	Characteristic		Value		Unit
			Min.	Max.	
$t_{W(INH)}$	$\overline{INTi}$ input high level pulse width	Edge sensitive	250		ns
		Level sensitive	$t_{C(CPU)} + 200$		ns
$t_{W(INL)}$	$\overline{INTi}$ input low level pulse width	Edge sensitive	250		ns
		Level sensitive	$t_{C(CPU)} + 200$		ns

Table 5.59 Intelligent I/O

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{C(ISCLK2)}$	ISCLK2 input clock cycle time	600		ns
$t_{W(ISCLK2H)}$	ISCLK2 input high level pulse width	270		ns
$t_{W(ISCLK2L)}$	ISCLK2 input low level pulse width	270		ns
$t_{su(RXD-ISCLK2)}$	ISRXD2 input setup time	150		ns
$t_{h(ISCLK2-RXD)}$	ISRXD2 input hold time	100		ns

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