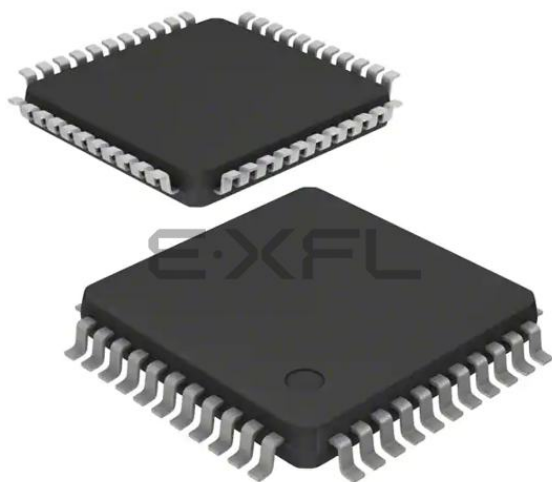




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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	eZ8
Core Size	8-Bit
Speed	20MHz
Connectivity	I ² C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	31
Program Memory Size	24KB (24K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LQFP
Supplier Device Package	44-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8f2421an020sg

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I²C

The I²C controller makes the Z8 Encore! XP F64xx Series compatible with the I²C protocol. The I²C controller consists of two bidirectional bus lines, a serial data (SDA) line and a serial clock (SCL) line.

Serial Peripheral Interface

The serial peripheral interface allows the Z8 Encore! XP F64xx Series to exchange data between other peripheral devices such as EEPROMs, A/D converters and ISDN devices. The SPI is a full-duplex, synchronous, character-oriented channel that supports a four-wire interface.

Timers

Up to four 16-bit reloadable timers can be used for timing/counting events or for motor control operations. These timers provide a 16-bit programmable reload counter and operate in ONE-SHOT, CONTINUOUS, GATED, CAPTURE, COMPARE, CAPTURE AND COMPARE and PWM modes. Only 3 timers (Timer 0–2) are available in the 44-pin package.

Interrupt Controller

The Z8 Encore! XP F64xx Series products support up to 24 interrupts. These interrupts consist of 12 internal and 12 GPIO pins. The interrupts have 3 levels of programmable interrupt priority.

Reset Controller

The Z8 Encore! XP F64xx Series can be reset using the $\overline{\text{RESET}}$ pin, Power-On Reset, Watchdog Timer, STOP Mode exit, or Voltage Brown-Out (VBO) warning signal.

On-Chip Debugger

The Z8 Encore! XP F64xx Series features an integrated On-Chip Debugger. The OCD provides a rich set of debugging capabilities, such as reading and writing registers, programming the Flash, setting breakpoints and executing code. A single-pin interface provides communication to the OCD.

Table 6. Z8 Encore! XP F64xx Series Information Area Map

Program Memory Address (Hex)	Function
FE00H–FE3FH	Reserved
FE40H–FE53H	Part Number 20-character ASCII alphanumeric code Left-justified and filled with zeros (ASCII Null character)
FE54H–FFFFH	Reserved

Table 7. Z8 Encore! XP F64xx Series Register File Address Map (Continued)

Address (Hex)	Register Description	Mnemonic	Reset (Hex)	Page
UART 1 (continued)				
F4D	UART1 Address Compare Register	U1ADDR	00	105
F4E	UART1 Baud Rate High Byte	U1BRH	FF	105
F4F	UART1 Baud Rate Low Byte	U1BRL	FF	105
I²C				
F50	I ² C Data	I2CDATA	00	141
F51	I ² C Status	I2CSTAT	80	142
F52	I ² C Control	I2CCTL	00	144
F53	I ² C Baud Rate High Byte	I2CBRH	FF	145
F54	I ² C Baud Rate Low Byte	I2CBRL	FF	145
F55	I ² C Diagnostic State	I2CDST	C0	147
F56	I ² C Diagnostic Control	I2CDIAG	00	149
F57–F5F	Reserved	—	XX	
Serial Peripheral Interface (SPI)				
F60	SPI Data	SPIDATA	XX	121
F61	SPI Control	SPICTL	00	122
F62	SPI Status	SPISTAT	01	123
F63	SPI Mode	SPIMODE	00	125
F64	SPI Diagnostic State	SPIDST	00	126
F65	Reserved	—	XX	
F66	SPI Baud Rate High Byte	SPIBRH	FF	126
F67	SPI Baud Rate Low Byte	SPIBRL	FF	126
F68–F6F	Reserved	—	XX	
Analog-to-Digital Converter				
F70	ADC Control	ADCCTL	20	165
F71	Reserved	—	XX	
F72	ADC Data High Byte	ADCD_H	XX	167
F73	ADC Data Low Bits	ADCD_L	XX	168
F74–FAF	Reserved	—	XX	
DMA 0				
FB0	DMA0 Control	DMA0CTL	00	153
FB1	DMA0 I/O Address	DMA0IO	XX	154

Note: XX = Undefined.

Table 10. Stop Mode Recovery Sources and Resulting Action

Operating Mode	Stop Mode Recovery Source	Action
STOP Mode	Watchdog Timer time-out when configured for Reset.	Stop Mode Recovery.
	Watchdog Timer time-out when configured for interrupt.	Stop Mode Recovery followed by interrupt (if interrupts are enabled).
	Data transition on any GPIO port pin enabled as a Stop Mode Recovery source.	Stop Mode Recovery.

Stop Mode Recovery Using Watchdog Timer Time-Out

If the Watchdog Timer times out during STOP Mode, the device undergoes a Stop Mode Recovery sequence. In the Watchdog Timer Control Register, the WDT and stop bits are set to 1. If the Watchdog Timer is configured to generate an interrupt upon time-out and the Z8 Encore! XP F64xx Series devices are configured to respond to interrupts, the eZ8 CPU services the Watchdog Timer interrupt request following the normal Stop Mode Recovery sequence.

Stop Mode Recovery Using a GPIO Port Pin Transition HALT

Each of the GPIO port pins may be configured as a Stop Mode Recovery input source. On any GPIO pin enabled as a Stop Mode Recovery source, a change in the input pin value (from High to Low or from Low to High) initiates Stop Mode Recovery. The GPIO Stop Mode Recovery signals are filtered to reject pulses less than 10 ns (typical) in duration. In the Watchdog Timer Control Register, the stop bit is set to 1.

! **Caution:** In STOP Mode, the GPIO Port Input Data registers (PxIN) are disabled. The Port Input Data registers record the Port transition only if the signal stays on the Port pin through the end of the Stop Mode Recovery delay. Thus, short pulses on the Port pin can initiate Stop Mode Recovery without being written to the Port Input Data Register or without initiating an interrupt (if enabled for that pin).

IRQ2 Enable High and Low Bit Registers

Table 33 describes the priority control for IRQ2. The IRQ2 Enable High and Low Bit registers, shown in Tables 34 and 35, form a priority-encoded enabling for interrupts in the Interrupt Request 2 Register. Priority is generated by setting bits in each register.

Table 33. IRQ2 Enable and Priority Encoding

IRQ2ENH[x]	IRQ2ENL[x]	Priority	Description
0	0	Disabled	Disabled
0	1	Level 1	Low
1	0	Level 2	Nominal
1	1	Level 3	High

Note: x indicates register bits in the range [7:0].

Table 34. IRQ2 Enable High Bit Register (IRQ2ENH)

Bit	7	6	5	4	3	2	1	0
Field	T3ENH	U1RENH	U1TENH	DMAENH	C3ENH	C2ENH	C1ENH	C0ENH
RESET	0							
R/W	R/W							
Address	FC7H							

Bit	Description
[7] T3ENH	Timer 3 Interrupt Request Enable High Bit
[6] U1RENH	UART 1 Receive Interrupt Request Enable High Bit
[5] U1TENH	UART 1 Transmit Interrupt Request Enable High Bit
[4] DMAENH	DMA Interrupt Request Enable High Bit
[3] C3ENH	Port C3 Interrupt Request Enable High Bit
[2] C2ENH	Port C2 Interrupt Request Enable High Bit
[1] C1ENH	Port C1 Interrupt Request Enable High Bit
[0] C0ENH	Port C0 Interrupt Request Enable High Bit

Timer Reload High and Low Byte Registers

The Timer 0–3 Reload High and Low Byte (TxRH and TxRL) registers, shown in Tables 41 and 42, store a 16-bit reload value, {TRH[7:0], TRL[7:0]}. Values written to the Timer Reload High Byte Register are stored in a temporary holding register. When a write to the Timer Reload Low Byte Register occurs, the temporary holding register value is written to the Timer High Byte Register. This operation allows simultaneous updates of the 16-bit timer reload value.

In COMPARE Mode, the Timer Reload High and Low Byte registers store the 16-bit compare value.

Table 41. Timer 0–3 Reload High Byte Register (TxRH)

Bit	7	6	5	4	3	2	1	0
Field	TRH							
RESET	1							
R/W	R/W							
Address	F02H, F0AH, F12H, F1AH							

Table 42. Timer 0–3 Reload Low Byte Register (TxRL)

Bit	7	6	5	4	3	2	1	0
Field	TRL							
RESET	1							
R/W	R/W							
Address	F03H, F0BH, F13H, F1BH							

Bit	Description
[7:0] TRH, TRL	Timer Reload Register High and Low These two bytes form the 16-bit reload value, {TRH[7:0], TRL[7:0]}. This value sets the maximum count value which initiates a timer reload to 0001H. In COMPARE Mode, these two bytes form the 16-bit compare value.

Timer 0–3 Control 1 Registers

The Timer 0–3 Control 1 (TxCTL1) registers enable/disable the timers, set the prescaler value, and determine the timer operating mode.

Table 46. Timer 0–3 Control 1 Register (TxCTL1)

Bit	7	6	5	4	3	2	1	0
Field	TEN	TPOL	PRES			TMODE		
RESET	0							
R/W	R/W							
Address	F07H, F0FH, F17H, F1FH							

- Set or clear the CTSE bit to enable or disable control from the remote receiver via the CTS pin
8. Execute an EI instruction to enable interrupts.

The UART is now configured for interrupt-driven data transmission. Because the UART Transmit Data Register is empty, an interrupt is generated immediately. When the UART transmit interrupt is detected, the associated interrupt service routine performs the following functions:

1. Write the UART Control 1 Register to select the outgoing address bit:
 - Set the MULTIPROCESSOR Bit Transmitter (MPBT) if sending an address byte; clear it if sending a data byte.
2. Write the data byte to the UART Transmit Data Register. The transmitter automatically transfers the data to the Transmit Shift Register and transmits the data.
3. Clear the UART transmit interrupt bit in the applicable Interrupt Request Register.
4. Execute the IRET instruction to return from the interrupt service routine and wait for the Transmit Data Register to again become empty.

Receiving Data using the Polled Method

Observe the following procedure to configure the UART for polled data reception:

1. Write to the UART Baud Rate High and Low Byte registers to set the appropriate baud rate.
2. Enable the UART pin functions by configuring the associated GPIO port pins for alternate function operation.
3. Write to the UART Control 1 Register to enable MULTIPROCESSOR Mode functions, if appropriate.
4. Write to the UART Control 0 Register to:
 - Set the receive enable bit (REN) to enable the UART for data reception
 - Enable parity, if appropriate and if MULTIPROCESSOR Mode is not enabled, and select either even or odd parity
5. Check the RDA bit in the UART Status 0 Register to determine if the Receive Data Register contains a valid data byte (indicated by a 1). If RDA is set to 1 to indicate available data, continue to [Step 6](#). If the Receive Data Register is empty (indicated by a 0), continue to monitor the RDA bit awaiting reception of the valid data.

The next time $\overline{SS}$ asserts, the MISO pin outputs SPIDAT[7], regardless of where the previous transaction left off. Writing a 1 to ABT clears this error flag.

SPI Interrupts

When SPI interrupts are enabled, the SPI generates an interrupt after character transmission/reception completes in both MASTER and SLAVE modes. A character can be defined to be 1 through 8 bits by the NUMBITS field in the SPI Mode Register. In slave mode it is not necessary for $\overline{SS}$ to deassert between characters to generate the interrupt. The SPI in Slave mode can also generate an interrupt if the $\overline{SS}$ signal deasserts prior to transfer of all the bits in a character (see description of slave abort error above). Writing a 1 to the IRQ bit in the SPI Status Register clears the pending SPI interrupt request. The IRQ bit must be cleared to 0 by the Interrupt Service Routine to generate future interrupts. To start the transfer process, an SPI interrupt may be forced by software writing a 1 to the STR bit in the SPICTL Register.

If the SPI is disabled, an SPI interrupt can be generated by a Baud Rate Generator time-out. This timer function must be enabled by setting the BIRQ bit in the SPICTL Register. This Baud Rate Generator time-out does not set the IRQ bit in the SPISTAT Register, just the SPI interrupt bit in the interrupt controller.

SPI Baud Rate Generator

In SPI Master Mode, the Baud Rate Generator creates a lower frequency serial clock (SCK) for data transmission synchronization between the Master and the external Slave. The input to the Baud Rate Generator is the system clock. The SPI Baud Rate High and Low Byte registers combine to form a 16-bit reload value, BRG[15:0], for the SPI Baud Rate Generator. The SPI baud rate is calculated using the following equation:

$$\text{SPI Baud Rate (bits/s)} = \frac{\text{System Clock Frequency (Hz)}}{2 \times \text{BRG}[15:0]}$$

Minimum baud rate is obtained by setting BRG[15:0] to 0000H for a clock divisor value of $(2 \times 65536 = 131072)$.

When the SPI is disabled, the Baud Rate Generator can function as a basic 16-bit timer with interrupt on time-out. Observe the following procedure to configure the Baud Rate Generator as a timer with interrupt on time-out:

1. Disable the SPI by clearing the SPIEN bit in the SPI Control Register to 0.
2. Load the appropriate 16-bit count value into the SPI Baud Rate High and Low Byte registers.
3. Enable the Baud Rate Generator timer function and associated interrupt by setting the BIRQ bit in the SPI Control Register to 1.

I²C Controller

The I²C Controller makes the Z8 Encore! XP F64xx Series products bus-compatible with the I²C protocol. The I²C Controller consists of two bidirectional bus lines: a serial data signal (SDA) and a serial clock signal (SCL). Features of the I²C Controller include:

- Transmit and Receive Operation in MASTER Mode
- Maximum data rate of 400kilobit/sec
- 7- and 10-bit addressing modes for Slaves
- Unrestricted number of data bytes transmitted per transfer

The I²C Controller in the Z8 Encore! XP F64xx Series products does not operate in SLAVE Mode.

Architecture

Figure 27 displays the architecture of the I²C Controller.

ADC Data High Byte Register

The ADC Data High Byte Register, shown in Table 88, contains the upper eight bits of the 10-bit ADC output. During a single-shot conversion, this value is invalid. Access to the ADC Data High Byte Register is read-only. The full 10-bit ADC result is provided by {ADCD_H[7:0], ADCD_L[7:6]}. Reading the ADC Data High Byte Register latches data in the ADC Low Bits Register.

Table 88. ADC Data High Byte Register (ADCD_H)

Bit	7	6	5	4	3	2	1	0
Field	ADCD_H							
RESET	X							
R/W	R							
Address	F72H							

Bit	Description
[7:0]	ADC Data High Byte
ADCD_H	This byte contains the upper eight bits of the 10-bit ADC output. These bits are not valid during a single-shot conversion. During a continuous conversion, the last conversion output is held in this register. These bits are undefined after a Reset.

The write-only Flash Control Register shares its Register File address with the read-only Flash Status Register.

Table 93. Flash Control Register (FCTL)

Bit	7	6	5	4	3	2	1	0
Field	FCMD							
RESET	0							
R/W	W							
Address	FF8H							

Bit	Description
[7:0]	Flash Command*
FCMD	73H = First unlock command. 8CH = Second unlock command. 95H = Page erase command. 63H = Mass erase command 5EH = Flash Sector Protect Register select.

Note: *All other commands, or any command out of sequence, lock the Flash Controller.

Figure 45 displays the typical current consumption in HALT Mode while operating at 25°C plotted opposite the system clock frequency. All GPIO pins are configured as outputs and driven High.

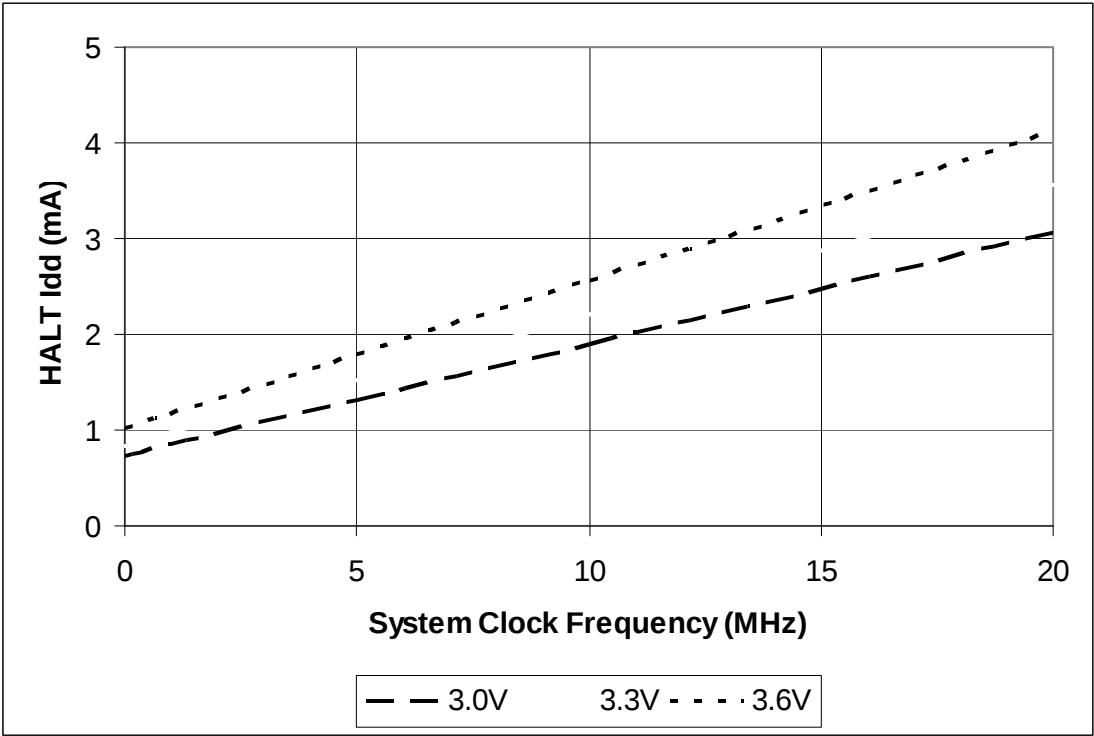


Figure 45. Typical HALT Mode I_{DD} vs. System Clock Frequency

Table 113 provides electrical characteristics and timing information for the Analog-to-Digital Converter. Figure 49 displays the input frequency response of the ADC.

Table 113. Analog-to-Digital Converter Electrical Characteristics and Timing

Symbol	Parameter	$V_{DD} = 3.0V-3.6V$ $T_A = -40^{\circ}C \text{ to } 125^{\circ}C$			Units	Conditions
		Minimum	Typical	Maximum		
	Resolution	10	–	–	bits	External $V_{REF} = 3.0V$;
	Differential Nonlinearity (DNL)	–1.0		+1.0	lsb	Guaranteed by design
	Integral Nonlinearity (INL)	–3.0	± 1.0	3.0	lsb	External $V_{REF} = 3.0V$
	DC Offset Error	–35	–	25	mV	80-pin QFP and 64-pin LQFP packages.
	DC Offset Error	–50	–	25	mV	44-pin LQFP, 44-pin PLCC, and 68-pin PLCC packages.
V_{REF}	Internal Reference Voltage	1.9	2.0	2.4	V	$V_{DD} = 3.0V-3.6V$ $T_A = -40^{\circ}C \text{ to } 105^{\circ}C$
VC_{REF}	Voltage Coefficient of Internal Reference Voltage	–	78	–	mV/V	V_{REF} variation as a function of AV_{DD} .
TC_{REF}	Temperature Coefficient of Internal Reference Voltage	–	1	–	mV/ $^{\circ}C$	
	Single-Shot Conversion Period	–	5129	–	cycles	System clock cycles
	Continuous Conversion Period	–	256	–	cycles	System clock cycles
R_S	Analog Source Impedance	–	–	150	W	Recommended
Z_{in}	Input Impedance		150		k Ω	20MHz system clock. Input impedance increases with lower system clock frequency.
V_{REF}	External Reference Voltage			AV_{DD}	V	$AV_{DD} \leq V_{DD}$. When using an external reference voltage, decoupling capacitance should be placed from V_{REF} to AV_{SS} .

Table 136. eZ8 CPU Instruction Summary (Continued)

Assembly Mnemonic	Symbolic Operation	Address Mode		Opcode(s) (Hex)	Flags						Fetch Cycles	Instr. Cycles
		dst	src		C	Z	S	V	D	H		
TM dst, src	dst AND src	r	r	72	–	*	*	0	–	–	2	3
		r	lr	73							2	4
		R	R	74							3	3
		R	IR	75							3	4
		R	IM	76							3	3
		IR	IM	77							3	4
TMX dst, src	dst AND src	ER	ER	78	–	*	*	0	–	–	4	3
		ER	IM	79							4	3
TRAP Vector	SP ← SP – 2 @SP ← PC SP ← SP – 1 @SP ← FLAGS PC ← @Vector		Vector	F2	–	–	–	–	–	–	2	6
WDT				5F	–	–	–	–	–	–	1	2
XOR dst, src	dst ← dst XOR src	r	r	B2	–	*	*	0	–	–	2	3
		r	lr	B3							2	4
		R	R	B4							3	3
		R	IR	B5							3	4
		R	IM	B6							3	3
		IR	IM	B7							3	4
XORX dst, src	dst ← dst XOR src	ER	ER	B8	–	*	*	0	–	–	4	3
		ER	IM	B9							4	3

Note: Flags Notation:

* = Value is a function of the result of the operation.

– = Unaffected.

X = Undefined.

0 = Reset to 0.

1 = Set to 1.

Hex Address: FB4

Table 208. DMAx End Address Low Byte Register (DMAxEND)

Bit	7	6	5	4	3	2	1	0
Field	DMA_END							
RESET	X							
R/W	R/W							
Address	FB4H, FBCH							

Hex Addresses: FB5–FB7

This address range is reserved.

Hex Address: FB8

Table 209. DMAx Control Register (DMAxCTL)

Bit	7	6	5	4	3	2	1	0
Field	DEN	DLE	DDIR	IRQEN	WSEL	RSS		
RESET	0							
R/W	R/W							
Address	FB0H, FB8H							

Hex Address: FB9

Table 210. DMAx I/O Address Register (DMAxIO)

Bit	7	6	5	4	3	2	1	0
Field	DMA_IO							
RESET	X							
R/W	R/W							
Address	FB1H, FB9H							

Table 271. Z8 Encore! XP F64xx Series Ordering Matrix

Part Number	Flash	RAM	I/O Lines	Interrupts	16-Bit Timers w/PWM	10-Bit A/D Channels	I ² C	SPI	UARTs with IrDA	Description
Z8F482x with 48KB Flash, 10-Bit Analog-to-Digital Converter										
Standard Temperature: 0°C to 70°C										
Z8F4821PM020SG	48KB	4KB	29	23	3	8	1	1	2	PDIP 40-pin package
Z8F4821AN020SG	48KB	4KB	31	23	3	8	1	1	2	LQFP 44-pin package
Z8F4821VN020SG	48KB	4KB	31	23	3	8	1	1	2	PLCC 44-pin package
Z8F4822AR020SG	48KB	4KB	46	24	4	12	1	1	2	LQFP 64-pin package
Z8F4822VS020SG	48KB	4KB	46	24	4	12	1	1	2	PLCC 68-pin package
Z8F4823FT020SG	48KB	4KB	60	24	4	12	1	1	2	QFP 80-pin package
Extended Temperature: –40°C to +105°C										
Z8F4821PM020EG	48KB	4KB	29	23	3	8	1	1	2	PDIP 40-pin package
Z8F4821AN020EG	48KB	4KB	31	23	3	8	1	1	2	LQFP 44-pin package
Z8F4821VN020EG	48KB	4KB	31	23	3	8	1	1	2	PLCC 44-pin package
Z8F4822AR020EG	48KB	4KB	46	24	4	12	1	1	2	LQFP 64-pin package
Z8F4822VS020EG	48KB	4KB	46	24	4	12	1	1	2	PLCC 68-pin package
Z8F4823FT020EG	48KB	4KB	60	24	4	12	1	1	2	QFP 80-pin package
Automotive/Industrial Temperature: –40°C to +125°C										
Z8F4821PM020AG	48KB	4KB	29	23	3	8	1	1	2	PDIP 40-pin package
Z8F4821AN020AG	48KB	4KB	31	23	3	8	1	1	2	LQFP 44-pin package
Z8F4821VN020AG	48KB	4KB	31	23	3	8	1	1	2	PLCC 44-pin package
Z8F4822AR020AG	48KB	4KB	46	24	4	12	1	1	2	LQFP 64-pin package
Z8F4822VS020AG	48KB	4KB	46	24	4	12	1	1	2	PLCC 68-pin package
Z8F4823FT020AG	48KB	4KB	60	24	4	12	1	1	2	QFP 80-pin package

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