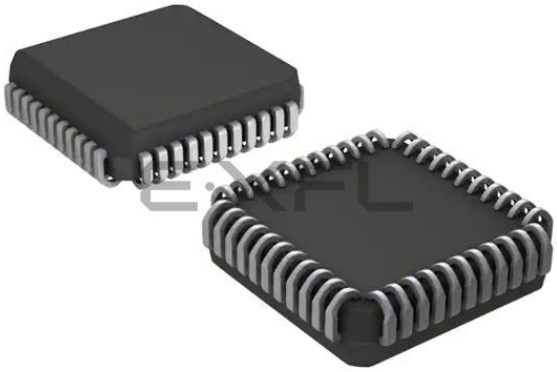

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	eZ8
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	31
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8f3221vn020sg

- Software stack allows much greater depth in subroutine calls and interrupts than hardware stacks
- Compatible with existing Z8 code
- Expanded internal Register File allows access of up to 4KB
- New instructions improve execution efficiency for code developed using higher-level programming languages, including C
- Pipelined instruction fetch and execution
- New instructions for improved performance including BIT, BSWAP, BTJ, CPC, LDC, LDCI, LEA, MULT and SRL
- New instructions support 12-bit linear addressing of the Register File
- Up to 10 MIPS operation
- C-Compiler friendly
- 2 to 9 clock cycles per instruction

For more information about the eZ8 CPU, refer to the eZ8 CPU Core User Manual (UM0128), which is available for download on www.zilog.com.

General-Purpose Input/Output

The Z8 Encore! XP F64xx Series features seven 8-bit ports (ports A–G) and one 4-bit port (Port H) for general-purpose input/output (GPIO). Each pin is individually programmable. All ports (except B and H) support 5V-tolerant inputs.

Flash Controller

The Flash Controller programs and erases the contents of Flash memory.

10-Bit Analog-to-Digital Converter

The Analog-to-Digital Converter converts an analog input signal to a 10-bit binary number. The ADC accepts inputs from up to 12 different analog input sources.

UARTs

Each UART is full-duplex and capable of handling asynchronous data transfers. The UARTs support 8- and 9-bit data modes, selectable parity, and an efficient bus transceiver Driver Enable signal for controlling a multitransceiver bus, such as RS-485.

Table 6. Z8 Encore! XP F64xx Series Information Area Map

Program Memory Address (Hex)	Function
FE00H–FE3FH	Reserved
FE40H–FE53H	Part Number 20-character ASCII alphanumeric code Left-justified and filled with zeros (ASCII Null character)
FE54H–FFFFH	Reserved

Every subsequent appropriate transition (after the first) of the timer input signal captures the current count value. The Capture value is written to the Timer PWM High and Low Byte Registers. When the capture event occurs, an interrupt is generated, the count value in the Timer High and Low Byte registers is reset to 0001H, and counting resumes.

If no capture event occurs, the timer counts up to the 16-bit compare value stored in the Timer Reload High and Low Byte registers. Upon reaching the compare value, the timer generates an interrupt, the count value in the Timer High and Low Byte registers is reset to 0001H and counting resumes.

Observe the following procedure for configuring a timer for CAPTURE/COMPARE Mode and initiating the count:

1. Write to the Timer Control 1 Register to:
   - Disable the timer
   - Configure the timer for CAPTURE/COMPARE Mode
   - Set the prescale value
   - Set the Capture edge (rising or falling) for the timer input
2. Write to the Timer High and Low Byte registers to set the starting count value (typically 0001H).
3. Write to the Timer Reload High and Low Byte registers to set the compare value.
4. If appropriate, enable the timer interrupt and set the timer interrupt priority by writing to the relevant interrupt registers.
5. Configure the associated GPIO port pin for the timer input alternate function.
6. Write to the Timer Control 1 Register to enable the timer.
7. Counting begins on the first appropriate transition of the timer input signal. No interrupt is generated by this first edge.

In COMPARE Mode, the elapsed time from timer start to capture event can be calculated using the following equation:

$$\text{Capture Elapsed Time (s)} = \frac{(\text{Capture Value} - \text{Start Value}) \times \text{Prescale}}{\text{System Clock Frequency (Hz)}}$$

Reading the Timer Count Values

The current count value in the timers can be read while counting (enabled). This capability has no effect on timer operation. When the timer is enabled and the Timer High Byte Register is read, the contents of the Timer Low Byte Register are placed in a holding register. A subsequent read from the Timer Low Byte Register returns the value in the holding reg-

Table 48. Watchdog Timer Control Register (WDTCTL)

Bit	7	6	5	4	3	2	1	0
Field	POR	STOP	WDT	EXT	Reserved			SM
RESET	See Table 49.			0				
R/W	R							
Address	FF0H							

Bit	Description
[7] POR	**Power-On Reset Indicator** If this bit is set to 1, a Power-On Reset event occurred. This bit is reset to 0 if a WDT time-out or Stop Mode Recovery occurs. This bit is also reset to 0 when the register is read.
[6] STOP	**Stop Mode Recovery Indicator** If this bit is set to 1, a Stop Mode Recovery occurred. If the stop and WDT bits are both set to 1, the Stop Mode Recovery occurred due to a WDT time-out. If the stop bit is 1 and the WDT bit is 0, the Stop Mode Recovery was not caused by a WDT time-out. This bit is reset by a Power-On Reset or a WDT time-out that occurred while not in STOP Mode. Reading this register also resets this bit.
[5] WDT	**Watchdog Timer Time-Out Indicator** If this bit is set to 1, a WDT time-out occurred. A Power-On Reset resets this pin. A Stop Mode Recovery from a change in an input pin also resets this bit. Reading this register resets this bit.
[4] EXT	**External Reset Indicator** If this bit is set to 1, a Reset initiated by the external $\overline{\text{RESET}}$ pin occurred. A Power-On Reset or a Stop Mode Recovery from a change in an input pin resets this bit. Reading this register resets this bit.
[3:1]	**Reserved** These bits are reserved and must be programmed to 000.
[0] SM	**STOP Mode Configuration Indicator** 0 = Watchdog Timer and its internal RC oscillator will continue to operate in STOP Mode. 1 = Watchdog Timer and its internal RC oscillator will be disabled in STOP Mode.

Table 60. UART Baud Rate High Byte Register (U*x*BRH)

Bit	7	6	5	4	3	2	1	0
Field	BRH							
RESET	1							
R/W	R/W							
Address	F46H and F4EH							

Table 61. UART Baud Rate Low Byte Register (U*x*BRL)

Bit7	7	6	5	4	3	2	1	0
Field	BRL							
RESET	1							
R/W	R/W							
Address	F47H and F4FH							

For a given UART data rate, the integer baud rate divisor value is calculated using the following equation:

$$\text{UART Baud Rate Divisor Value (BRG)} = \text{Round}\left(\frac{\text{System Clock Frequency (Hz)}}{16 \times \text{UART Data Rate (bits/s)}}\right)$$

The baud rate error relative to the appropriate baud rate is calculated using the following equation:

$$\text{UART Baud Rate Error (\%)} = 100 \times \left(\frac{\text{Actual Data Rate} - \text{Desired Data Rate}}{\text{Desired Data Rate}}\right)$$

For reliable communication, the UART baud rate error must never exceed 5 percent. Table 62 lists data rate errors for popular baud rates and commonly used crystal oscillator frequencies.

SPI Mode Register

The SPI Mode Register, shown in Table 67, configures the character bit width and the direction and value of the $\overline{SS}$ pin.

Table 67. SPI Mode Register (SPIMODE)

Bit	7	6	5	4	3	2	1	0
Field	Reserved		DIAG	NUMBITS[2:0]			SSIO	SSV
RESET	0							
R/W	R		R/W					
Address	F63H							

Bit	Description
[7:6]	**Reserved** These bits are reserved and must be programmed to 00.
[5] DIAG	**Diagnostic Mode Control bit** This bit is for SPI diagnostics. Setting this bit allows the Baud Rate Generator value to be read using the SPIBRH and SPIBRL Register locations. 0 = Reading SPIBRH, SPIBRL returns the value in the SPIBRH and SPIBRL registers. 1 = Reading SPIBRH returns bits [15:8] of the SPI Baud Rate Generator; and reading SPIBRL returns bits [7:0] of the SPI Baud Rate Counter. The Baud Rate Counter High and Low byte values are not buffered. **Caution:** Exercise caution if reading the values while the BRG is counting.
[4] NUMBITS[2:0]	**Number of Data Bits Per Character to Transfer** This field contains the number of bits to shift for each character transfer. For information about valid bit positions when the character length is less than 8 bits, see the SPI Data Register (SPIDATA) description. 000 = 8 bits. 001 = 1 bit. 010 = 2 bits. 011 = 3 bits. 100 = 4 bits. 101 = 5 bits. 110 = 6 bits. 111 = 7 bits.
[1] SSIO	**Slave Select I/O** 0 = $\overline{SS}$ pin configured as an input. 1 = $\overline{SS}$ pin configured as an output (Master mode only).
[0] SSV	**Slave Select Value** If SSIO = 1 and SPI is configured as a Master, the following conditions are true: 0 = $\overline{SS}$ pin driven Low (0). 1 = $\overline{SS}$ pin driven High (1). This bit has no effect if SSIO = 0 or if SPI is configured as a Slave.

Table 71. I²C Data Register (I2CDATA)

Bit	7	6	5	4	3	2	1	0
Field	DATA							
RESET	0							
R/W	R/W							
Address	F50H							

I²C Status Register

The read-only I²C Status Register, shown in Table 72, indicates the status of the I²C Controller.

Table 72. I²C Status Register (I2CSTAT)

Bit	7	6	5	4	3	2	1	0
Field	TDRE	RDRF	ACK	10B	RD	TAS	DSS	NCKI
RESET	1	0						
R/W	R							
Address	F51H							

Bit	Description
[7] TDRE	**Transmit Data Register Empty** When the I²C Controller is enabled, this bit is 1 when the I²C Data Register is empty. When this bit is set, an interrupt is generated if the TXI bit is set, except when the I²C Controller is shifting in data during the reception of a byte or when shifting an address and the RD bit is set. This bit is cleared by writing to the I2CDATA Register.
[6] RDRF	**Receive Data Register Full** This bit is set = 1 when the I²C Controller is enabled and the I²C Controller has received a byte of data. When asserted, this bit causes the I²C Controller to generate an interrupt. This bit is cleared by reading the I²C Data Register (unless the read is performed using execution of the On-Chip Debugger's Read Register command).

Operation

This section describes the operational aspects of the ADC's power-down and conversion features.

Automatic Power-Down

If the ADC is idle (i.e., no conversions are in progress) for 160 consecutive system clock cycles, portions of the ADC are automatically powered down. From this powered-down state, the ADC requires 40 system clock cycles to power up. The ADC powers up when a conversion is requested using the ADC Control Register.

Single-Shot Conversion

When configured for single-shot conversion, the ADC performs a single analog-to-digital conversion on the selected analog input channel. After completion of the conversion, the ADC shuts down. Observe the following procedure for setting up the ADC and initiating a single-shot conversion:

1. Enable the appropriate analog inputs by configuring the general-purpose I/O pins for alternate function. This configuration disables the digital input and output drivers.
2. Write to the ADC Control Register to configure the ADC and begin the conversion. The bit fields in the ADC Control Register can be written simultaneously:
   - Write to the ANAIN[3:0] field to select one of the 12 analog input sources
   - Clear CONT to 0 to select a single-shot conversion
   - Write to the $\overline{\text{VREF}}$ bit to enable or disable the internal voltage reference generator
   - Set CEN to 1 to start the conversion
3. CEN remains 1 while the conversion is in progress. A single-shot conversion requires 5129 system clock cycles to complete. If a single-shot conversion is requested from an ADC powered-down state, the ADC uses 40 additional clock cycles to power up before beginning the 5129 cycle conversion.
4. When the conversion is complete, the ADC control logic performs the following operations:
   - 10-bit data result written to {ADCD_H[7:0], ADCD_L[7:6]}
   - CEN resets to 0 to indicate the conversion is complete
   - An interrupt request is sent to the Interrupt Controller
5. If the ADC remains idle for 160 consecutive system clock cycles, it is automatically powered down.

Continuous Conversion

When configured for continuous conversion, the ADC continuously performs an analog-to-digital conversion on the selected analog input. Each new data value over-writes the previous value stored in the ADC Data registers. An interrupt is generated after each conversion.

Caution: In CONTINUOUS Mode, you must be aware that ADC updates are limited by the input signal bandwidth of the ADC and the latency of the ADC and its digital filter. Step changes at the input are not seen at the next output from the ADC. The response of the ADC (in all modes) is limited by the input signal bandwidth and the latency.

Observe the following procedure for setting up the ADC and initiating continuous conversion:

1. Enable the appropriate analog input by configuring the general-purpose I/O pins for alternate function. This disables the digital input and output driver.
2. Write to the ADC Control Register to configure the ADC for continuous conversion. The bit fields in the ADC Control Register may be written simultaneously:
   - Write to the ANAIN[3:0] field to select one of the 12 analog input sources
   - Set CONT to 1 to select continuous conversion
   - Write to the $\overline{\text{VREF}}$ bit to enable or disable the internal voltage reference generator
   - Set CEN to 1 to start the conversions
3. When the first conversion in continuous operation is complete (after 5129 system clock cycles, plus the 40 cycles required to power up, if necessary), the ADC control logic performs the following operations:
   - CEN resets to 0 to indicate the first conversion is complete. CEN remains 0 for all subsequent conversions in continuous operation
   - An interrupt request is sent to the Interrupt Controller to indicate the conversion is complete
4. Thereafter, the ADC writes a new 10-bit data result to {ADCD_H[7:0], ADCD_L[7:6]} every 256 system clock cycles. An interrupt request is sent to the Interrupt Controller when each conversion is complete.
5. To disable continuous conversion, clear the CONT bit in the ADC Control Register to 0.

ADC Data Low Bits Register

The ADC Data Low Bits Register, Table 89, contains the lower two bits of the conversion value. The data in the ADC Data Low Bits Register is latched each time the ADC Data High Byte Register is read. Reading this register always returns the lower two bits of the conversion last read into the ADC High Byte Register. Access to the ADC Data Low Bits Register is read-only. The full 10-bit ADC result is provided by {ADCD_H[7:0], ADCD_L[7:6]}.

Table 89. ADC Data Low Bits Register (ADCD_L)

Bit	7	6	5	4	3	2	1	0
Field	ADCD_L		Reserved					
RESET	X							
R/W	R							
Address	F73H							

Bit	Description
[7:6] ADCD_L	**ADC Data Low Bits** These are the least significant two bits of the 10-bit ADC output. These bits are undefined after a Reset.
[5:0]	**Reserved** These bits are reserved and are always undefined.

Bit	Description (Continued)
[4] BRKLOOP	**Breakpoint Loop** This bit determines what action the OCD takes when a BRK instruction is decoded if breakpoints are enabled (BRKEN is 1). If this bit is 0, then the DBGMODE bit is automatically set to 1 and the OCD entered DEBUG Mode. If BRKLOOP is set to 1, then the eZ8 CPU loops on the BRK instruction. 0 = BRK instruction sets DBGMODE to 1. 1 = eZ8 CPU loops on BRK instruction.
[3:1]	**Reserved** These bits are reserved and must be programmed to 000.
[0] RST	**Reset** Setting this bit to 1 resets the Z8 Encore! XP F64xx Series devices. The devices go through a normal Power-On Reset sequence with the exception that the On-Chip Debugger is not reset. This bit is automatically cleared to 0 when the reset finishes. 0 = No effect. 1 = Reset the Z8 Encore! XP F64xx Series device.

OCD Status Register

The OCD Status Register, shown in Table 104, reports status information about the current state of the debugger and the system.

Table 104. OCD Status Register (OCDSTAT)

Bit	7	6	5	4	3	2	1	0
Field	IDLE	HALT	RPEN	Reserved				
RESET	0							
R/W	R							

Bit	Description
[7] IDLE	**CPU Idle** This bit is set if the part is in DEBUG Mode (DBGMODE is 1), or if a BRK instruction occurred since the last time OCDCTL was written. This can be used to determine if the CPU is running or if it is idling. 0 = The eZ8 CPU is running. 1 = The eZ8 CPU is either stopped or looping on a BRK instruction.
[6] HALT	**HALT Mode** 0 = The device is not in HALT Mode. 1 = The device is in HALT Mode.

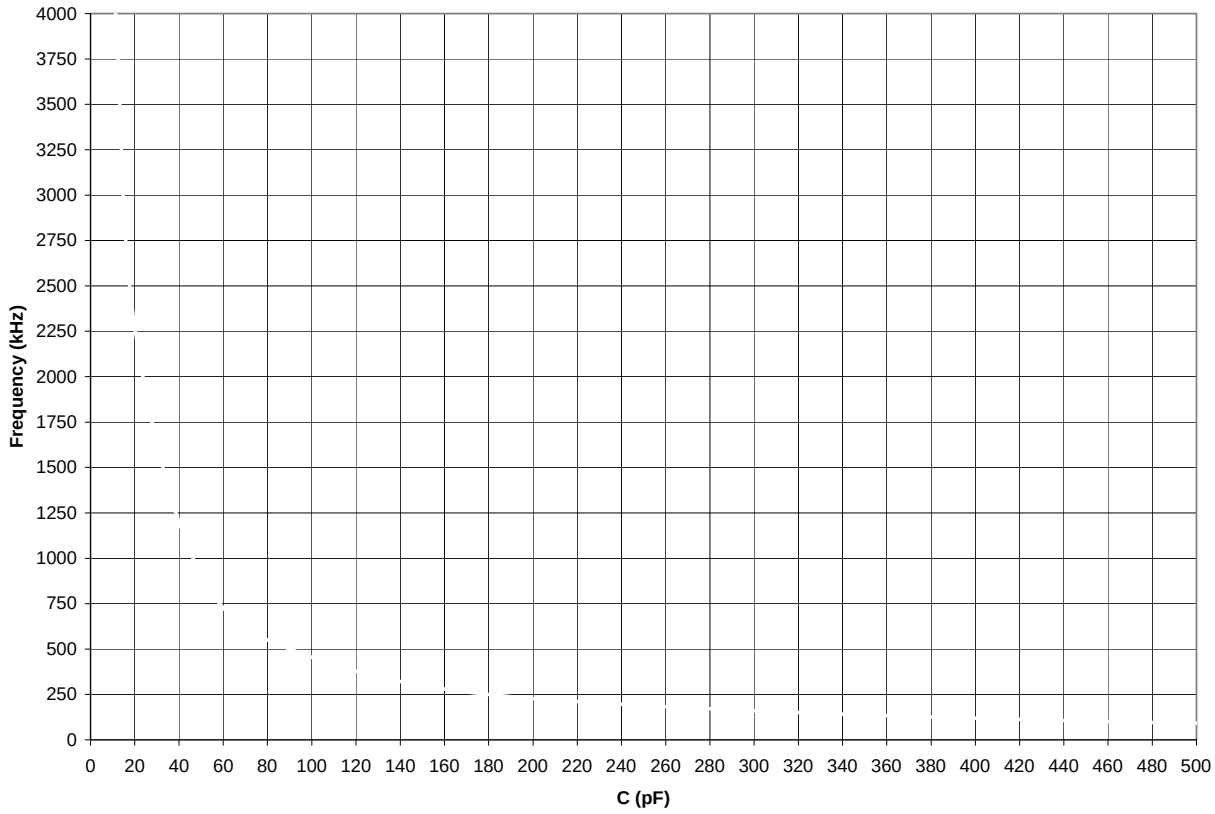

Figure 42. Typical RC Oscillator Frequency as a Function of the External Capacitance with a 45kΩ Resistor

Caution: When using the external RC oscillator mode, the oscillator may stop oscillating if the power supply drops below 2.7V, but before the power supply drops to the voltage brown-out threshold. The oscillator will resume oscillation as soon as the supply voltage exceeds 2.7V.

AC Characteristics

This section provides AC characteristics and timing data which assumes a standard load of 50 pF on all outputs. Table 114 lists the Z8 Encore! XP F64xx Series AC characteristics and timing.

Table 114. AC Characteristics

		V_{DD} = 3.0 V–3.6 V T_A = –40°C to 125°C			
Symbol	**Parameter**	**Minimum**	**Maximum**	**Units**	**Conditions**
F_{SYSCLK}	System Clock Frequency	–	20.0	MHz	Read-only from Flash memory.
		0.032768	20.0	MHz	Program or erasure of Flash memory.
F_{XTAL}	Crystal Oscillator Frequency	0.032768	20.0	MHz	System clock frequencies below the crystal oscillator minimum require an external clock driver.
T_{XIN}	Crystal Oscillator Clock Period	50	–	ns	$T_{CLK} = 1/F_{SYSCLK}$
T_{XINH}	System Clock High Time	20		ns	
T_{XINL}	System Clock Low Time	20		ns	
T_{XINR}	System Clock Rise Time	–	3	ns	T_{CLK} = 50 ns. Slower rise times can be tolerated with longer clock periods.
T_{XINF}	System Clock Fall Time	–	3	ns	T_{CLK} = 50 ns. Slower fall times can be tolerated with longer clock periods.

Table 131. CPU Control Instructions

Mnemonic	Operands	Instruction
ATM	—	Atomic Execution
CCF	—	Complement Carry Flag
DI	—	Disable Interrupts
EI	—	Enable Interrupts
HALT	—	HALT Mode
NOP	—	No Operation
RCF	—	Reset Carry Flag
SCF	—	Set Carry Flag
SRP	src	Set Register Pointer
STOP	—	STOP Mode
WDT	—	Watchdog Timer Refresh

Table 132. Load Instructions

Mnemonic	Operands	Instruction
CLR	dst	Clear
LD	dst, src	Load
LDC	dst, src	Load Constant to/from program memory
LDCI	dst, src	Load Constant to/from program memory and Auto-Increment addresses
LDE	dst, src	Load External Data to/from Data Memory
LDEI	dst, src	Load External Data to/from Data Memory and Auto-Increment addresses
LDWX	dst, src	Load Word using Extended Addressing
LDX	dst, src	Load using Extended Addressing
LEA	dst, X(src)	Load Effective Address
POP	dst	Pop
POPX	dst	Pop using Extended Addressing
PUSH	src	Push
PUSHX	src	Push using Extended Addressing

Table 133. Logical Instructions

Mnemonic	Operands	Instruction
AND	dst, src	Logical AND
ANDX	dst, src	Logical AND using Extended Addressing
COM	dst	Complement
OR	dst, src	Logical OR
ORX	dst, src	Logical OR using Extended Addressing
XOR	dst, src	Logical Exclusive OR
XORX	dst, src	Logical Exclusive OR using Extended Addressing

Table 134. Program Control Instructions

Mnemonic	Operands	Instruction
BRK	—	On-Chip Debugger Break
BTJ	p, bit, src, DA	Bit Test and Jump
BTJNZ	bit, src, DA	Bit Test and Jump if Non-Zero
BTJZ	bit, src, DA	Bit Test and Jump if Zero
CALL	dst	Call Procedure
DJNZ	dst, src, RA	Decrement and Jump Non-Zero
IRET	—	Interrupt Return
JP	dst	Jump
JP cc	dst	Jump Conditional
JR	DA	Jump Relative
JR cc	DA	Jump Relative Conditional
RET	—	Return
TRAP	vector	Software Trap

Hex Addresses: FC9–FCC

This address range is reserved.

Hex Address: FCD

Table 226. Interrupt Edge Select Register (IRQES)

Bit	7	6	5	4	3	2	1	0
Field	IES7	IES6	IES5	IES4	IES3	IES2	IES1	IES0
RESET	0							
R/W	R/W							
Address	FCDH							

Hex Address: FCE

Table 227. Interrupt Port Select Register (IRQPS)

Bit	7	6	5	4	3	2	1	0
Field	PAD7S	PAD6S	PAD5S	PAD4S	PAD3S	PAD2S	PAD1S	PAD0S
RESET	0							
R/W	R/W							
Address	FCEH							

Hex Address: FCF

Table 228. Interrupt Control Register (IRQCTL)

Bit	7	6	5	4	3	2	1	0
Field	IRQE	Reserved						
RESET	0							
R/W	R/W	R						
Address	FCFH							

Table 271. Z8 Encore! XP F64xx Series Ordering Matrix

Part Number	Flash	RAM	I/O Lines	Interrupts	16-Bit Timers w/PWM	10-Bit A/D Channels	I^2C	SPI	UARTs with IrDA	Description
Z8F482x with 48KB Flash, 10-Bit Analog-to-Digital Converter										
Standard Temperature: 0°C to 70°C										
Z8F4821PM020SG	48KB	4KB	29	23	3	8	1	1	2	PDIP 40-pin package
Z8F4821AN020SG	48KB	4KB	31	23	3	8	1	1	2	LQFP 44-pin package
Z8F4821VN020SG	48KB	4KB	31	23	3	8	1	1	2	PLCC 44-pin package
Z8F4822AR020SG	48KB	4KB	46	24	4	12	1	1	2	LQFP 64-pin package
Z8F4822VS020SG	48KB	4KB	46	24	4	12	1	1	2	PLCC 68-pin package
Z8F4823FT020SG	48KB	4KB	60	24	4	12	1	1	2	QFP 80-pin package
Extended Temperature: –40°C to +105°C										
Z8F4821PM020EG	48KB	4KB	29	23	3	8	1	1	2	PDIP 40-pin package
Z8F4821AN020EG	48KB	4KB	31	23	3	8	1	1	2	LQFP 44-pin package
Z8F4821VN020EG	48KB	4KB	31	23	3	8	1	1	2	PLCC 44-pin package
Z8F4822AR020EG	48KB	4KB	46	24	4	12	1	1	2	LQFP 64-pin package
Z8F4822VS020EG	48KB	4KB	46	24	4	12	1	1	2	PLCC 68-pin package
Z8F4823FT020EG	48KB	4KB	60	24	4	12	1	1	2	QFP 80-pin package
Automotive/Industrial Temperature: –40°C to +125°C										
Z8F4821PM020AG	48KB	4KB	29	23	3	8	1	1	2	PDIP 40-pin package
Z8F4821AN020AG	48KB	4KB	31	23	3	8	1	1	2	LQFP 44-pin package
Z8F4821VN020AG	48KB	4KB	31	23	3	8	1	1	2	PLCC 44-pin package
Z8F4822AR020AG	48KB	4KB	46	24	4	12	1	1	2	LQFP 64-pin package
Z8F4822VS020AG	48KB	4KB	46	24	4	12	1	1	2	PLCC 68-pin package
Z8F4823FT020AG	48KB	4KB	60	24	4	12	1	1	2	QFP 80-pin package

Table 271. Z8 Encore! XP F64xx Series Ordering Matrix

Part Number	Flash	RAM	I/O Lines	Interrupts	16-Bit Timers w/PWM	10-Bit A/D Channels	I^2C	SPI	UARTs with IrDA	Description
Z8F242x with 24KB Flash, 10-Bit Analog-to-Digital Converter										
Standard Temperature: 0°C to 70°C										
Z8F2421PM020SG	24KB	2KB	29	23	3	8	1	1	2	PDIP 40-pin package
Z8F2421AN020SG	24KB	2KB	31	23	3	8	1	1	2	LQFP 44-pin package
Z8F2421VN020SG	24KB	2KB	31	23	3	8	1	1	2	PLCC 44-pin package
Z8F2422AR020SG	24KB	2KB	46	24	4	12	1	1	2	LQFP 64-pin package
Z8F2422VS020SG	24KB	2KB	46	24	4	12	1	1	2	PLCC 68-pin package
Extended Temperature: –40°C to 105°C										
Z8F2421PM020EG	24KB	2KB	29	23	3	8	1	1	2	PDIP 40-pin package
Z8F2421AN020EG	24KB	2KB	31	23	3	8	1	1	2	LQFP 44-pin package
Z8F2421VN020EG	24KB	2KB	31	23	3	8	1	1	2	PLCC 44-pin package
Z8F2422AR020EG	24KB	2KB	46	24	4	12	1	1	2	LQFP 64-pin package
Z8F2422VS020EG	24KB	2KB	46	24	4	12	1	1	2	PLCC 68-pin package
Automotive/Industrial Temperature: –40°C to 125°C										
Z8F2421PM020AG	24KB	2KB	29	23	3	8	1	1	2	PDIP 40-pin package
Z8F2421AN020AG	24KB	2KB	31	23	3	8	1	1	2	LQFP 44-pin package
Z8F2421VN020AG	24KB	2KB	31	23	3	8	1	1	2	PLCC 44-pin package
Z8F2422AR020AG	24KB	2KB	46	24	4	12	1	1	2	LQFP 64-pin package
Z8F2422VS020AG	24KB	2KB	46	24	4	12	1	1	2	PLCC 68-pin package

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