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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | eZ8 |
| Core Size | 8-Bit |
| Speed | 20MHz |
| Connectivity | I²C, IrDA, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, DMA, POR, PWM, WDT |
| Number of I/O | 46 |
| Program Memory Size | 32KB (32K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 2K x 8 |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 3.6V |
| Data Converters | A/D 12x10b |
| Oscillator Type | Internal |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 68-LCC (J-Lead) |
| Supplier Device Package | - |
| Purchase URL | https://www.e-xfl.com/product-detail/zilog/z8f3222vs020sg |

# List of Tables

# Signal Descriptions

Table 3 lists the Z8 Encore! XP signals. To determine the available signals for a specific package style, see the Pin Configurations section on page 8.

**Table 3. Signal Descriptions**

| Signal Mnemonic | I/O | Description |
|---|---|---|
| **General-Purpose I/O Ports A–H** | | |
| PA[7:0] | I/O | Port A[7:0]. These pins are used for general-purpose I/O and support 5V-tolerant inputs. |
| PB[7:0] | I/O | Port B[7:0]. These pins are used for general-purpose I/O. |
| PC[7:0] | I/O | Port C[7:0]. These pins are used for general-purpose I/O. These pins are used for general-purpose I/O and support 5V-tolerant inputs |
| PD[7:0] | I/O | Port D[7:0]. These pins are used for general-purpose I/O. These pins are used for general-purpose I/O and support 5V-tolerant inputs |
| PE[7:0] | I/O | Port E[7:0]. These pins are used for general-purpose I/O. These pins are used for general-purpose I/O and support 5V-tolerant inputs. |
| PF[7:0] | I/O | Port F[7:0]. These pins are used for general-purpose I/O. These pins are used for general-purpose I/O and support 5V-tolerant inputs. |
| PG[7:0] | I/O | Port G[7:0]. These pins are used for general-purpose I/O. These pins are used for general-purpose I/O and support 5V-tolerant inputs. |
| PH[3:0] | I/O | Port H[3:0]. These pins are used for general-purpose I/O. |
| **$I^2C$ Controller** | | |
| SCL | O | Serial Clock. This is the output clock for the $I^2C$. This pin is multiplexed with a general-purpose I/O pin. When the general-purpose I/O pin is configured for alternate function to enable the SCL function, this pin is open-drain. |
| SDA | I/O | Serial Data. This open-drain pin transfers data between the $I^2C$ and a slave. This pin is multiplexed with a general-purpose I/O pin. When the general-purpose I/O pin is configured for alternate function to enable the SDA function, this pin is open-drain. |
| **SPI Controller** | | |
| $\overline{SS}$ | I/O | Slave Select. This signal can be an output or an input. If the Z8 Encore! XP F64xx Series is the SPI master, this pin may be configured as the Slave Select output. If the Z8 Encore! XP F64xx Series is the SPI slave, this pin is the input slave select. It is multiplexed with a general-purpose I/O pin. |
| SCK | I/O | SPI Serial Clock. The SPI master supplies this pin. If the Z8 Encore! XP F64xx Series is the SPI master, this pin is an output. If the Z8 Encore! XP F64xx Series is the SPI slave, this pin is an input. It is multiplexed with a general-purpose I/O pin. |

**Table 31. IRQ1 Enable High Bit Register (IRQ1ENH)**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | PAD7ENH | PAD6ENH | PAD5ENH | PAD4ENH | PAD3ENH | PAD2ENH | PAD1ENH | PAD0ENH |
| RESET | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Address | FC4H | | | | | | | |

| Bit | Description |
|---|---|
| [7:0] PADxENH | **Port A or Port D Bit[*x*] Interrupt Request Enable High Bit**<br>To select either Port A or Port D as the interrupt source, see the Interrupt Port Select Register on page 60. |

Note: *x* indicates register bits in the range [7:0].

**Table 32. IRQ1 Enable Low Bit Register (IRQ1ENL)**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | PAD7ENL | PAD6ENL | PAD5ENL | PAD4ENL | PAD3ENL | PAD2ENL | PAD1ENL | PAD0ENL |
| RESET | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Address | FC5H | | | | | | | |

| Bit | Description |
|---|---|
| [7:0] PADxENL | **Port A or Port D Bit[*x*] Interrupt Request Enable Low Bit**<br>To select either Port A or Port D as the interrupt source, see the Interrupt Port Select Register on page 60. |

Note: *x* indicates register bits in the range [7:0].

unlock the Watchdog Timer Reload Byte registers (WDTU, WDTH, and WDTL) for write access.

1. Write 55H to the Watchdog Timer Control Register (WDTCTL).
2. Write AAH to the Watchdog Timer Control Register (WDTCTL).
3. Write the Watchdog Timer Reload Upper Byte Register (WDTU).
4. Write the Watchdog Timer Reload High Byte Register (WDTH).
5. Write the Watchdog Timer Reload Low Byte Register (WDTL).

All steps of the Watchdog Timer reload unlock sequence must be written in the sequence described above; there must be no other register writes between each of these operations. If a register write occurs, the lock state machine resets and no further writes can occur, unless the sequence is restarted. The value in the Watchdog Timer Reload registers is loaded into the counter when the Watchdog Timer is first enabled and every time a WDT instruction is executed.

# Watchdog Timer Control Register Definitions

This section defines the features of the following Watchdog Timer Control registers.

Watchdog Timer Control Register: see page 83

Watchdog Timer Reload Upper, High and Low Byte Registers: see page 85

## Watchdog Timer Control Register

The Watchdog Timer Control (WDTCTL) Register, shown in Table 48, is a read-only register that indicates the source of the most recent Reset event, indicates a Stop Mode Recovery event, and indicates a Watchdog Timer time-out. Reading this register resets the upper four bits to 0.

Writing the 55H, AAH unlock sequence to the Watchdog Timer Control (WDTCTL) Register address unlocks the three Watchdog Timer Reload Byte registers (WDTU, WDTH, and WDTL) to allow changes to the time-out period. These write operations to the WDTCTL Register address produce no effect on the bits in the WDTCTL Register. The locking mechanism prevents spurious writes to the Reload registers.

# Serial Peripheral Interface

The Serial Peripheral Interface is a synchronous interface allowing several SPI-type devices to be interconnected. SPI-compatible devices include EEPROMs, Analog-to-Digital Converters, and ISDN devices. Features of the SPI include:

- Full-duplex, synchronous, character-oriented communication
- Four-wire interface
- Data transfers rates up to a maximum of one-half the system clock frequency
- Error detection
- Dedicated Baud Rate Generator

## Architecture

The SPI may be configured as either a Master (in single or multimaster systems) or a Slave as displayed in Figures 22 through 24.

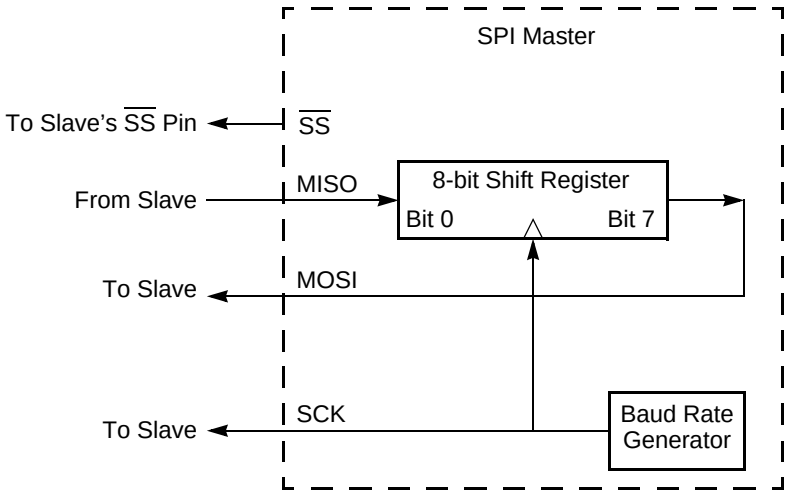



**Figure 22. SPI Configured as a Master in a Single-Master, Single-Slave System**

**Table 64. SPI Data Register (SPIDATA)**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | DATA | | | | | | | |
| RESET | X | | | | | | | |
| R/W | R/W | | | | | | | |
| Address | F60H | | | | | | | |

| Bit | Description |
|---|---|
| [7:0]<br>DATA | **Data**<br>Transmit and/or receive data. |

## SPI Control Register

The SPI Control Register, shown in Table 65, configures the SPI for transmit and receive operations.

**Table 65. SPI Control Register (SPICTL)**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | IRQE | STR | BIRQ | PHASE | CLKPOL | WOR | MMEN | SPIEN |
| RESET | 0 | | | | | | | |
| R/W | R/W | | | | | | | |
| Address | F61H | | | | | | | |

| Bit | Description |
|---|---|
| [7]<br>IRQE | **Interrupt Request Enable**<br>0 = SPI interrupts are disabled. No interrupt requests are sent to the Interrupt Controller.<br>1 = SPI interrupts are enabled. Interrupt requests are sent to the Interrupt Controller. |
| [6]<br>STR | **Start an SPI Interrupt Request**<br>0 = No effect.<br>1 = Setting this bit to 1 also sets the IRQ bit in the SPI Status Register to 1. Setting this bit forces the SPI to send an interrupt request to the Interrupt Control. This bit can be used by software for a function similar to transmit buffer empty in a UART. Writing a 1 to the IRQ bit in the SPI Status Register clears this bit to 0. |
| [5]<br>BIRQ | **BRG Timer Interrupt Request**<br>If the SPI is enabled, this bit has no effect. If the SPI is disabled:<br>0 = The Baud Rate Generator timer function is disabled.<br>1 = The Baud Rate Generator timer function and time-out interrupt are enabled. |

**Table 71. I²C Data Register (I2CDATA)**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | DATA | | | | | | | |
| RESET | 0 | | | | | | | |
| R/W | R/W | | | | | | | |
| Address | F50H | | | | | | | |

## I²C Status Register

The read-only I²C Status Register, shown in Table 72, indicates the status of the I²C Controller.

**Table 72. I²C Status Register (I2CSTAT)**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | TDRE | RDRF | ACK | 10B | RD | TAS | DSS | NCKI |
| RESET | 1 | 0 | | | | | | |
| R/W | R | | | | | | | |
| Address | F51H | | | | | | | |

| Bit | Description |
|---|---|
| [7]<br>TDRE | **Transmit Data Register Empty**<br>When the I²C Controller is enabled, this bit is 1 when the I²C Data Register is empty. When this bit is set, an interrupt is generated if the TXI bit is set, except when the I²C Controller is shifting in data during the reception of a byte or when shifting an address and the RD bit is set. This bit is cleared by writing to the I2CDATA Register. |
| [6]<br>RDRF | **Receive Data Register Full**<br>This bit is set = 1 when the I²C Controller is enabled and the I²C Controller has received a byte of data. When asserted, this bit causes the I²C Controller to generate an interrupt. This bit is cleared by reading the I²C Data Register (unless the read is performed using execution of the On-Chip Debugger's Read Register command). |

## DMA_ADC Address Register

The DMA_ADC Address Register, shown in Table 84, points to a block of the Register File to store the ADC conversion values displayed in Table 83. This register contains the seven most significant bits of the 12-bit Register File addresses. The five least significant bits are calculated from the ADC analog input number (5-bit base address is equal to twice the ADC analog input number). The 10-bit ADC conversion data is stored as two bytes with the most significant byte of the ADC data stored at the even-numbered Register File address.

Table 83 provides an example of the Register File addresses if the DMA_ADC Address Register contains the value 72H.

**Table 83. DMA_ADC Register File Address Example**

| ADC Analog Input | Register File Address (Hex)* |
|---|---|
| 0 | 720H–721H |
| 1 | 722H–723H |
| 2 | 724H–725H |
| 3 | 726H–727H |
| 4 | 728H–729H |
| 5 | 72AH–72BH |
| 6 | 72CH–72DH |
| 7 | 72EH–72FH |
| 8 | 730H–731H |
| 9 | 732H–733H |
| 10 | 734H–735H |
| 11 | 736H–737H |

Note: *DMAA_ADDR is set to 72H.

| Bit | Description (Continued) |
|---|---|
| [2]<br>IRQA | **DMA_ADC Interrupt Request Indicator**<br>This bit is automatically reset to 0 each time a read from this register occurs.<br>0 = DMA_ADC is not the source of the interrupt from the DMA Controller.<br>1 = DMA_ADC completed transfer of data from the last ADC analog input and generated an interrupt. |
| [1]<br>IRQ1 | **DMA1 Interrupt Request Indicator**<br>This bit is automatically reset to 0 each time a read from this register occurs.<br>0 = DMA1 is not the source of the interrupt from the DMA Controller.<br>1 = DMA1 completed transfer of data to/from the End Address and generated an interrupt. |
| [0]<br>IRQ0 | **DMA0 Interrupt Request Indicator**<br>This bit is automatically reset to 0 each time a read from this register occurs.<br>0 = DMA0 is not the source of the interrupt from the DMA Controller.<br>1 = DMA0 completed transfer of data to/from the End Address and generated an interrupt. |

## Flash Read Protection

The user code contained within Flash memory can be protected from external access. Programming the Flash Read Protect option bit prevents reading of user code by the On-Chip Debugger or by using the Flash Controller Bypass mode. For more information, see the Option Bits chapter on page 180 and the On-Chip Debugger chapter on page 183.

## Flash Write/Erase Protection

The Z8 Encore! XP F64xx Series provides several levels of protection against accidental program and erasure of the Flash memory contents. This protection is provided by the Flash Controller unlock mechanism, the Flash Sector Protect Register, and the Flash Write Protect option bit.

### Flash Controller Unlock Mechanism

At Reset, the Flash Controller locks to prevent accidental program or erasure of Flash memory. To program or erase Flash memory, the Flash Controller must be unlocked. After unlocking the Flash Controller, the Flash can be programmed or erased. Any value written by user code to the Flash Control Register or Page Select Register out of sequence will lock the Flash Controller.

Observe the following procedure to unlock the Flash Controller from user code:

1. Write 00H to the Flash Control Register to reset the Flash Controller.
2. Write the page to be programmed or erased to the Page Select Register.
3. Write the first unlock command 73H to the Flash Control Register.
4. Write the second unlock command 8CH to the Flash Control Register.
5. Rewrite the page written in Step 2 to the Page Select Register.

### Flash Sector Protection

The Flash Sector Protect Register can be configured to prevent sectors from being programmed or erased. After a sector is protected, it cannot be unprotected by user code. The Flash Sector Protect Register is cleared after reset and any previously written protection values is lost. User code must write this register in their initialization routine if they want to enable sector protection.

The Flash Sector Protect Register shares its Register File address with the Page Select Register. The Flash Sector Protect Register is accessed by writing the Flash Control Register with 5EH. After the Flash Sector Protect Register is selected, it can be accessed at the Page Select Register address. When user code writes the Flash Sector Protect Register, bits can only be set to 1. Thus, sectors can be protected, but not unprotected, via register write operations. Writing a value other than 5EH to the Flash Control Register deselects the Flash Sector Protect Register and reenables access to the Page Select Register.

- Voltage Brown-Out reset
- Asserting the $\overline{\text{RESET}}$ pin Low to initiate a Reset
- Driving the DBG pin Low while the device is in STOP Mode initiates a system reset

## OCD Data Format

The OCD interface uses the asynchronous data format defined for RS-232. Each character is transmitted as 1 start bit, 8 data bits (least significant bit first), and 1 stop bit, as shown in Figure 39.

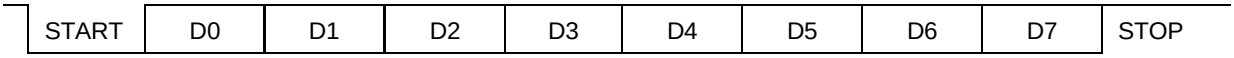



**Figure 39. OCD Data Format**

## OCD Autobaud Detector/Generator

To run over a range of baud rates (bits per second) with various system clock frequencies, the On-Chip Debugger has an Autobaud Detector/Generator. After a reset, the OCD is idle until it receives data. The OCD requires that the first character sent from the host is the character 80H. The character 80H has eight continuous bits Low (one start bit plus 7 data bits). The Autobaud Detector measures this period and sets the OCD Baud Rate Generator accordingly.

The Autobaud Detector/Generator is clocked by the system clock. The minimum baud rate is the system clock frequency divided by 512. For optimal operation, the maximum recommended baud rate is the system clock frequency divided by 8. The theoretical maximum baud rate is the system clock frequency divided by 4. This theoretical maximum is possible for low noise designs with clean signals. Table 101 lists minimum and recommended maximum baud rates for sample crystal frequencies.

**Table 101. OCD Baud-Rate Limits**

| System Clock Frequency (MHz) | Recommended Maximum Baud Rate (kbits/s) | Minimum Baud Rate (kbits/s) |
|---|---|---|
| 20.0 | 2500 | 39.1 |
| 1.0 | 125.0 | 1.96 |
| 0.032768 (32kHz) | 4.096 | 0.064 |

Figure 48 displays the maximum current consumption in STOP Mode with the VBO disabled and Watchdog Timer enabled plotted opposite the power supply voltage. All GPIO pins are configured as outputs and driven High. Disabling the Watchdog Timer and its internal RC oscillator in STOP Mode will provide some additional reduction in STOP Mode current consumption. This small current reduction would be indistinguishable on the scale shown in the figure.

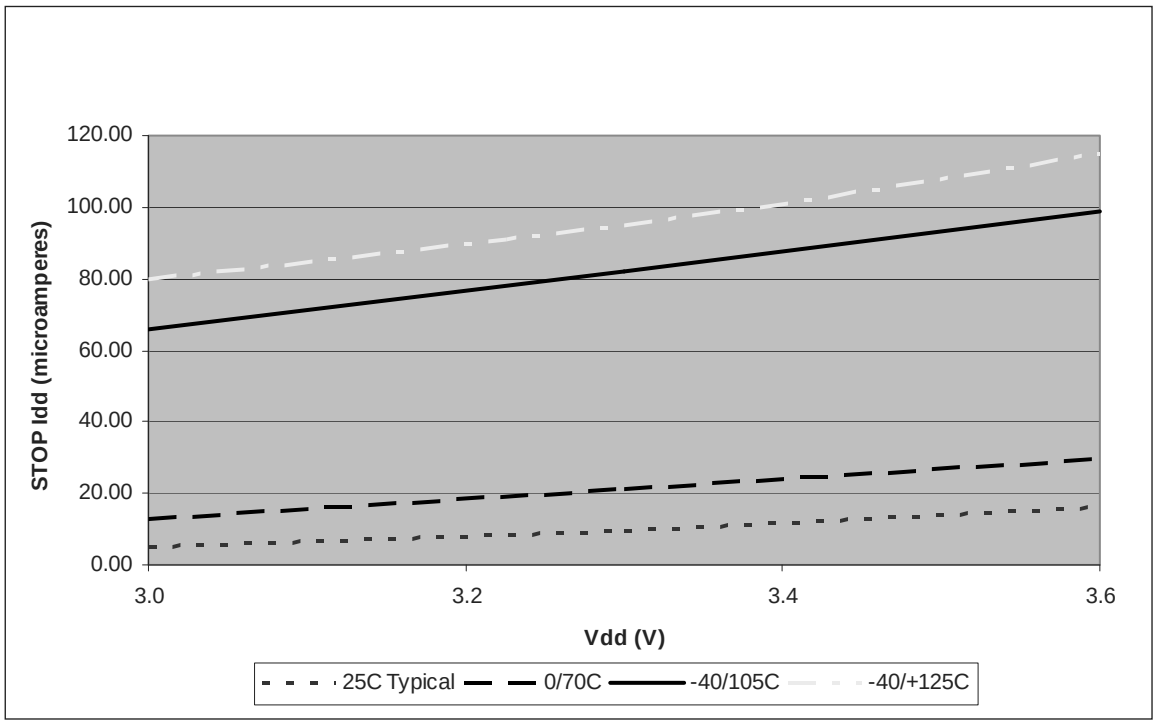



**Figure 48. Maximum STOP Mode $I_{DD}$ with VBO Disabled vs. Power Supply Voltage**

**Table 109. External RC Oscillator Electrical Characteristics and Timing**

| | | $T_A$ = –40°C to 125°C | | | | |
|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Minimum** | **Typical*** | **Maximum** | **Units** | **Conditions** |
| $V_{DD}$ | Operating Voltage Range | 2.70[1] | – | – | V | |
| $R_{EXT}$ | External Resistance from $X_{IN}$ to $V_{DD}$ | 40 | 45 | 200 | kΩ | $V_{DD} = V_{VBO}$ |
| $C_{EXT}$ | External Capacitance from $X_{IN}$ to $V_{SS}$ | 0 | 20 | 1000 | pF | |
| $F_{OSC}$ | External RC Oscillation Frequency | – | – | 4 | MHz | |

Note: *When using the external RC oscillator mode, the oscillator may stop oscillating if the power supply drops below 2.7V, but before the power supply drops to the voltage brown-out threshold. The oscillator will resume oscillation as soon as the supply voltage exceeds 2.7V.

**Table 110. Reset and Stop Mode Recovery Pin Timing**

| | | $T_A$ = –40°C to 125°C | | | | |
|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Minimum** | **Typical** | **Maximum** | **Units** | **Conditions** |
| $T_{RESET}$ | $\overline{\text{RESET}}$ pin assertion to initiate a system reset. | 4 | – | – | $T_{CLK}$ | Not in STOP Mode. $T_{CLK}$ = System Clock period. |
| $T_{SMR}$ | Stop Mode Recovery pin Pulse Rejection Period | 10 | 20 | 40 | ns | RESET, DBG, and GPIO pins configured as SMR sources. |

# I²C Timing

Figure 55 and Table 120 provide timing information for I²C pins.

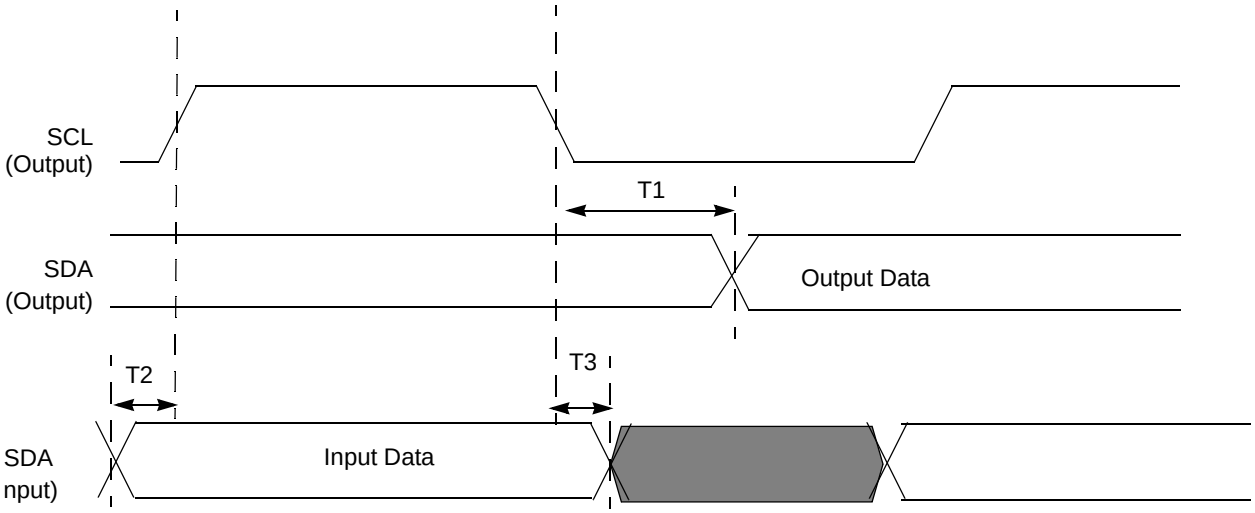
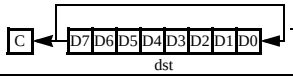
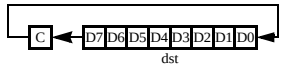
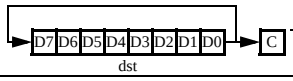
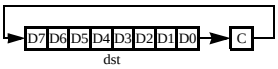



**Figure 55. I²C Timing**

**Table 120. I²C Timing**

| | | Delay (ns) | |
|---|---|---|---|
| **Parameter** | **Abbreviation** | **Minimum** | **Maximum** |
| **I²C** | | | |
| $T_1$ | SCL Fall to SDA output delay | SCL period/4 | |
| $T_2$ | SDA Input to SCL rising edge Setup Time | 0 | |
| $T_3$ | SDA Input to SCL falling edge Hold Time | 0 | |

**Table 136. eZ8 CPU Instruction Summary (Continued)**

| Assembly Mnemonic | Symbolic Operation | Address Mode dst | Address Mode src | Opcode(s) (Hex) | Flags C | Z | S | V | D | H | Fetch Cycles | Instr. Cycles |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| POPX dst | dst ← @SP<br>SP ← SP + 1 | ER | | D8 | – | – | – | – | – | – | 3 | 2 |
| PUSH src | SP ← SP – 1<br>@SP ← src | R | | 70 | – | – | – | – | – | – | 2 | 2 |
| | | IR | | 71 | | | | | | | 2 | 3 |
| | | IM | | 1F 70 | | | | | | | 3 | 2 |
| PUSHX src | SP ← SP – 1<br>@SP ← src | ER | | C8 | – | – | – | – | – | – | 3 | 2 |
| RCF | C ← 0 | | | CF | 0 | – | – | – | – | – | 1 | 2 |
| RET | PC ← @SP<br>SP ← SP + 2 | | | AF | – | – | – | – | – | – | 1 | 4 |
| RL dst |  | R | | 90 | * | * | * | * | – | – | 2 | 2 |
| | | IR | | 91 | | | | | | | 2 | 3 |
| RLC dst |  | R | | 10 | * | * | * | * | – | – | 2 | 2 |
| | | IR | | 11 | | | | | | | 2 | 3 |
| RR dst |  | R | | E0 | * | * | * | * | – | – | 2 | 2 |
| | | IR | | E1 | | | | | | | 2 | 3 |
| RRC dst |  | R | | C0 | * | * | * | * | – | – | 2 | 2 |
| | | IR | | C1 | | | | | | | 2 | 3 |
| SBC dst, src | dst ← dst – src – C | r | r | 32 | * | * | * | * | 1 | * | 2 | 3 |
| | | r | Ir | 33 | | | | | | | 2 | 4 |
| | | R | R | 34 | | | | | | | 3 | 3 |
| | | R | IR | 35 | | | | | | | 3 | 4 |
| | | R | IM | 36 | | | | | | | 3 | 3 |
| | | IR | IM | 37 | | | | | | | 3 | 4 |
| SBCX dst, src | dst ← dst – src – C | ER | ER | 38 | * | * | * | * | 1 | * | 4 | 3 |
| | | ER | IM | 39 | | | | | | | 4 | 3 |
| SCF | C ← 1 | | | DF | 1 | – | – | – | – | – | 1 | 2 |

Note: Flags Notation:
* = Value is a function of the result of the operation.
– = Unaffected.
X = Undefined.
0 = Reset to 0.
1 = Set to 1.

### Hex Address: F09

**Table 147. Timer 0–3 Low Byte Register (TxL)**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | TL | | | | | | | |
| RESET | 0 | | | | | | | 1 |
| R/W | R/W | | | | | | | |
| Address | F01H, F09H, F11H, F19H | | | | | | | |

### Hex Address: F0A

**Table 148. Timer 0–3 Reload High Byte Register (TxRH)**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | TRH | | | | | | | |
| RESET | 1 | | | | | | | |
| R/W | R/W | | | | | | | |
| Address | F02H, F0AH, F12H, F1AH | | | | | | | |

### Hex Address: F0B

**Table 149. Timer 0–3 Reload Low Byte Register (TxRL)**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | TRL | | | | | | | |
| RESET | 1 | | | | | | | |
| R/W | R/W | | | | | | | |
| Address | F03H, F0BH, F13H, F1BH | | | | | | | |

### Hex Address: F0C

**Table 150. Timer 0–3 PWM High Byte Register (TxPWMH)**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | PWMH | | | | | | | |
| RESET | 0 | | | | | | | |
| R/W | R/W | | | | | | | |
| Address | F04H, F0CH, F14H, F1CH | | | | | | | |

### Hex Address: F19

**Table 163. Timer 0–3 Low Byte Register (TxL)**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | TL | | | | | | | |
| RESET | 0 | | | | | | | 1 |
| R/W | R/W | | | | | | | |
| Address | F01H, F09H, F11H, F19H | | | | | | | |

### Hex Address: F1A

**Table 164. Timer 0–3 Reload High Byte Register (TxRH)**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | TRH | | | | | | | |
| RESET | 1 | | | | | | | |
| R/W | R/W | | | | | | | |
| Address | F02H, F0AH, F12H, F1AH | | | | | | | |

### Hex Address: F1B

**Table 165. Timer 0–3 Reload Low Byte Register (TxRL)**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | TRL | | | | | | | |
| RESET | 1 | | | | | | | |
| R/W | R/W | | | | | | | |
| Address | F03H, F0BH, F13H, F1BH | | | | | | | |

### Hex Address: F1C

**Table 166. Timer 0–3 PWM High Byte Register (TxPWMH)**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | PWMH | | | | | | | |
| RESET | 0 | | | | | | | |
| R/W | R/W | | | | | | | |
| Address | F04H, F0CH, F14H, F1CH | | | | | | | |

### Hex Address: F55

**Table 193. I²C Diagnostic State Register (I2CDST)**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | SCLIN | SDAIN | STPCNT | TXRXSTATE | | | | |
| RESET | X | | 0 | | | | | |
| R/W | R | | | | | | | |
| Address | F55H | | | | | | | |

### Hex Address: F56

**Table 194. I²C Diagnostic Control Register (I2CDIAG)**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | Reserved | | | | | | | DIAG |
| RESET | 0 | | | | | | | |
| R/W | R | | | | | | | R/W |
| Address | F56H | | | | | | | |

### Hex Addresses: F57–F5F

This address range is reserved.

## Serial Peripheral Interface

For more information about these SPI Control registers, see the SPI Control Register Definitions section on page 121.

### Hex Address: F60

**Table 195. SPI Data Register (SPIDATA)**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | DATA | | | | | | | |
| RESET | X | | | | | | | |
| R/W | R/W | | | | | | | |
| Address | F60H | | | | | | | |

# Analog-to-Digital Converter (ADC)

For more information about these ADC Control registers, see the ADC Control Register Definitions section on page 165.

### Hex Addresses: F70–F71

This address range is reserved.

### Hex Address: F72

**Table 202. ADC Data High Byte Register (ADCD_H)**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | ADCD_H | | | | | | | |
| RESET | X | | | | | | | |
| R/W | R | | | | | | | |
| Address | F72H | | | | | | | |

### Hex Address: F73

**Table 203. ADC Data Low Bits Register (ADCD_L)**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | ADCD_L | | Reserved | | | | | |
| RESET | X | | | | | | | |
| R/W | R | | | | | | | |
| Address | F73H | | | | | | | |

### Hex Addresses: F74–FAF

This address range is reserved.

# Direct Memory Access (DMA)

For more information about these DMA Control registers, see the DMA Control Register Definitions section on page 152.

## V



## W



## X



## Z