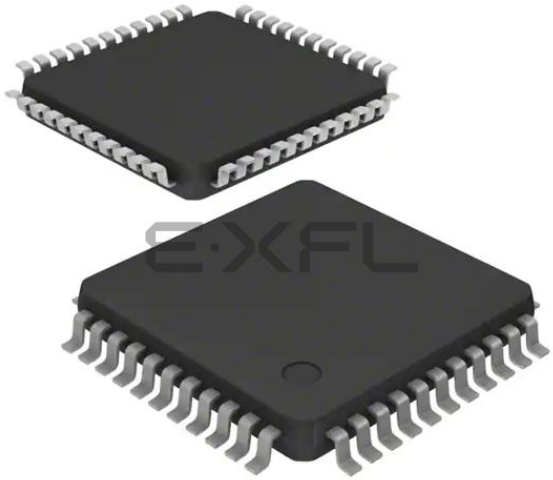

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	eZ8
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	31
Program Memory Size	48KB (48K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LQFP
Supplier Device Package	44-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8f4821an020eg

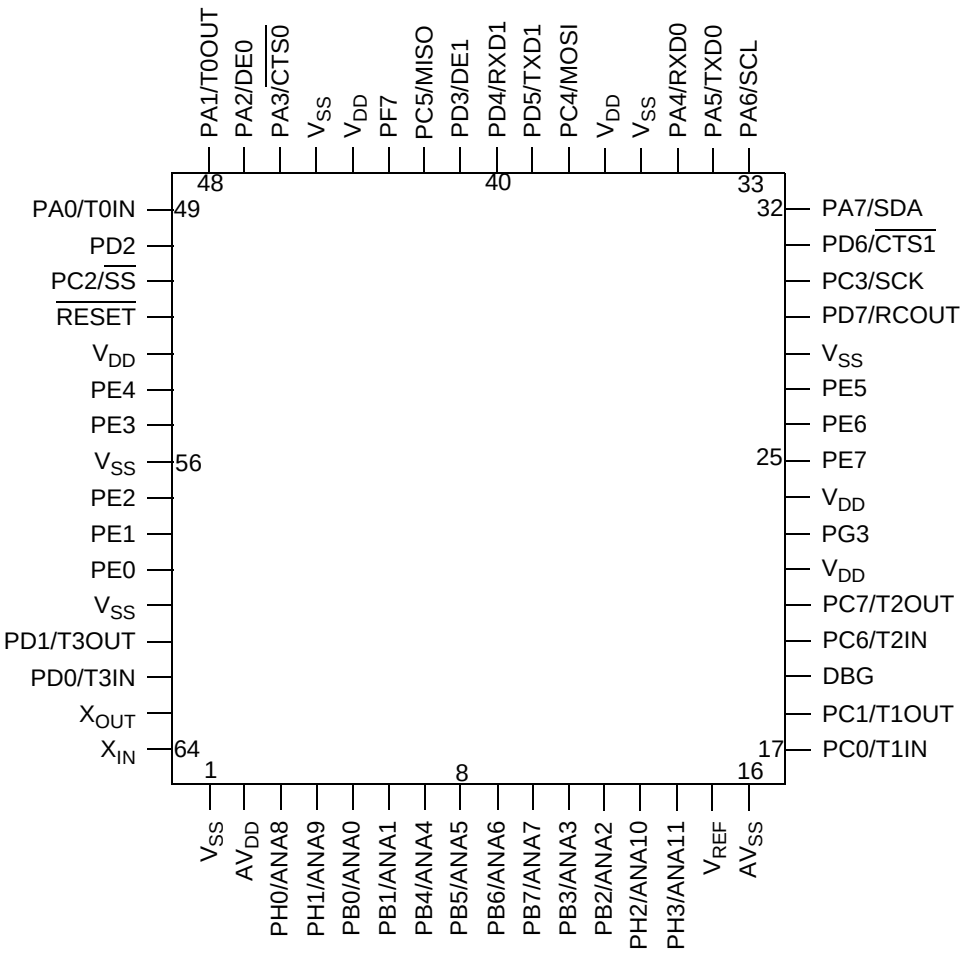

Figure 5. Z8 Encore! XP F64xx Series in 64-Pin Low-Profile Quad Flat Package (LQFP)

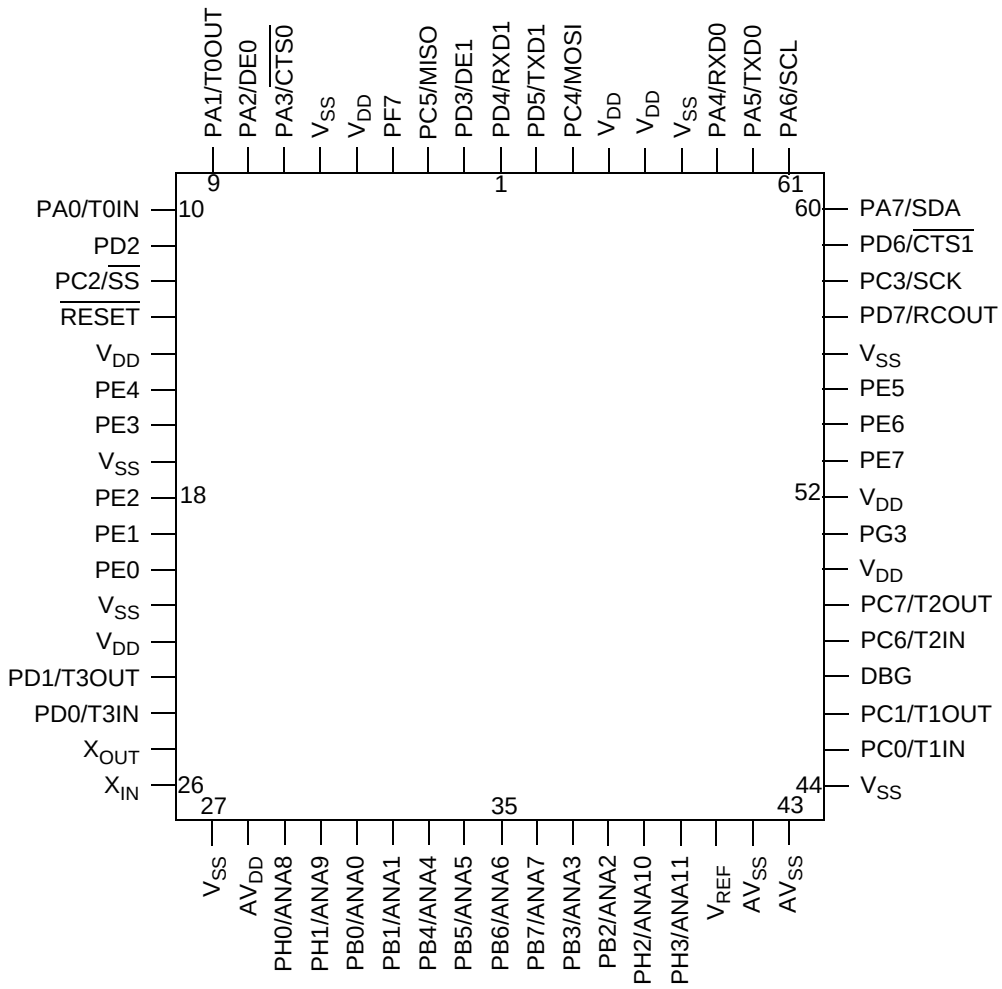

Figure 6. Z8 Encore! XP F64xx Series in 68-Pin Plastic Leaded Chip Carrier (PLCC)

Table 12. Port Alternate Function Mapping

Port	Pin	Mnemonic	Alternate Function Description
Port A	PA0	T0IN	Timer 0 Input
	PA1	T0OUT	Timer 0 Output
	PA2	DE0	UART 0 Driver Enable
	PA3	$\overline{\text{CTS0}}$	$\overline{\text{UART 0 Clear to Send}}$
	PA4	RXD0/IRRX0	UART 0/IrDA 0 Receive Data
	PA5	TXD0/IRTX0	UART 0/IrDA 0 Transmit Data
	PA6	SCL	I^2C Clock (automatically open-drain)
	PA7	SDA	I^2C Data (automatically open-drain)
Port B	PB0	ANA0	ADC analog input 0
	PB1	ANA1	ADC analog input 1
	PB2	ANA2	ADC analog input 2
	PB3	ANA3	ADC analog input 3
	PB4	ANA4	ADC analog input 4
	PB5	ANA5	ADC analog input 5
	PB6	ANA6	ADC analog input 6
	PB7	ANA7	ADC analog input 7
Port C	PC0	T1IN	Timer 1 Input
	PC1	T1OUT	Timer 1 Output
	PC2	$\overline{\text{SS}}$	$\overline{\text{SPI Slave Select}}$
	PC3	SCK	SPI Serial Clock
	PC4	MOSI	SPI Master Out/Slave In
	PC5	MISO	SPI Master In/Slave Out
	PC6	T2IN	Timer 2 In
	PC7	T2OUT	Timer 2 Out
Port D	PD0	T3IN	Timer 3 In (unavailable in the 44-pin package)
	PD1	T3OUT	Timer 3 Out (unavailable in the 44-pin package)
	PD2	N/A	No alternate function
	PD3	DE1	UART 1 Driver Enable
	PD4	RXD1/IRRX1	UART 1/IrDA 1 Receive Data
	PD5	TXD1/IRTX1	UART 1/IrDA 1 Transmit Data
	PD6	$\overline{\text{CTS1}}$	$\overline{\text{UART 1 Clear to Send}}$
	PD7	RCOUT	Watchdog Timer RC Oscillator Output
Port E	PE[7:0]	N/A	No alternate functions

Table 53. UART Transmit Data Register (U*x*TXD)

Bit	7	6	5	4	3	2	1	0
Field	TXD							
RESET	X							
R/W	W							
Address	F40H and F48H							

Bit	Description
[7:0] TXD	**Transmit Data** UART transmitter data byte to be shifted out through the TXD*x* pin.

UART Receive Data Register

Data bytes received through the RXD*x* pin are stored in the UART Receive Data Register, shown in Table 54. The read-only UART Receive Data Register shares a Register File address with the write-only UART Transmit Data Register.

Table 54. UART Receive Data Register (U*x*RXD)

Bit	7	6	5	4	3	2	1	0
Field	RXD							
RESET	X							
R/W	R							
Address	F40H and F48H							

Bit	Description
[7:0] RXD	**Receive Data** UART receiver data byte from the RXD*x* pin.

Table 63. SPI Clock Phase (PHASE) and Clock Polarity (CLKPOL) Operation

PHASE	CLKPOL	SCK Transmit Edge	SCK Receive Edge	SCK Idle State
0	0	Falling	Rising	Low
0	1	Rising	Falling	High
1	0	Rising	Falling	Low
1	1	Falling	Rising	High

Transfer Format PHASE Equals Zero

Figure 25 displays the timing diagram for an SPI transfer in which PHASE is cleared to 0. The two SCK waveforms show polarity with CLKPOL reset to 0 and with CLKPOL set to one. The diagram may be interpreted as either a Master or Slave timing diagram because the SCK Master-In/Slave-Out (MISO) and Master-Out/Slave-In (MOSI) pins are directly connected between the Master and the Slave.

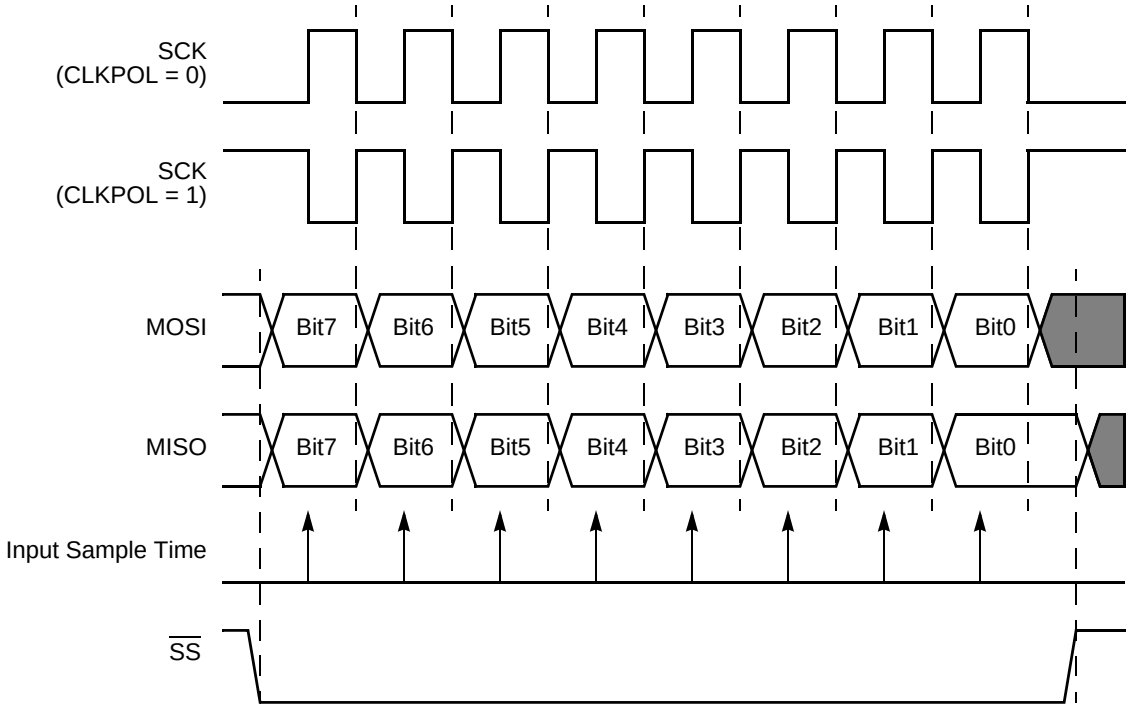

Figure 25. SPI Timing When PHASE is 0

2. Software asserts the TXI bit of the I^2C Control Register to enable transmit interrupts.
3. The I^2C interrupt asserts because the I^2C Data Register is empty.
4. Software responds to the TDRE interrupt by writing the first slave address byte to the I^2C Data Register. The least significant bit must be 0 for the write operation.
5. Software asserts the start bit of the I^2C Control Register.
6. The I^2C Controller sends the start condition to the I^2C slave.
7. The I^2C Controller loads the I^2C Shift Register with the contents of the I^2C Data Register.
8. After one bit of address is shifted out by the SDA signal, the transmit interrupt is asserted.
9. Software responds by writing the second byte of address into the contents of the I^2C Data Register.
10. The I^2C Controller shifts the rest of the first byte of address and write bit out the SDA signal.
11. If the I^2C slave acknowledges the first address byte by pulling the SDA signal Low during the next High period of SCL, the I^2C Controller sets the ACK bit in the I^2C Status Register. Continue with Step 12.

    If the slave does not acknowledge the first address byte, the I^2C Controller sets the NCKI bit and clears the ACK bit in the I^2C Status Register. Software responds to the Not Acknowledge interrupt by setting the stop and flush bits and clearing the TXI bit. The I^2C Controller sends the stop condition on the bus and clears the stop and NCKI bits. The transaction is complete (ignore the following steps).
12. The I^2C Controller loads the I^2C Shift Register with the contents of the I^2C Data Register.
13. The I^2C Controller shifts the second address byte out the SDA signal. After the first bit has been sent, the transmit interrupt is asserted.
14. Software responds by writing a data byte to the I^2C Data Register.
15. The I^2C Controller completes shifting the contents of the shift register on the SDA signal.
16. If the I^2C slave sends an acknowledge by pulling the SDA signal Low during the next High period of SCL, the I^2C Controller sets the ACK bit in the I^2C Status Register. Continue with Step 17.

    If the slave does not acknowledge the second address byte or one of the data bytes, the I^2C Controller sets the NCKI bit and clears the ACK bit in the I^2C Status Register. Software responds to the Not Acknowledge interrupt by setting the stop and flush bits and clearing the TXI bit. The I^2C Controller sends the stop condition on the bus and

Table 71. I²C Data Register (I2CDATA)

Bit	7	6	5	4	3	2	1	0
Field	DATA							
RESET	0							
R/W	R/W							
Address	F50H							

I²C Status Register

The read-only I²C Status Register, shown in Table 72, indicates the status of the I²C Controller.

Table 72. I²C Status Register (I2CSTAT)

Bit	7	6	5	4	3	2	1	0
Field	TDRE	RDRF	ACK	10B	RD	TAS	DSS	NCKI
RESET	1	0						
R/W	R							
Address	F51H							

Bit	Description
[7] TDRE	**Transmit Data Register Empty** When the I²C Controller is enabled, this bit is 1 when the I²C Data Register is empty. When this bit is set, an interrupt is generated if the TXI bit is set, except when the I²C Controller is shifting in data during the reception of a byte or when shifting an address and the RD bit is set. This bit is cleared by writing to the I2CDATA Register.
[6] RDRF	**Receive Data Register Full** This bit is set = 1 when the I²C Controller is enabled and the I²C Controller has received a byte of data. When asserted, this bit causes the I²C Controller to generate an interrupt. This bit is cleared by reading the I²C Data Register (unless the read is performed using execution of the On-Chip Debugger's Read Register command).

DMA*x* Control Register

The DMA*x* Control Register, shown in Table 78, enables and selects the mode of operation for DMA*x*.

Table 78. DMA*x* Control Register (DMA*x*CTL)

Bit	7	6	5	4	3	2	1	0
Field	DEN	DLE	DDIR	IRQEN	WSEL	RSS		
RESET	0							
R/W	R/W							
Address	FB0H, FB8H							

Bit	Description
[7] DEN	**DMA*x* Enable** 0 = DMA*x* is disabled and data transfer requests are disregarded. 1 = DMA*x* is enabled and initiates a data transfer upon receipt of a request from the trigger source.
[6] DLE	**DMA*x* Loop Enable** 0 = DMA*x* reloads the original Start Address and is then disabled after the End Address data is transferred. 1 = DMA*x*, after the End Address data is transferred, reloads the original Start Address and continues operating.
[5] DDIR	**DMA*x* Data Transfer Direction** 0 = Register File → on-chip peripheral control register. 1 = On-chip peripheral control → Register File.
[4] IRQEN	**DMA*x* Interrupt Enable** 0 = DMA*x* does not generate any interrupts. 1 = DMA*x* generates an interrupt when the End Address data is transferred.

DMA*x* Address High Nibble Register

The DMA*x* Address High Register, shown in Table 80, specifies the upper four bits of address for the Start/Current and End addresses of DMA*x*.

Table 80. DMA*x* Address High Nibble Register (DMA*x*H)

Bit	7	6	5	4	3	2	1	0
Field	DMA_END_H				DMA_START_H			
RESET	X							
R/W	R/W							
Address	FB2H, FBAH							

Bit	Description
[7:4] DMA_END_H	**DMA*x* End Address High Nibble** These bits, used with the DMA*x* End Address Low Register, form a 12-bit End Address. The full 12-bit address is provided by {DMA_END_H[3:0], DMA_END[7:0]}.
[3:0] DMA_START_H	**DMA*x* Start/Current Address High Nibble** These bits, used with the DMA*x* Start/Current Address Low Register, form a 12-bit Start/Current Address. The full 12-bit address is provided by {DMA_START_H[3:0], DMA_START[7:0]}.

Table 95. Page Select Register (FPS)

Bit	7	6	5	4	3	2	1	0
Field	INFO_EN	PAGE						
RESET	0							
R/W	R/W							
Address	FF9H							

Bit	Description
[7] INFO_EN	**Information Area Enable** 0 = Information Area is not selected. 1 = Information Area is selected. The Information area is mapped into the Flash memory address space at addresses FE00H through FFFFH.
[6:0] PAGE	**Page Select** This 7-bit field selects the Flash memory page for programming and Page Erase operations. Flash Memory Address[15:9] = PAGE[6:0].

Flash Sector Protect Register

The Flash Sector Protect Register, shown in Table 96, protects Flash memory sectors from being programmed or erased from user code. The Flash Sector Protect Register shares its Register File address with the Page Select Register. The Flash Sector Protect Register can be accessed only after writing the Flash Control Register with 5EH.

User code can only write bits in this register to 1 (bits cannot be cleared to 0 by user code). To determine the appropriate Flash memory sector address range and sector number for your Z8F64xx Series product, please refer to Table 91 on page 169.

Table 96. Flash Sector Protect Register (FPROT)

Bit	7	6	5	4	3	2	1	0
Field	SECT7	SECT6	SECT5	SECT4	SECT3	SECT2	SECT1	SECT0
RESET	0							
R/W	R/W*							
Address	FF9H							

Note: *R/W = This register is accessible for read operations; it can be written to 1 only via user code.

Bit	Description
[7:0] SECT*n*	**Sector Protect**** 0 = Sector *n* can be programmed or erased from user code. 1 = Sector *n* is protected and cannot be programmed or erased from user code.

Note: **User code can only write bits from 0 to 1.

On-Chip Debugger Control Register Definitions

This section describes the features of the On-Chip Debugger Control and Status registers.

OCD Control Register

The OCD Control Register, shown in Table 103, controls the state of the On-Chip Debugger. This register enters or exits DEBUG Mode and enables the BRK instruction.

A *reset and stop* function can be achieved by writing 81H to this register. A *reset and go* function can be achieved by writing 41H to this register. If the device is operating in DEBUG Mode, a *run* function can be implemented by writing 40H to this register.

Table 103. OCD Control Register (OCDCTL)

Bit	7	6	5	4	3	2	1	0
Field	DBGMODE	BRKEN	DBGACK	BRKLOOP	Reserved			RST
RESET	0							
R/W	R/W			R				R/W

Bit	Description
[7] DBGMODE	**DEBUG Mode** Setting this bit to 1 causes the device to enter DEBUG Mode. When in DEBUG Mode, the eZ8 CPU stops fetching new instructions. Clearing this bit causes the eZ8 CPU to start running again. This bit is automatically set when a BRK instruction is decoded and breakpoints are enabled. If the Read Protect option bit is enabled, this bit can only be cleared by resetting the device, it cannot be written to 0. 0 = TheZ8 Encore! XP F64xx Series device is operating in NORMAL Mode. 1 = The Z8 Encore! XP F64xx Series device is in DEBUG Mode.
[6] BRKEN	**Breakpoint Enable** This bit controls the behavior of the BRK instruction (op code 00H). By default, breakpoints are disabled and the BRK instruction behaves like a NOP. If this bit is set to 1 and a BRK instruction is decoded, the OCD takes action dependent upon the BRKLOOP bit. 0 = BRK instruction is disabled. 1 = BRK instruction is enabled.
[5] DBGACK	**Debug Acknowledge** This bit enables the debug acknowledge feature. If this bit is set to 1, then the OCD sends an Debug Acknowledge character (FFH) to the host when a breakpoint occurs. 0 = Debug Acknowledge is disabled. 1 = Debug Acknowledge is enabled.

Table 106. Absolute Maximum Ratings (Continued)

Parameter	Minimum	Maximum	Units	Notes
64-pin LQFP maximum ratings at –40°C to 70°C				
Total power dissipation		1000	mW	
Maximum current into V_{DD} or out of V_{SS}		275	mA	
64-pin LQFP maximum ratings at 70°C to 125°C				
Total power dissipation		540	mW	
Maximum current into V_{DD} or out of V_{SS}		150	mA	
44-pin PLCC maximum ratings at –40°C to 70°C				
Total power dissipation		750	mW	
Maximum current into V_{DD} or out of V_{SS}		200	mA	
44-pin PLCC maximum ratings at 70°C to 125°C				
Total power dissipation		295	mW	
Maximum current into V_{DD} or out of V_{SS}		83	mA	
44-pin LQFP maximum ratings at –40°C to 70°C				
Total power dissipation		750	mW	
Maximum current into V_{DD} or out of V_{SS}		200	mA	
44-pin LQFP maximum ratings at 70°C to 125°C				
Total power dissipation		360	mW	
Maximum current into V_{DD} or out of V_{SS}		100	mA	

Note: This voltage applies to all pins, with the exception of V_{DD}, AV_{DD}, pins supporting analog input (ports B and H), $\overline{\text{RESET}}$, and where noted otherwise.

Figure 43 displays the typical active mode current consumption while operating at 25 ºC plotted opposite the system clock frequency. All GPIO pins are configured as outputs and driven High.

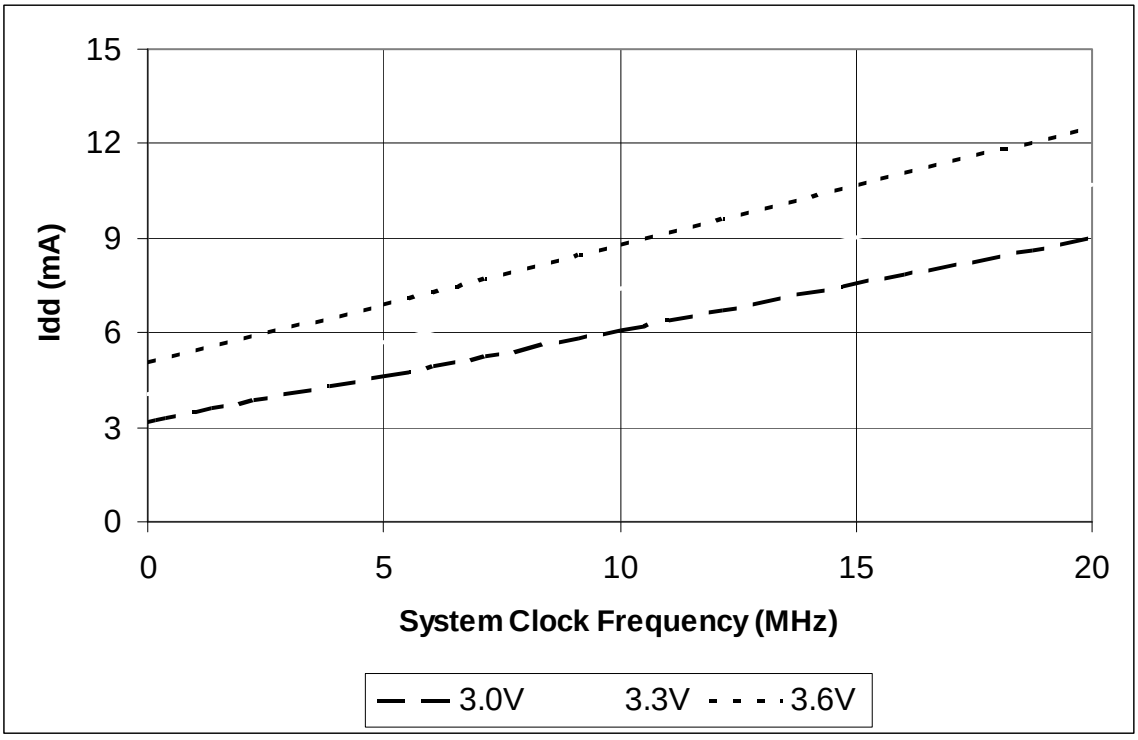

Figure 43. Typical Active Mode I_{DD} vs. System Clock Frequency

Table 111 list the Flash memory electrical characteristics and timing.

Table 111. Flash Memory Electrical Characteristics and Timing

	V_{DD} = 3.0–3.6V T_A = –40°C to 125°C				
Parameter	**Minimum**	**Typical**	**Maximum**	**Units**	**Notes**
Flash Byte Read Time	50	–	–	ns	
Flash Byte Program Time	20	–	40	µs	
Flash Page Erase Time	10	–	–	ms	
Flash Mass Erase Time	200	–	–	ms	
Writes to Single Address Before Next Erase	–	–	2		
Flash Row Program Time	–	–	8	ms	Cumulative program time for single row cannot exceed limit before next erase. This parameter is only an issue when bypassing the Flash Controller.
Data Retention	100	–	–	years	25°C
Endurance, –40°C to 105°C	10,000	–	–	cycles	Program/erase cycles
Endurance, 106°C to 125°C	1,000	–	–	cycles	Program/erase cycles

Table 112 lists the Watchdog Timer electrical characteristics and timing.

Table 112. Watchdog Timer Electrical Characteristics and Timing

		V_{DD} = 3.0–3.6V T_A = –40°C to 125°C				
Symbol	**Parameter**	**Minimum**	**Typical**	**Maximum**	**Units**	**Conditions**
F_{WDT}	WDT Oscillator Frequency	5	10	20	kHz	
I_{WDT}	WDT Oscillator Current including internal RC Oscillator	–	<1	5	µA	

Upper Nibble (Hex) \ Lower Nibble (Hex)	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0																
1																
2																
3																
4																
5																
6																
7	3,2 **PUSH** IM															
8																
9																
A			3.3 **CPC** r1,r2	3.4 **CPC** r1,Ir2	4.3 **CPC** R2,R1	4.4 **CPC** IR2,R1	4.3 **CPC** R1,IM	4.4 **CPC** IR1,IM	5.3 **CPCX** ER2,ER1	5.3 **CPCX** IM,ER1						
B																
C	3.2 **SRL** R1	3.3 **SRL** IR1														
D																
E									5,4 **LDWX** ER2,ER1							
F																

Figure 61. Second Op Code Map after 1FH

Hex Address: F15

Table 159. Timer 0–3 PWM Low Byte Register (TxPWML)

Bit	7	6	5	4	3	2	1	0
Field	PWML							
RESET	0							
R/W	R/W							
Address	F05H, F0DH, F15H, F1DH							

Hex Address: F16

Table 160. Timer 0–3 Control 0 Register (TxCTL0)

Bit	7	6	5	4	3	2	1	0
Field	Reserved			CSC	Reserved			
RESET	0							
R/W	R/W							
Address	F06H, F0EH, F16H, F1EH							

Hex Address: F17

Table 161. Timer 0–3 Control 1 Register (TxCTL1)

Bit	7	6	5	4	3	2	1	0
Field	TEN	TPOL	PRES			TMODE		
RESET	0							
R/W	R/W							
Address	F07H, F0FH, F17H, F1FH							

Hex Address: F18

Table 162. Timer 0–3 High Byte Register (TxH)

Bit	7	6	5	4	3	2	1	0
Field	TH							
RESET	0							
R/W	R/W							
Address	F00H, F08H, F10H, F18H							

Hex Address: FBA

Table 211. DMA*x* Address High Nibble Register (DMA*x*H)

Bit	7	6	5	4	3	2	1	0
Field	DMA_END_H				DMA_START_H			
RESET	X							
R/W	R/W							
Address	FB2H, FBAH							

Hex Address: FBB

Table 212. DMA*x* Start/Current Address Low Byte Register (DMA*x*START)

Bit	7	6	5	4	3	2	1	0
Field	DMA_START							
RESET	X							
R/W	R/W							
Address	FB3H, FBBH							

Hex Address: FBC

Table 213. DMA*x* End Address Low Byte Register (DMA*x*END)

Bit	7	6	5	4	3	2	1	0
Field	DMA_END							
RESET	X							
R/W	R/W							
Address	FB4H, FBCH							

Hex Address: FBD

Table 214. DMA_ADC Address Register (DMAA_ADDR)

Bit	7	6	5	4	3	2	1	0
Field	DMAA_ADDR							Reserved
RESET	X							
R/W	R/W							
Address	FBDH							

Hex Address: FF2

Table 263. Watchdog Timer Reload High Byte Register (WDTH)

Bit	7	6	5	4	3	2	1	0
Field	WDTH							
RESET	1							
R/W	R/W*							
Address	FF2H							
Note: *R/W = Read returns the current WDT count value; write sets the appropriate reload value.								

Hex Address: FF3

Table 264. Watchdog Timer Reload Low Byte Register (WDTL)

Bit	7	6	5	4	3	2	1	0
Field	WDTL							
RESET	1							
R/W	R/W*							
Address	FF3H							
Note: *R/W = Read returns the current WDT count value; write sets the appropriate reload value.								

Hex Addresses: FF4–FF7

This address range is reserved.

Ordering Information

Order your F64xx Series products from Zilog using the part numbers shown in Table 271. For more information about ordering, please consult your local Zilog sales office. The Sales Location page on the Zilog website lists all regional offices.

Table 271. Z8 Encore! XP F64xx Series Ordering Matrix

Part Number	Flash	RAM	I/O Lines	Interrupts	16-Bit Timers w/PWM	10-Bit A/D Channels	I^2C	SPI	UARTs with IrDA	Description
Z8F642x with 64KB Flash, 10-Bit Analog-to-Digital Converter										
Standard Temperature: 0°C to 70°C										
Z8F6421PM020SG	64KB	2KB	29	23	3	8	1	1	2	PDIP 40-pin package
Z8F6421AN020SG	64KB	4KB	31	23	3	8	1	1	2	LQFP 44-pin package
Z8F6421VN020SG	64KB	4KB	31	23	3	8	1	1	2	PLCC 44-pin package
Z8F6422AR020SG	64KB	4KB	46	24	4	12	1	1	2	LQFP 64-pin package
Z8F6422VS020SG	64KB	4KB	46	24	4	12	1	1	2	PLCC 68-pin package
Z8F6423FT020SG	64KB	4KB	60	24	4	12	1	1	2	QFP 80-pin package
Extended Temperature: –40°C to +105°C										
Z8F6421PM020EG	64KB	2KB	29	23	3	8	1	1	2	PDIP 40-pin package
Z8F6421AN020EG	64KB	4KB	31	23	3	8	1	1	2	LQFP 44-pin package
Z8F6421VN020EG	64KB	4KB	31	23	3	8	1	1	2	PLCC 44-pin package
Z8F6422AR020EG	64KB	4KB	46	24	4	12	1	1	2	LQFP 64-pin package
Z8F6422VS020EG	64KB	4KB	46	24	4	12	1	1	2	PLCC 68-pin package
Z8F6423FT020EG	64KB	4KB	60	24	4	12	1	1	2	QFP 80-pin package
Automotive/Industrial Temperature: –40°C to +125°C										
Z8F6421PM020AG	64KB	2KB	29	23	3	8	1	1	2	PDIP 40-pin package
Z8F6421AN020AG	64KB	4KB	31	23	3	8	1	1	2	LQFP 44-pin package
Z8F6421VN020AG	64KB	4KB	31	23	3	8	1	1	2	PLCC 44-pin package
Z8F6422AR020AG	64KB	4KB	46	24	4	12	1	1	2	LQFP 64-pin package
Z8F6422VS020AG	64KB	4KB	46	24	4	12	1	1	2	PLCC 68-pin package
Z8F6423FT020AG	64KB	4KB	60	24	4	12	1	1	2	QFP 80-pin package

Table 271. Z8 Encore! XP F64xx Series Ordering Matrix

Part Number	Flash	RAM	I/O Lines	Interrupts	16-Bit Timers w/PWM	10-Bit A/D Channels	I^2C	SPI	UARTs with IrDA	Description
Z8F162x with 16KB Flash, 10-Bit Analog-to-Digital Converter										
Standard Temperature: 0°C to 70°C										
Z8F1621PM020SG	16KB	2KB	29	23	3	8	1	1	2	PDIP 40-pin package
Z8F1621AN020SG	16KB	2KB	31	23	3	8	1	1	2	LQFP 44-pin package
Z8F1621VN020SG	16KB	2KB	31	23	3	8	1	1	2	PLCC 44-pin package
Z8F1622AR020SG	16KB	2KB	46	24	4	12	1	1	2	LQFP 64-pin package
Z8F1622VS020SG	16KB	2KB	46	24	4	12	1	1	2	PLCC 68-pin package
Extended Temperature: –40°C to +105°C										
Z8F1621PM020EG	16KB	2KB	29	23	3	8	1	1	2	PDIP 40-pin package
Z8F1621AN020EG	16KB	2KB	31	23	3	8	1	1	2	LQFP 44-pin package
Z8F1621VN020EG	16KB	2KB	31	23	3	8	1	1	2	PLCC 44-pin package
Z8F1622AR020EG	16KB	2KB	46	24	4	12	1	1	2	LQFP 64-pin package
Z8F1622VS020EG	16KB	2KB	46	24	4	12	1	1	2	PLCC 68-pin package
Automotive/Industrial Temperature: –40°C to +125°C										
Z8F1621PM020AG	16KB	2KB	29	23	3	8	1	1	2	PDIP 40-pin package
Z8F1621AN020AG	16KB	2KB	31	23	3	8	1	1	2	LQFP 44-pin package
Z8F1621VN020AG	16KB	2KB	31	23	3	8	1	1	2	PLCC 44-pin package
Z8F1622AR020AG	16KB	2KB	46	24	4	12	1	1	2	LQFP 64-pin package
Z8F1622VS020AG	16KB	2KB	46	24	4	12	1	1	2	PLCC 68-pin package
Z8F64200100KITG										Development Kit
ZUSBSC00100ZACG										USB Smart Cable Accessory Kit
ZUSBOPTSC01ZACG										Opto-Isolated USB Smart Cable Accessory Kit
ZENETSC0100ZACG										Ethernet Smart Cable Accessory Kit