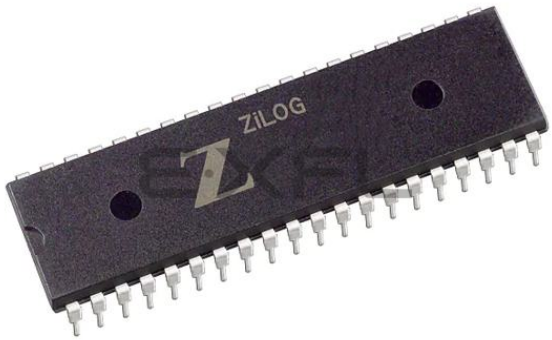

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	eZ8
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	29
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	40-DIP (0.620", 15.75mm)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8f6421pm020sg

Part Selection Guide

Table 1 identifies the basic features and package styles available for each device within the Z8 Encore! XP product line.

Table 1. Z8 Encore! XP F64xx Series Part Selection Guide

Part Number	Flash (KB)	RAM (KB)	I/O	16-bit Timers with PWM	ADC Inputs	UARTs with IrDA	I^2C	SPI	40-/ 44-Pin Package	64/68-Pin Package	80-Pin Package
Z8F1621	16	2	31	3	8	2	1	1	X		
Z8F1622	16	2	46	4	12	2	1	1		X	
Z8F2421	24	2	31	3	8	2	1	1	X		
Z8F2422	24	2	46	4	12	2	1	1		X	
Z8F3221	32	2	31	3	8	2	1	1	X		
Z8F3222	32	2	46	4	12	2	1	1		X	
Z8F4821	48	4	31	3	8	2	1	1	X		
Z8F4822	48	4	46	4	12	2	1	1		X	
Z8F4823	48	4	60	4	12	2	1	1			X
Z8F6421	64	4	31	3	8	2	1	1	X		
Z8F6422	64	4	46	4	12	2	1	1		X	
Z8F6423	64	4	60	4	12	2	1	1			X

Note: For die form sales, contact your local Zilog Sales Office.

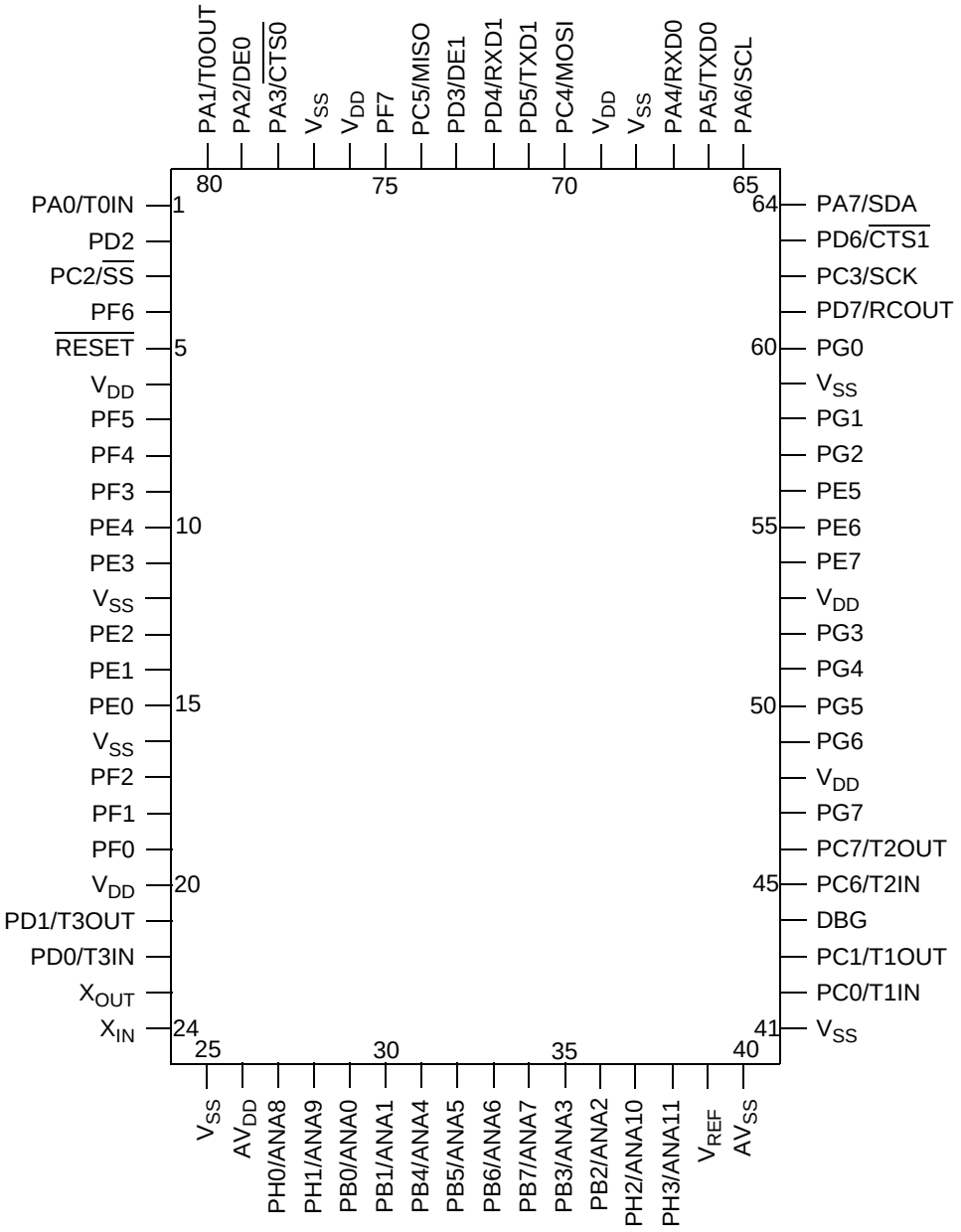

Figure 7. Z8 Encore! XP F64xx Series in 80-Pin Quad Flat Package (QFP)

Register File Address Map

Table 7 provides the address map for the Register File of the Z8 Encore! XP F64xx Series products. Not all devices and package styles in the Z8 Encore! XP F64xx Series support Timer 3 and all of the GPIO ports. Consider registers for unimplemented peripherals to be reserved.

Table 7. Z8 Encore! XP F64xx Series Register File Address Map

Address (Hex)	Register Description	Mnemonic	Reset (Hex)	Page
General-Purpose RAM				
000–EFF	General-Purpose Register File RAM	—	XX	
Timer 0				
F00	Timer 0 High Byte	T0H	00	72
F01	Timer 0 Low Byte	T0L	01	72
F02	Timer 0 Reload High Byte	T0RH	FF	74
F03	Timer 0 Reload Low Byte	T0RL	FF	74
F04	Timer 0 PWM High Byte	T0PWMH	00	75
F05	Timer 0 PWM Low Byte	T0PWML	00	75
F06	Timer 0 Control 0	T0CTL0	00	76
F07	Timer 0 Control 1	T0CTL1	00	77
Timer 1				
F08	Timer 1 High Byte	T1H	00	72
F09	Timer 1 Low Byte	T1L	01	72
F0A	Timer 1 Reload High Byte	T1RH	FF	74
F0B	Timer 1 Reload Low Byte	T1RL	FF	74
F0C	Timer 1 PWM High Byte	T1PWMH	00	75
F0D	Timer 1 PWM Low Byte	T1PWML	00	75
F0E	Timer 1 Control 0	T1CTL0	00	76
F0F	Timer 1 Control 1	T1CTL1	00	77
Timer 2				
F10	Timer 2 High Byte	T2H	00	72
F11	Timer 2 Low Byte	T2L	01	72
F12	Timer 2 Reload High Byte	T2RH	FF	74
F13	Timer 2 Reload Low Byte	T2RL	FF	74

Note: XX = Undefined.

Table 7. Z8 Encore! XP F64xx Series Register File Address Map (Continued)

Address (Hex)	Register Description	Mnemonic	Reset (Hex)	Page
UART 1 (continued)				
F4D	UART1 Address Compare Register	U1ADDR	00	105
F4E	UART1 Baud Rate High Byte	U1BRH	FF	105
F4F	UART1 Baud Rate Low Byte	U1BRL	FF	105
I^2C				
F50	I^2C Data	I2CDATA	00	141
F51	I^2C Status	I2CSTAT	80	142
F52	I^2C Control	I2CCTL	00	144
F53	I^2C Baud Rate High Byte	I2CBRH	FF	145
F54	I^2C Baud Rate Low Byte	I2CBRL	FF	145
F55	I^2C Diagnostic State	I2CDST	C0	147
F56	I^2C Diagnostic Control	I2CDIAG	00	149
F57–F5F	Reserved	—	XX	
Serial Peripheral Interface (SPI)				
F60	SPI Data	SPIDATA	XX	121
F61	SPI Control	SPICTL	00	122
F62	SPI Status	SPISTAT	01	123
F63	SPI Mode	SPIMODE	00	125
F64	SPI Diagnostic State	SPIDST	00	126
F65	Reserved	—	XX	
F66	SPI Baud Rate High Byte	SPIBRH	FF	126
F67	SPI Baud Rate Low Byte	SPIBRL	FF	126
F68–F6F	Reserved	—	XX	
Analog-to-Digital Converter				
F70	ADC Control	ADCCTL	20	165
F71	Reserved	—	XX	
F72	ADC Data High Byte	ADCD_H	XX	167
F73	ADC Data Low Bits	ADCD_L	XX	168
F74–FAF	Reserved	—	XX	
DMA 0				
FB0	DMA0 Control	DMA0CTL	00	153
FB1	DMA0 I/O Address	DMA0IO	XX	154

Note: XX = Undefined.

HALT Mode

Execution of the eZ8 CPU's HALT instruction places the device into HALT Mode. In HALT Mode, the operating characteristics are:

- Primary crystal oscillator is enabled and continues to operate
- System clock is enabled and continues to operate
- eZ8 CPU is stopped
- Program Counter stops incrementing
- Watchdog Timer's internal RC oscillator continues to operate
- The Watchdog Timer continues to operate, if enabled
- All other on-chip peripherals continue to operate

The eZ8 CPU can be brought out of HALT Mode by any of the following operations:

- Interrupt
- Watchdog Timer time-out (interrupt or reset)
- Power-On Reset
- Voltage Brown-Out Reset
- External $\overline{\text{RESET}}$ pin assertion

To minimize current in HALT Mode, all GPIO pins which are configured as inputs must be driven to one of the supply rails (V_{CC} or GND).

Timer 0–3 Control 1 Registers

The Timer 0–3 Control 1 (TxCTL1) registers enable/disable the timers, set the prescaler value, and determine the timer operating mode.

Table 46. Timer 0–3 Control 1 Register (TxCTL1)

Bit	7	6	5	4	3	2	1	0
Field	TEN	TPOL	PRES			TMODE		
RESET	0							
R/W	R/W							
Address	F07H, F0FH, F17H, F1FH							

Bit	Description
[7] TEN	**Timer Enable** 0 = Timer is disabled. 1 = Timer enabled to count.
[6] TPOL	**Timer Input/Output Polarity** Operation of this bit is a function of the current operating mode of the timer. **ONE-SHOT Mode** When the timer is disabled, the timer output signal is set to the value of this bit. When the timer is enabled, the timer output signal is complemented upon timer reload. **CONTINUOUS Mode** When the timer is disabled, the timer output signal is set to the value of this bit. When the timer is enabled, the timer output signal is complemented upon timer reload. **COUNTER Mode** When the timer is disabled, the timer output signal is set to the value of this bit. When the timer is enabled, the timer output signal is complemented upon timer reload. 0 = Count occurs on the rising edge of the timer input signal. 1 = Count occurs on the falling edge of the timer input signal. **PWM Mode** 0 = timer output is forced Low (0) when the timer is disabled. When enabled, the timer output is forced High (1) upon PWM count match and forced Low (0) upon reload. 1 = timer output is forced High (1) when the timer is disabled. When enabled, the timer output is forced Low (0) upon PWM count match and forced High (1) upon reload. **CAPTURE Mode** 0 = Count is captured on the rising edge of the timer input signal. 1 = Count is captured on the falling edge of the timer input signal. **COMPARE Mode** When the timer is disabled, the timer output signal is set to the value of this bit. When the timer is enabled, the timer output signal is complemented upon timer reload. **GATED Mode** 0 = Timer counts when the timer input signal is High (1) and interrupts are generated on the falling edge of the timer input. 1 = Timer counts when the timer input signal is Low (0) and interrupts are generated on the rising edge of the timer input. **CAPTURE/COMPARE Mode** 0 = Counting is started on the first rising edge of the timer input signal. The current count is captured on subsequent rising edges of the timer input signal. 1 = Counting is started on the first falling edge of the timer input signal. The current count is captured on subsequent falling edges of the timer input signal. **Caution:** When the timer output alternate function TxOUT on a GPIO port pin is enabled, TxOUT will change to whatever state the TPOL bit is in. The timer does not need to be enabled for that to happen. Also, the Port Data Direction Subregister is not needed to be set to output on TxOUT. Changing the TPOL bit with the timer enabled and running does not immediately change the TxOUT.

UART Interrupts

The UART features separate interrupts for the transmitter and the receiver. In addition, when the UART primary functionality is disabled, the Baud Rate Generator can also function as a basic timer with interrupt capability.

Transmitter Interrupts

The transmitter generates a single interrupt when the Transmit Data Register Empty bit (TDRE) is set to 1. This indicates that the transmitter is ready to accept new data for transmission. The TDRE interrupt occurs after the Transmit Shift Register has shifted the first bit of data out. At this point, the Transmit Data Register can be written with the next character to send. This provides 7 bit-periods of latency to load the Transmit Data Register before the Transmit Shift Register completes shifting the current character. Writing to the UART Transmit Data Register clears the TDRE bit to 0.

Receiver Interrupts

The receiver generates an interrupt when any of the following events occurs:

- A data byte has been received and is available in the UART Receive Data Register. This interrupt can be disabled independent of the other receiver interrupt sources. The received data interrupt occurs once the receive character has been received and placed in the Receive Data Register. Software must respond to this received data available condition before the next character is completely received to avoid an overrun error.

Note: In MULTIPROCESSOR Mode (MPEN = 1), the receive data interrupts are dependent on the multiprocessor configuration and the most recent address byte.

- A break is received
- An overrun is detected
- A data framing error is detected

UART Overrun Errors

When an overrun error condition occurs the UART prevents overwriting of the valid data currently in the Receive Data Register. The Break Detect and Overrun status bits are not displayed until after the valid data has been read.

After the valid data has been read, the UART Status 0 Register is updated to indicate the overrun condition (and Break Detect, if applicable). The RDA bit is set to 1 to indicate that the Receive Data Register contains a data byte. However, because the overrun error occurred, this byte may not contain valid data and should be ignored. The BRKD bit indicates if the overrun was caused by a break condition on the line. After reading the status

UART Control 0 and Control 1 Registers

The UART Control 0 and Control 1 Registers, shown in Tables 57 and 58, configure the properties of the UART's transmit and receive operations. The UART Control registers must not been written while the UART is enabled.

Table 57. UART Control 0 Register (U*x*CTL0)

Bit	7	6	5	4	3	2	1	0
Field	TEN	REN	CTSE	PEN	PSEL	SBRK	STOP	LBEN
RESET	0							
R/W	R/W							
Address	F42H and F4AH							

Bit	Description
[7] TEN	**Transmit Enable** This bit enables or disables the transmitter. The enable is also controlled by the $\overline{\text{CTS}}$ signal and the CTSE bit. If the $\overline{\text{CTS}}$ signal is low and the CTSE bit is 1, the transmitter is enabled. 0 = Transmitter disabled. 1 = Transmitter enabled.
[6] REN	**Receive Enable** This bit enables or disables the receiver. 0 = Receiver disabled. 1 = Receiver enabled.
[5] CTSE	**CTS Enable** 0 = The $\overline{\text{CTS}}$ signal has no effect on the transmitter. 1 = The UART recognizes the $\overline{\text{CTS}}$ signal as an enable control from the transmitter.
[4] PEN	**Parity Enable** This bit enables or disables parity. Even or odd is determined by the PSEL bit. It is overridden by the MPEN bit. 0 = Parity is disabled. 1 = The transmitter sends data with an additional parity bit and the receiver receives an additional parity bit.
[3] PSEL	**Parity Select** 0 = Even parity is transmitted and expected on all received data. 1 = Odd parity is transmitted and expected on all received data.
[2] SBRK	**Send Break** This bit pauses or breaks data transmission. Sending a break interrupts any transmission in progress, so ensure that the transmitter has finished sending data before setting this bit. 0 = No break is sent. 1 = The output of the transmitter is zero.

Serial Peripheral Interface

The Serial Peripheral Interface is a synchronous interface allowing several SPI-type devices to be interconnected. SPI-compatible devices include EEPROMs, Analog-to-Digital Converters, and ISDN devices. Features of the SPI include:

- Full-duplex, synchronous, character-oriented communication
- Four-wire interface
- Data transfers rates up to a maximum of one-half the system clock frequency
- Error detection
- Dedicated Baud Rate Generator

Architecture

The SPI may be configured as either a Master (in single or multimaster systems) or a Slave as displayed in Figures 22 through 24.

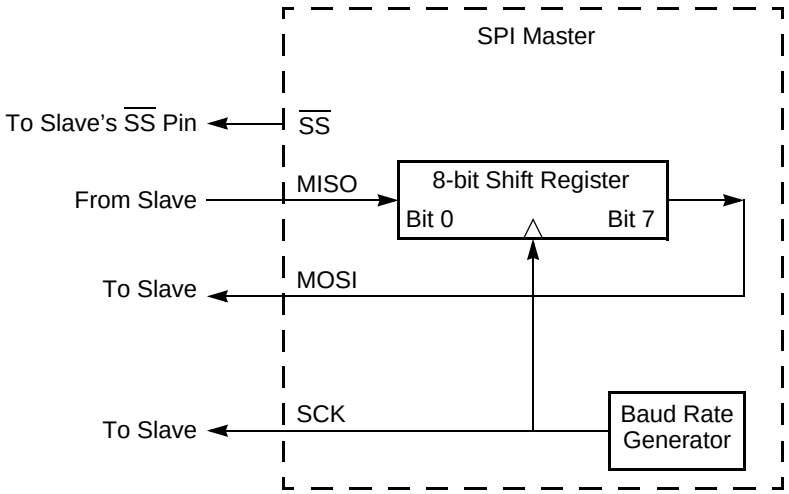

Figure 22. SPI Configured as a Master in a Single-Master, Single-Slave System

Transfer Format PHASE Equals One

Figure 26 displays the timing diagram for an SPI transfer in which PHASE is 1. Two waveforms are depicted for SCK, one for CLKPOL reset to 0 and another for CLKPOL set to 1.

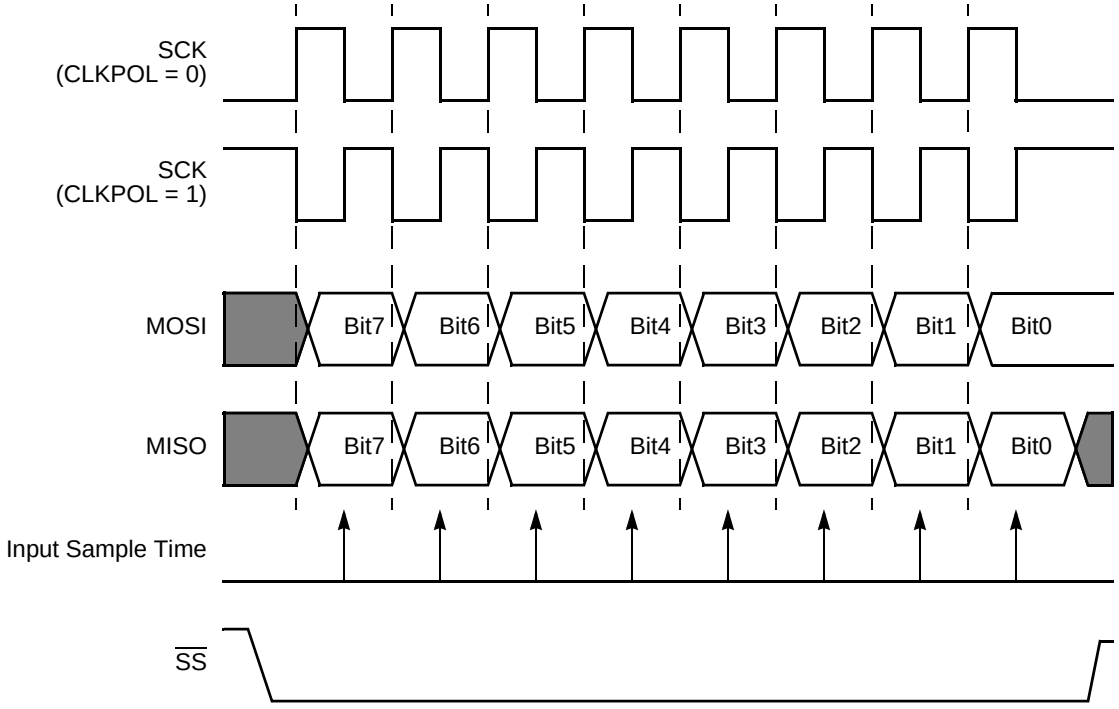

Figure 26. SPI Timing When PHASE is 1

Multimaster Operation

In a multimaster SPI system, all SCK pins are tied together, all MOSI pins are tied together and all MISO pins are tied together. All SPI pins must then be configured in OPEN-DRAIN mode to prevent bus contention. At any one time, only one SPI device is configured as the Master and all other SPI devices on the bus are configured as Slaves. The Master enables a single Slave by asserting the $\overline{SS}$ pin on that Slave only. Then, the single Master drives data out its SCK and MOSI pins to the SCK and MOSI pins on the Slaves (including those which are not enabled). The enabled Slave drives data out its MISO pin to the MISO Master pin.

For a Master device operating in a multimaster system, if the $\overline{SS}$ pin is configured as an input and is driven Low by another Master, the COL bit is set to 1 in the SPI Status Register. The COL bit indicates the occurrence of a multimaster collision (mode fault error condition).

Table 69. SPI Baud Rate High Byte Register (SPIBRH)

Bit	7	6	5	4	3	2	1	0
Field	BRH							
RESET	1							
R/W	R/W							
Address	F66H							

Bit	Description
[7:0] BRH	**SPI Baud Rate High Byte** Most significant byte, BRG[15:8], of the SPI Baud Rate Generator's reload value.

Table 70. SPI Baud Rate Low Byte Register (SPIBRL)

Bit	7	6	5	4	3	2	1	0
Field	BRL							
RESET	1							
R/W	R/W							
Address	F67H							

Bit	Description
[7:0] BRL	**SPI Baud Rate Low Byte** Least significant byte, BRG[7:0], of the SPI Baud Rate Generator's reload value.

Bit	Description (Continued)	
[4:0] TXRXSTATE	**Internal State** Value of the internal I^2C state machine.	
	TXRXSTATE	**State Description**
[4:0] TXRXSTATE (continued)	0_0000	Idle State.
	0_0001	Start State.
	0_0010	Send/Receive data bit 7.
	0_0011	Send/Receive data bit 6.
	0_0100	Send/Receive data bit 5.
	0_0101	Send/Receive data bit 4.
	0_0110	Send/Receive data bit 3.
	0_0111	Send/Receive data bit 2.
	0_1000	Send/Receive data bit 1.
	0_1001	Send/Receive data bit 0.
	0_1010	Data Acknowledge State.
	0_1011	Second half of data Acknowledge State used only for not acknowledge.
	0_1100	First part of stop state.
	0_1101	Second part of stop state.
	0_1110	10-bit addressing: Acknowledge State for 2nd address byte 7-bit addressing: Address Acknowledge State.
	0_1111	10-bit address: Bit 0 (Least significant bit) of 2nd address byte 7-bit address: Bit 0 (Least significant bit) (R/W) of address byte.
	1_0000	10-bit addressing: Bit 7 (Most significant bit) of 1st address byte.
	1_0001	10-bit addressing: Bit 6 of 1st address byte.
	1_0010	10-bit addressing: Bit 5 of 1st address byte.
	1_0011	10-bit addressing: Bit 4 of 1st address byte.
	1_0100	10-bit addressing: Bit 3 of 1st address byte.
	1_0101	10-bit addressing: Bit 2 of 1st address byte.
	1_0110	10-bit addressing: Bit 1 of 1st address byte.
	1_0111	10-bit addressing: Bit 0 (R/W) of 1st address byte.
	1_1000	10-bit addressing: Acknowledge state for 1st address byte.
	1_1001	10-bit addressing: Bit 7 of 2nd address byte 7-bit addressing: Bit 7 of address byte.
	1_1010	10-bit addressing: Bit 6 of 2nd address byte 7-bit addressing: Bit 6 of address byte.
	1_1011	10-bit addressing: Bit 5 of 2nd address byte 7-bit addressing: Bit 5 of address byte.
	1_1100	10-bit addressing: Bit 4 of 2nd address byte 7-bit addressing: Bit 4 of address byte.
	1_1101	10-bit addressing: Bit 3 of 2nd address byte 7-bit addressing: Bit 3 of address byte.
	1_1110	10-bit addressing: Bit 2 of 2nd address byte 7-bit addressing: Bit 2 of address byte.
	1_1111	10-bit addressing: Bit 1 of 2nd address byte 7-bit addressing: Bit 1 of address byte.

2. Determine the 12-bit Start and End Register File addresses. The 12-bit Start Address is provided by {DMA*x*_H[3:0], DMA_START[7:0]}. The 12-bit End Address is provided by {DMA*x*_H[7:4], DMA_END[7:0]}.
3. Write the Start and End Register File address high nibbles to the DMA*x* End/Start Address High Nibble Register.
4. Write the lower byte of the Start Address to the DMA*x* Start/Current Address Register.
5. Write the lower byte of the End Address to the DMA*x* End Address Register.
6. Write to the DMA*x* Control Register to complete the following operations:
   - Select loop or single-pass mode operation
   - Select the data transfer direction (either from the Register File RAM to the on-chip peripheral control register; or from the on-chip peripheral control register to the Register File RAM)
   - Enable the DMA*x* interrupt request, if appropriate
   - Select Word or Byte mode
   - Select the DMA*x* request trigger
   - Enable the DMA*x* channel

DMA_ADC Operation

DMA_ADC transfers data from the ADC to the Register File. The sequence of operations in a DMA_ADC data transfer is:

1. ADC completes conversion on the current ADC input channel and signals the DMA controller that two-bytes of ADC data are ready for transfer.
2. DMA_ADC requests control of the system bus (address and data) from the eZ8 CPU.
3. After the eZ8 CPU acknowledges the bus request, DMA_ADC transfers the two-byte ADC output value to the Register File and then returns system bus control back to the eZ8 CPU.
4. If the current ADC analog input is the highest-numbered input to be converted:
   - The DMA_ADC resets the ADC analog input number to 0 and initiates data conversion on ADC analog input 0
   - If configured to generate an interrupt, the DMA_ADC sends an interrupt request to the Interrupt Controller

   If the current ADC analog input is not the highest-numbered input to be converted, then the DMA_ADC initiates data conversion in the next higher-numbered ADC analog input.

Observe the following procedure to setup the Flash Sector Protect Register from user code:

1. Write 00H to the Flash Control Register to reset the Flash Controller.
2. Write 5EH to the Flash Control Register to select the Flash Sector Protect Register.
3. Read and/or write the Flash Sector Protect Register which is now at Register File address FF9H.
4. Write 00H to the Flash Control Register to return the Flash Controller to its reset state.

Flash Write Protection Option Bit

The Flash Write Protect option bit can be enabled to block all program and erase operations from user code. For more information, see the Option Bits chapter on page 180.

Byte Programming

When the Flash Controller is unlocked, writes to Flash memory from user code will program a byte into the Flash if the address is located in the unlocked page. An erased Flash byte contains all ones (FFH). The programming operation can only be used to change bits from one to zero. To change a Flash bit (or multiple bits) from zero to one requires a Page Erase or Mass Erase operation.

Byte programming can be accomplished using the eZ8 CPU's LDC or LDCI instructions. For a description of the LDC and LDCI instructions, refer to the eZ8 CPU Core User Manual (UM0128), which is available for download on www.zilog.com.

While the Flash Controller programs Flash memory, the eZ8 CPU idles but the system clock and on-chip peripherals continue to operate. Interrupts that occur when a programming operation is in progress are serviced after the programming operation is complete. To exit programming mode and lock the Flash Controller, write 00H to the Flash Control Register.

User code cannot program Flash memory on a page that resides in a protected sector. When user code writes memory locations, only addresses located in the unlocked page are programmed. Memory writes outside of the unlocked page are ignored.

! **Caution:** Each memory location must not be programmed more than twice before an erase occurs.

Observe the following procedure to program the Flash from user code:

1. Write 00H to the Flash Control Register to reset the Flash Controller.
2. Write the page of memory to be programmed to the Page Select Register.
3. Write the first unlock command 73H to the Flash Control Register.

Table 106. Absolute Maximum Ratings (Continued)

Parameter	Minimum	Maximum	Units	Notes
64-pin LQFP maximum ratings at –40°C to 70°C				
Total power dissipation		1000	mW	
Maximum current into V_{DD} or out of V_{SS}		275	mA	
64-pin LQFP maximum ratings at 70°C to 125°C				
Total power dissipation		540	mW	
Maximum current into V_{DD} or out of V_{SS}		150	mA	
44-pin PLCC maximum ratings at –40°C to 70°C				
Total power dissipation		750	mW	
Maximum current into V_{DD} or out of V_{SS}		200	mA	
44-pin PLCC maximum ratings at 70°C to 125°C				
Total power dissipation		295	mW	
Maximum current into V_{DD} or out of V_{SS}		83	mA	
44-pin LQFP maximum ratings at –40°C to 70°C				
Total power dissipation		750	mW	
Maximum current into V_{DD} or out of V_{SS}		200	mA	
44-pin LQFP maximum ratings at 70°C to 125°C				
Total power dissipation		360	mW	
Maximum current into V_{DD} or out of V_{SS}		100	mA	

Note: This voltage applies to all pins, with the exception of V_{DD}, AV_{DD}, pins supporting analog input (ports B and H), $\overline{\text{RESET}}$, and where noted otherwise.

Hex Address: FBE

Table 215. DMA_ADC Control Register (DMAACTL)

Bit	7	6	5	4	3	2	1	0
Field	DAEN	IRQEN	Reserved		ADC_IN			
RESET	0							
R/W	R/W							
Address	FBEH							

Hex Address: FBF

Table 216. DMA_ADC Status Register (DMAA_STAT)

Bit	7	6	5	4	3	2	1	0
Field	CADC[3:0]				Reserved	IRQA	IRQ1	IRQ0
RESET	0							
R/W	R							
Address	FBFH							

Interrupt Request (IRQ)

For more information about these IRQ Control registers, see the Interrupt Control Register Definitions section on page 51.

Hex Address: FC0

Table 217. Interrupt Request 0 Register (IRQ0)

Bit	7	6	5	4	3	2	1	0
Field	T2I	T1I	T0I	U0RXI	U0TXI	I2CI	SPII	ADCI
RESET	0							
R/W	R/W							
Address	FC0H							

Hex Address: FC5

Table 222. IRQ1 Enable Low Bit Register (IRQ1ENL)

Bit	7	6	5	4	3	2	1	0
Field	PAD7ENL	PAD6ENL	PAD5ENL	PAD4ENL	PAD3ENL	PAD2ENL	PAD1ENL	PAD0ENL
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	FC5H							

Hex Address: FC6

Table 223. Interrupt Request 2 Register (IRQ2)

Bit	7	6	5	4	3	2	1	0
Field	T3I	U1RXI	U1TXI	DMAI	PC3I	PC2I	PC1I	PC0I
RESET	0							
R/W	R/W							
Address	FC6H							

Hex Address: FC7

Table 224. IRQ2 Enable High Bit Register (IRQ2ENH)

Bit	7	6	5	4	3	2	1	0
Field	T3ENH	U1RENH	U1TENH	DMAENH	C3ENH	C2ENH	C1ENH	C0ENH
RESET	0							
R/W	R/W							
Address	FC7H							

Hex Address: FC8

Table 225. IRQ2 Enable Low Bit Register (IRQ2ENL)

Bit	7	6	5	4	3	2	1	0
Field	T3ENL	U1RENL	U1TENL	DMAENL	C3ENL	C2ENL	C1ENL	C0ENL
RESET	0							
R/W	R/W							
Address	FC8H							

Hex Address: FF2

Table 263. Watchdog Timer Reload High Byte Register (WDTH)

Bit	7	6	5	4	3	2	1	0
Field	WDTH							
RESET	1							
R/W	R/W*							
Address	FF2H							
Note: *R/W = Read returns the current WDT count value; write sets the appropriate reload value.								

Hex Address: FF3

Table 264. Watchdog Timer Reload Low Byte Register (WDTL)

Bit	7	6	5	4	3	2	1	0
Field	WDTL							
RESET	1							
R/W	R/W*							
Address	FF3H							
Note: *R/W = Read returns the current WDT count value; write sets the appropriate reload value.								

Hex Addresses: FF4–FF7

This address range is reserved.

Part Number Suffix Designations

Zilog part numbers consist of a number of component. In the following example, part number Z8F6421AN020SG is an 8-bit Flash MCU with 4KB of program memory in a 44-pin LQFP package, operating with a maximum 20MHz external clock frequency over a 0ºC to +70ºC temperature range and built using environmentally friendly (lead-free) solder.