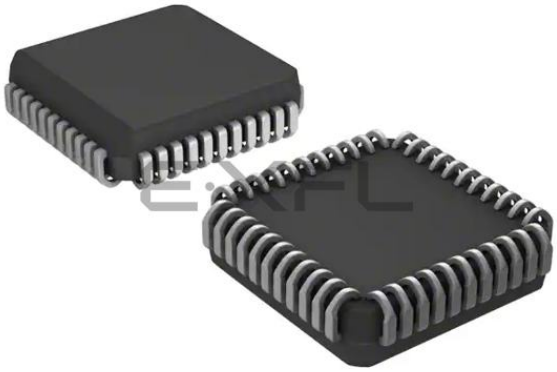

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	eZ8
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	31
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8f6421vn020eg

Introduction

Zilog's Z8 Encore! XP F64xx Series MCU family of products are a line of Zilog microcontroller products based upon the 8-bit eZ8 CPU. The Z8 Encore! XP F64xx Series adds Flash memory to Zilog's extensive line of 8-bit microcontrollers. The Flash in-circuit programming capability allows for faster development time and program changes in the field. The new eZ8 CPU is upward-compatible with existing Z8 instructions. The rich-peripheral set of the Z8 Encore! XP F64xx Series makes it suitable for a variety of applications including motor control, security systems, home appliances, personal electronic devices, and sensors.

Features

The features of Z8 Encore! XP F64xx Series include:

- 20MHz eZ8 CPU
- Up to 64KB Flash with in-circuit programming capability
- Up to 4KB register RAM
- 12-channel, 10-bit Analog-to-Digital Converter (ADC)
- Two full-duplex 9-bit UARTs with bus transceiver Driver Enable control
- Inter-integrated circuit (I^2C)
- Serial Peripheral Interface (SPI)
- Two Infrared Data Association (IrDA)-compliant infrared encoder/decoders
- Up to four 16-bit timers with capture, compare and PWM capability
- Watchdog Timer (WDT) with internal RC oscillator
- Three-channel DMA
- Up to 60 input/output (I/O) pins
- 24 interrupts with configurable priority
- On-Chip Debugger
- Voltage Brown-Out (VBO) Protection
- Power-On Reset (POR)
- Operating voltage of 3.0V to 3.6V with 5V-tolerant inputs
- 0°C to +70°C, –40°C to +105°C, and –40°C to +125°C operating temperature ranges

Table 7. Z8 Encore! XP F64xx Series Register File Address Map (Continued)

Address (Hex)	Register Description	Mnemonic	Reset (Hex)	Page
UART 1 (continued)				
F4D	UART1 Address Compare Register	U1ADDR	00	105
F4E	UART1 Baud Rate High Byte	U1BRH	FF	105
F4F	UART1 Baud Rate Low Byte	U1BRL	FF	105
I^2C				
F50	I^2C Data	I2CDATA	00	141
F51	I^2C Status	I2CSTAT	80	142
F52	I^2C Control	I2CCTL	00	144
F53	I^2C Baud Rate High Byte	I2CBRH	FF	145
F54	I^2C Baud Rate Low Byte	I2CBRL	FF	145
F55	I^2C Diagnostic State	I2CDST	C0	147
F56	I^2C Diagnostic Control	I2CDIAG	00	149
F57–F5F	Reserved	—	XX	
Serial Peripheral Interface (SPI)				
F60	SPI Data	SPIDATA	XX	121
F61	SPI Control	SPICTL	00	122
F62	SPI Status	SPISTAT	01	123
F63	SPI Mode	SPIMODE	00	125
F64	SPI Diagnostic State	SPIDST	00	126
F65	Reserved	—	XX	
F66	SPI Baud Rate High Byte	SPIBRH	FF	126
F67	SPI Baud Rate Low Byte	SPIBRL	FF	126
F68–F6F	Reserved	—	XX	
Analog-to-Digital Converter				
F70	ADC Control	ADCCTL	20	165
F71	Reserved	—	XX	
F72	ADC Data High Byte	ADCD_H	XX	167
F73	ADC Data Low Bits	ADCD_L	XX	168
F74–FAF	Reserved	—	XX	
DMA 0				
FB0	DMA0 Control	DMA0CTL	00	153
FB1	DMA0 I/O Address	DMA0IO	XX	154

Note: XX = Undefined.

Timer 0–3 Control 1 Registers

The Timer 0–3 Control 1 (TxCTL1) registers enable/disable the timers, set the prescaler value, and determine the timer operating mode.

Table 46. Timer 0–3 Control 1 Register (TxCTL1)

Bit	7	6	5	4	3	2	1	0
Field	TEN	TPOL	PRES			TMODE		
RESET	0							
R/W	R/W							
Address	F07H, F0FH, F17H, F1FH							

Table 53. UART Transmit Data Register (U*x*TXD)

Bit	7	6	5	4	3	2	1	0
Field	TXD							
RESET	X							
R/W	W							
Address	F40H and F48H							

Bit	Description
[7:0] TXD	**Transmit Data** UART transmitter data byte to be shifted out through the TXD*x* pin.

UART Receive Data Register

Data bytes received through the RXD*x* pin are stored in the UART Receive Data Register, shown in Table 54. The read-only UART Receive Data Register shares a Register File address with the write-only UART Transmit Data Register.

Table 54. UART Receive Data Register (U*x*RXD)

Bit	7	6	5	4	3	2	1	0
Field	RXD							
RESET	X							
R/W	R							
Address	F40H and F48H							

Bit	Description
[7:0] RXD	**Receive Data** UART receiver data byte from the RXD*x* pin.

Transfer Format PHASE Equals One

Figure 26 displays the timing diagram for an SPI transfer in which PHASE is 1. Two waveforms are depicted for SCK, one for CLKPOL reset to 0 and another for CLKPOL set to 1.

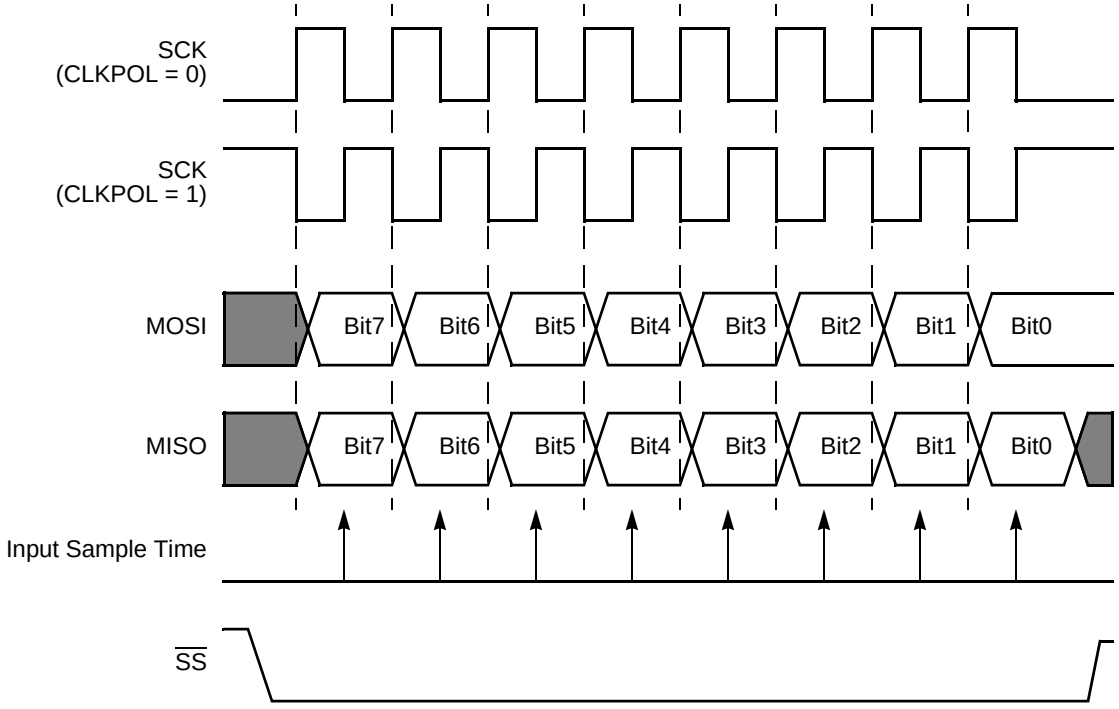

Figure 26. SPI Timing When PHASE is 1

Multimaster Operation

In a multimaster SPI system, all SCK pins are tied together, all MOSI pins are tied together and all MISO pins are tied together. All SPI pins must then be configured in OPEN-DRAIN mode to prevent bus contention. At any one time, only one SPI device is configured as the Master and all other SPI devices on the bus are configured as Slaves. The Master enables a single Slave by asserting the $\overline{SS}$ pin on that Slave only. Then, the single Master drives data out its SCK and MOSI pins to the SCK and MOSI pins on the Slaves (including those which are not enabled). The enabled Slave drives data out its MISO pin to the MISO Master pin.

For a Master device operating in a multimaster system, if the $\overline{SS}$ pin is configured as an input and is driven Low by another Master, the COL bit is set to 1 in the SPI Status Register. The COL bit indicates the occurrence of a multimaster collision (mode fault error condition).

When configured as a general purpose timer, the interrupt interval is calculated using the following equation:

Interrupt Interval (s) = System Clock Period (s) × BRG[15:0]

SPI Control Register Definitions

This section defines the features of the following Serial Peripheral Interface registers.

SPI Data Register

The SPI Data Register, shown in Table 64, stores both the outgoing (transmit) data and the incoming (receive) data. Reads from the SPI Data Register always return the current contents of the 8-bit shift register. Data is shifted out starting with bit 7. The last bit received resides in bit position 0.

With the SPI configured as a Master, writing a data byte to this register initiates the data transmission. With the SPI configured as a Slave, writing a data byte to this register loads the shift register in preparation for the next data transfer with the external Master. In either the Master or Slave modes, if a transmission is already in progress, writes to this register are ignored and the overrun error flag, OVR, is set in the SPI Status Register.

When the character length is less than 8 bits (as set by the NUMBITS field in the SPI Mode Register), the transmit character must be left justified in the SPI Data Register. A received character of less than 8 bits is right justified (last bit received is in bit position 0). For example, if the SPI is configured for 4-bit characters, the transmit characters must be written to SPIDATA[7:4] and the received characters are read from SPIDATA[3:0].

SPI Mode Register

The SPI Mode Register, shown in Table 67, configures the character bit width and the direction and value of the $\overline{SS}$ pin.

Table 67. SPI Mode Register (SPIMODE)

Bit	7	6	5	4	3	2	1	0
Field	Reserved		DIAG	NUMBITS[2:0]			SSIO	SSV
RESET	0							
R/W	R		R/W					
Address	F63H							

Bit	Description
[7:6]	**Reserved** These bits are reserved and must be programmed to 00.
[5] DIAG	**Diagnostic Mode Control bit** This bit is for SPI diagnostics. Setting this bit allows the Baud Rate Generator value to be read using the SPIBRH and SPIBRL Register locations. 0 = Reading SPIBRH, SPIBRL returns the value in the SPIBRH and SPIBRL registers. 1 = Reading SPIBRH returns bits [15:8] of the SPI Baud Rate Generator; and reading SPIBRL returns bits [7:0] of the SPI Baud Rate Counter. The Baud Rate Counter High and Low byte values are not buffered. **Caution:** Exercise caution if reading the values while the BRG is counting.
[4] NUMBITS[2:0]	**Number of Data Bits Per Character to Transfer** This field contains the number of bits to shift for each character transfer. For information about valid bit positions when the character length is less than 8 bits, see the SPI Data Register (SPIDATA) description. 000 = 8 bits. 001 = 1 bit. 010 = 2 bits. 011 = 3 bits. 100 = 4 bits. 101 = 5 bits. 110 = 6 bits. 111 = 7 bits.
[1] SSIO	**Slave Select I/O** 0 = $\overline{SS}$ pin configured as an input. 1 = $\overline{SS}$ pin configured as an output (Master mode only).
[0] SSV	**Slave Select Value** If SSIO = 1 and SPI is configured as a Master, the following conditions are true: 0 = $\overline{SS}$ pin driven Low (0). 1 = $\overline{SS}$ pin driven High (1). This bit has no effect if SSIO = 0 or if SPI is configured as a Slave.

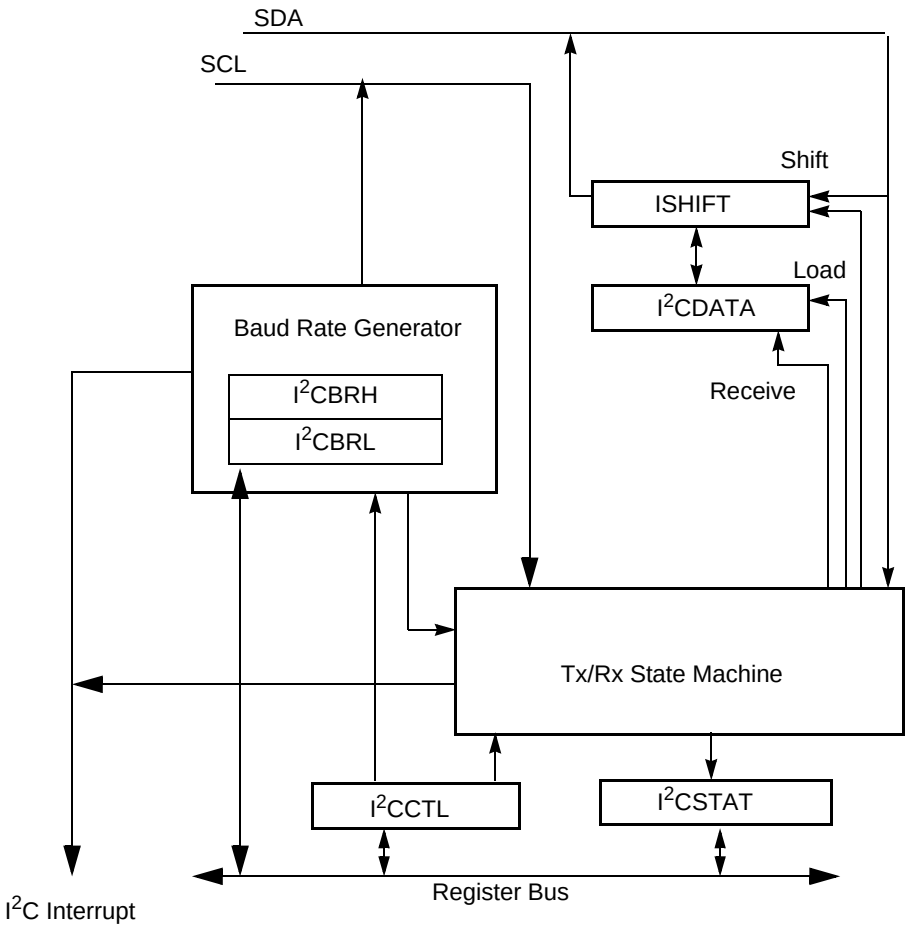

Figure 27. I²C Controller Block Diagram

Operation

The I²C Controller operates in MASTER Mode to transmit and receive data. Only a single master is supported. Arbitration between two masters must be accomplished in software. I²C supports the following operations:

- Master transmits to a 7-bit slave
- Master transmits to a 10-bit slave
- Master receives from a 7-bit slave
- Master receives from a 10-bit slave

Bit	Description (Continued)
[4] CONT	**Conversion** 0 = Single-shot conversion. ADC data is output once at completion of the 5129 system clock cycles. 1 = Continuous conversion. ADC data updated every 256 system clock cycles.
[3:0] ANAIN[3:0]	**Analog Input Select** These bits select the analog input for conversion. For information about the Port pins available with each package style, see the Signal and Pin Descriptions chapter on page 7. Do not enable unavailable analog inputs. 0000 = ANA0. 0001 = ANA1. 0010 = ANA2. 0011 = ANA3. 0100 = ANA4. 0101 = ANA5. 0110 = ANA6. 0111 = ANA7. 1000 = ANA8. 1001 = ANA9. 1010 = ANA10. 1011 = ANA11. 11xx = Reserved.

Observe the following procedure to setup the Flash Sector Protect Register from user code:

1. Write 00H to the Flash Control Register to reset the Flash Controller.
2. Write 5EH to the Flash Control Register to select the Flash Sector Protect Register.
3. Read and/or write the Flash Sector Protect Register which is now at Register File address FF9H.
4. Write 00H to the Flash Control Register to return the Flash Controller to its reset state.

Flash Write Protection Option Bit

The Flash Write Protect option bit can be enabled to block all program and erase operations from user code. For more information, see the Option Bits chapter on page 180.

Byte Programming

When the Flash Controller is unlocked, writes to Flash memory from user code will program a byte into the Flash if the address is located in the unlocked page. An erased Flash byte contains all ones (FFH). The programming operation can only be used to change bits from one to zero. To change a Flash bit (or multiple bits) from zero to one requires a Page Erase or Mass Erase operation.

Byte programming can be accomplished using the eZ8 CPU's LDC or LDCI instructions. For a description of the LDC and LDCI instructions, refer to the eZ8 CPU Core User Manual (UM0128), which is available for download on www.zilog.com.

While the Flash Controller programs Flash memory, the eZ8 CPU idles but the system clock and on-chip peripherals continue to operate. Interrupts that occur when a programming operation is in progress are serviced after the programming operation is complete. To exit programming mode and lock the Flash Controller, write 00H to the Flash Control Register.

User code cannot program Flash memory on a page that resides in a protected sector. When user code writes memory locations, only addresses located in the unlocked page are programmed. Memory writes outside of the unlocked page are ignored.

! **Caution:** Each memory location must not be programmed more than twice before an erase occurs.

Observe the following procedure to program the Flash from user code:

1. Write 00H to the Flash Control Register to reset the Flash Controller.
2. Write the page of memory to be programmed to the Page Select Register.
3. Write the first unlock command 73H to the Flash Control Register.

Table 95. Page Select Register (FPS)

Bit	7	6	5	4	3	2	1	0
Field	INFO_EN	PAGE						
RESET	0							
R/W	R/W							
Address	FF9H							

Bit	Description
[7] INFO_EN	**Information Area Enable** 0 = Information Area is not selected. 1 = Information Area is selected. The Information area is mapped into the Flash memory address space at addresses FE00H through FFFFH.
[6:0] PAGE	**Page Select** This 7-bit field selects the Flash memory page for programming and Page Erase operations. Flash Memory Address[15:9] = PAGE[6:0].

Flash Sector Protect Register

The Flash Sector Protect Register, shown in Table 96, protects Flash memory sectors from being programmed or erased from user code. The Flash Sector Protect Register shares its Register File address with the Page Select Register. The Flash Sector Protect Register can be accessed only after writing the Flash Control Register with 5EH.

User code can only write bits in this register to 1 (bits cannot be cleared to 0 by user code). To determine the appropriate Flash memory sector address range and sector number for your Z8F64xx Series product, please refer to Table 91 on page 169.

Table 96. Flash Sector Protect Register (FPROT)

Bit	7	6	5	4	3	2	1	0
Field	SECT7	SECT6	SECT5	SECT4	SECT3	SECT2	SECT1	SECT0
RESET	0							
R/W	R/W*							
Address	FF9H							

Note: *R/W = This register is accessible for read operations; it can be written to 1 only via user code.

Bit	Description
[7:0] SECT*n*	**Sector Protect**** 0 = Sector *n* can be programmed or erased from user code. 1 = Sector *n* is protected and cannot be programmed or erased from user code.

Note: **User code can only write bits from 0 to 1.

Option Bits

Option bits allow user configuration of certain aspects of the Z8 Encore! XP F64xx Series operation. The feature configuration data is stored in the Flash memory and read during Reset. The features available for control via the option bits are:

- Watchdog Timer time-out response selection–interrupt or Reset
- Watchdog Timer enabled at Reset
- The ability to prevent unwanted read access to user code in Flash memory
- The ability to prevent accidental programming and erasure of the user code in Flash memory
- Voltage Brown-Out configuration is always enabled or disabled during STOP Mode to reduce STOP Mode power consumption
- Oscillator mode selection for high-, medium-, and low-power crystal oscillators or an external RC oscillator

Operation

This section describes the type and configuration of the programmable Flash option bits.

Option Bit Configuration By Reset

Each time the option bits are programmed or erased, the device must be Reset for the change to take place. During any reset operation (System Reset, Reset, or Stop Mode Recovery), the option bits are automatically read from the Flash memory and written to Option Configuration registers. The Option Configuration registers control operation of the devices within the Z8 Encore! XP F64xx Series. Option bit control is established before the device exits Reset and the eZ8 CPU begins code execution. The Option Configuration registers are not part of the Register File and are not accessible for read or write access.

Option Bit Address Space

The first two bytes of Flash memory at addresses 0000H (see Table 99) and 0001H (see Table 100) are reserved for the user option bits. The byte at Flash memory address 0000H configures user options. The byte at Flash memory address 0001H is reserved for future use and must remain unprogrammed.

Figure 46 displays the maximum HALT Mode current consumption across the full operating temperature range of the device and plotted opposite the system clock frequency. All GPIO pins are configured as outputs and driven High.

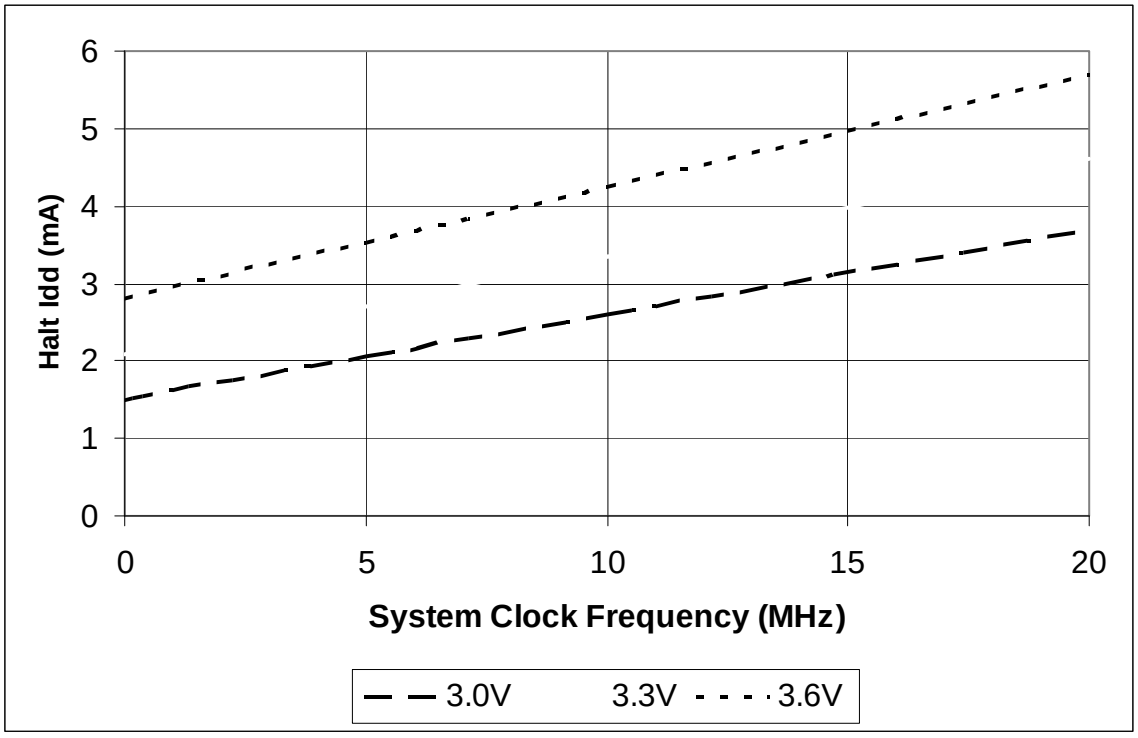

Figure 46. Maximum HALT Mode I_{CC} vs. System Clock Frequency

Condition Codes

The C, Z, S and V flags control the operation of the conditional jump (JP cc and JR cc) instructions. Sixteen frequently useful functions of the flag settings are encoded in a 4-bit field called the condition code (cc), which forms bits 7:4 of the conditional jump instructions. The condition codes are summarized in Table 127. Some binary condition codes can be created using more than one assembly code mnemonic. The result of the flag test operation decides if the conditional jump is executed.

Table 127. Condition Codes

Binary	Hex	Assembly Mnemonic	Definition	Flag Test Operation
0000	0	F	Always False	–
0001	1	LT	Less Than	(S XOR V) = 1
0010	2	LE	Less Than or Equal	(Z OR (S XOR V)) = 1
0011	3	ULE	Unsigned Less Than or Equal	(C OR Z) = 1
0100	4	OV	Overflow	V = 1
0101	5	MI	Minus	S = 1
0110	6	Z	Zero	Z = 1
0110	6	EQ	Equal	Z = 1
0111	7	C	Carry	C = 1
0111	7	ULT	Unsigned Less Than	C = 1
1000	8	T (or blank)	Always True	–
1001	9	GE	Greater Than or Equal	(S XOR V) = 0
1010	A	GT	Greater Than	(Z OR (S XOR V)) = 0
1011	B	UGT	Unsigned Greater Than	(C = 0 AND Z = 0) = 1
1100	C	NOV	No Overflow	V = 0
1101	D	PL	Plus	S = 0
1110	E	NZ	Non-Zero	Z = 0
1110	E	NE	Not Equal	Z = 0
1111	F	NC	No Carry	C = 0
1111	F	UGE	Unsigned Greater Than or Equal	C = 0

Table 136. eZ8 CPU Instruction Summary (Continued)

Assembly Mnemonic	Symbolic Operation	Address Mode dst	Address Mode src	Opcode(s) (Hex)	Flags C	Z	S	V	D	H	Fetch Cycles	Instr. Cycles
LDX dst, src	dst ← src	r	ER	84	–	–	–	–	–	–	3	2
		Ir	ER	85							3	3
		R	IRR	86							3	4
		IR	IRR	87							3	5
		r	X(rr)	88							3	4
		X(rr)	r	89							3	4
		ER	r	94							3	2
		ER	Ir	95							3	3
		IRR	R	96							3	4
		IRR	IR	97							3	5
		ER	ER	E8							4	2
		ER	IM	E9							4	2
LEA dst, X(src)	dst ← src + X	r	X(r)	98	–	–	–	–	–	–	3	3
		rr	X(rr)	99							3	5
MULT dst	dst[15:0] ← dst[15:8] * dst[7:0]	RR		F4	–	–	–	–	–	–	2	8
NOP	No operation			0F	–	–	–	–	–	–	1	2
OR dst, src	dst ← dst OR src	r	r	42	–	*	*	0	–	–	2	3
		r	Ir	43							2	4
		R	R	44							3	3
		R	IR	45							3	4
		R	IM	46							3	3
		IR	IM	47							3	4
ORX dst, src	dst ← dst OR src	ER	ER	48	–	*	*	0	–	–	4	3
		ER	IM	49							4	3
POP dst	dst ← @SP SP ← SP + 1	R		50	–	–	–	–	–	–	2	2
		IR		51							2	3

Note: Flags Notation:
* = Value is a function of the result of the operation.
– = Unaffected.
X = Undefined.
0 = Reset to 0.
1 = Set to 1.

Table 137. Op Code Map Abbreviations (Continued)

Abbreviation	Description	Abbreviation	Description
IM	Immediate data value	r2, R2, Ir2, Irr2, IR2, rr2, RR2, IRR2, ER2	Source address
Ir	Indirect working register	RA	Relative
IR	Indirect register	rr	Working register pair
Irr	Indirect working register pair	RR	Register pair

Appendix B. Register Tables

For the reader's convenience, this appendix lists all F64xx Series registers numerically by hexadecimal address.

General Purpose RAM

In the F64xx Series, the 000–FFF hexadecimal address range is partitioned for general-purpose random access memory, as follows.

Hex Addresses: 000–7FF

This address range is reserved for 2KB general-purpose register file RAM devices. For more details, see the Register File section on page 18.

Hex Addresses: 000–FFF

This address range is reserved for 4KB general-purpose register file RAM devices. For more details, see the Register File section on page 18.

Timer 0

For more information about these Timer Control registers, see the Timer Control Register Definitions section on page 72.

Hex Address: F00

Table 138. Timer 0–3 High Byte Register (TxH)

Bit	7	6	5	4	3	2	1	0
Field	TH							
RESET	0							
R/W	R/W							
Address	F00H, F08H, F10H, F18H							

Hex Address: FB4

Table 208. DMA*x* End Address Low Byte Register (DMA*x*END)

Bit	7	6	5	4	3	2	1	0
Field	DMA_END							
RESET	X							
R/W	R/W							
Address	FB4H, FBCH							

Hex Addresses: FB5–FB7

This address range is reserved.

Hex Address: FB8

Table 209. DMA*x* Control Register (DMA*x*CTL)

Bit	7	6	5	4	3	2	1	0
Field	DEN	DLE	DDIR	IRQEN	WSEL	RSS		
RESET	0							
R/W	R/W							
Address	FB0H, FB8H							

Hex Address: FB9

Table 210. DMA*x* I/O Address Register (DMA*x*IO)

Bit	7	6	5	4	3	2	1	0
Field	DMA_IO							
RESET	X							
R/W	R/W							
Address	FB1H, FB9H							

Packaging

Zilog's F64xx Series of MCUs includes the Z8F1621, Z8F2421, Z8F3221, Z8F4821 and Z8F6421 devices, which are available in the following packages:

- 40-pin Pin Dual Inline Package (PDIP)
- 44-pin Low Profile Quad Flat Package (LQFP)
- 44-pin Plastic Lead Chip Carrier (PLCC)

Zilog's F64xx Series of MCUs also includes the Z8F1622, Z8F2422, Z8F3222, Z8F4822 and Z8F6422 devices, which are available in the following packages:

- 64-pin Low-Profile Quad Flat Package (LQFP)
- 68-pin Plastic Lead Chip Carrier (PLCC)

Lastly, Zilog's F64xx Series of MCUs includes the Z8F4823 and Z8F6423 devices, which are available in the following package:

- 80-pin Quad Flat Package (QFP)

Current diagrams for each of these packages are published in Zilog's Packaging Product Specification (PS0072), which is available free for download from the Zilog website.