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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4/M0
Core Size	32-Bit Dual-Core
Speed	100MHz, 150MHz
Connectivity	I²C, LINbus, QSPI, SPI, UART/USART, USB
Peripherals	Bluetooth, Brown-out Detect/Reset, Cap Sense, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	78
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	32K x 8
RAM Size	288K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 8x12b SAR; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	116-WFBGA
Supplier Device Package	116-BGA (5.2x6.4)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c6347bzi-bld33

Functional Definition

CPU and Memory Subsystem

CPU

The CPU subsystem in the PSoC 63 consists of two Arm Cortex cores and their associated busses and memories: M4 with Floating-point unit and Memory Protection Units (FPU and MPU) and an M0+ with an MPU. The Cortex M4 and M0+ have 8 KB Instruction Caches (I-Cache) with 4-way set associativity. This subsystem also includes independent DMA controllers with 32 channels each, a Cryptographic accelerator block, 1 MB of on-chip Flash, 288 KB of SRAM, and 128 KB of ROM.

The Cortex M0+ provides a secure, un-interruptible Boot function. This guarantees that post-Boot, system integrity is checked and privileges enforced. Shared resources can be accessed through the normal Arm multi-layer bus arbitration and exclusive accesses are supported by an Inter-Processor Communication (IPC) scheme, which implements hardware semaphores and protection. Active power consumption for the Cortex M4 is 22 µA/MHz and 15 µA/MHz for the Cortex M0+, both at 3.3 V chip supply voltage with the internal buck enabled and at 0.9 V internal supply. Note that at Cortex M4 speeds above 100 MHz, the M0+ and Peripheral subsystem are limited to half the M4 speed. If the M4 is running at 150 Mhz, the M0+and peripheral subsystem is limited to 75 MHz.

DMA Controllers

There are two DMA controllers with 16 channels each. They support independent accesses to peripherals using the AHB Multi-layer bus.

Flash

PSoC 63 has a 1 MB flash module with additional 32 KB of Flash that can be used for EEPROM emulation for longer retention and a separate 32 KB block of Flash that can be securely locked and is only accessible via a key lock that cannot be changed (one Time Programmable).

SRAM with 32 KB Retention Granularity

There is 288 KB of SRAM memory, which can be fully retained or retained in increments of user-designated 32 KB blocks.

SROM

There is a supervisory 128 KB ROM that contains boot and configuration routines. This ROM will guarantee Secure Boot if authentication of User Flash is required.

One-Time-Programmable (OTP) eFuse

The 1024-bit OTP memory can provide a unique and unalterable Identifier on a per-chip basis. This unalterable key can be used to access Secured Flash.

System Resources

Power System

The power system provides assurance that voltage levels are as required for each respective mode and will either delay mode entry (on power-on reset (POR), for example) until voltage levels are as required for proper function or generate resets (Brown-Out Detect (BOD)) when the power supply drops below specified levels. The design will guaranteed safe chip operation between power supply voltage dropping below specified levels (for example, below 1.7 V) and the Reset occurring. There are no voltage sequencing requirements. The VDD core logic supply (1.7 to 3.6 V) will feed an on-chip buck, which will produce the core logic supply of either 1.1 V or 0.9 V selectable. Depending on the frequency of operation, the buck converter will have a quiescent current of <1 µA. A separate power domain called Backup is provided; note this is not a power mode. This domain is powered from the VBACKUP domain and includes the 32-kHz WCO, RTC, and backup registers. It is connected to VDD when not used as a backup domain. Port 0 is powered from this supply. Pin 5 of Port 0 (P0.5) can be assigned as a PMIC wakeup output (timed by the RTC); P0.5 is driven to the resistive pull-up mode by default.

Clock System

The PSoC 63 clock system is responsible for providing clocks to all subsystems that require clocks and for switching between different clock sources without glitching. In addition, the clock system ensures that no metastable conditions occur.

The clock system for PSoC 63 consists of the Internal Main Oscillator (IMO) and the Internal Low-speed Oscillator (ILO), crystal oscillators (ECO and WCO), PLL, FLL, and provision for an external clock. An FLL will provide fast wake-up at high clock speeds without waiting for a PLL lock event (which can take up to 50 µs). Clocks may be buffered and brought out to a pin on a Smart I/O port.

The 32-kHz oscillator is trimmable to within 2 ppm using a higher accuracy clock. The ECO will deliver ±20 ppm accuracy and will use an external crystal.

IMO Clock Source

The IMO is the primary source of internal clocking in PSoC 63. It is trimmed during testing to achieve the specified accuracy. The IMO default frequency is 8 MHz. IMO tolerance is ±2% and its current consumption is less than 10 µA.

ILO Clock Source

The ILO is a very low power oscillator, nominally 32 kHz, which may be used to generate clocks for peripheral operation in Deep Sleep mode. ILO-driven counters can be calibrated to the IMO to improve accuracy. Cypress provides a software component, which does the calibration.

Watchdog Timer

A watchdog timer is implemented in the clock block running from the ILO or from the WCO; this allows watchdog operation during Deep Sleep and Hibernate modes, and generates a watchdog reset if not serviced before the timeout occurs. The watchdog reset is recorded in the Reset Cause register.

Clock Dividers

Integer and Fractional clock dividers are provided for peripheral use and timing purposes. There are eight 8-bit integer and sixteen 16-bit integer clock dividers. There is also one 24.5-bit fractional and four 16.5-bit fractional clock dividers.

Reset

The PSoC 63 can be reset from a variety of sources including a software reset. Reset events are asynchronous and guarantee reversion to a known state. The reset cause is recorded in a register, which is sticky through reset and allows software to determine the cause of the Reset. An XRES pin is reserved for external reset to avoid complications with configuration and multiple pin functions during power-on or reconfiguration.

BLE Radio and Subsystem

PSoC 63 incorporates a Bluetooth Smart subsystem that contains the Physical Layer (PHY) and Link Layer (LL) engines with an embedded security engine. The physical layer consists of the digital PHY and the RF transceiver that transmits and receives GFSK packets at 2 Mbps over a 2.4-GHz ISM band, which is compliant with Bluetooth Smart Bluetooth Specification 5.0. The baseband controller is a composite hardware and firmware implementation that supports both master and slave modes. Key protocol elements, such as HCI and link control, are implemented in firmware. Time-critical functional blocks, such as encryption, CRC, data whitening, and access code correlation, are implemented in hardware (in the LL engine).

The RF transceiver contains an integrated balun, which provides a single-ended RF port pin to drive a 50-Ω antenna via a matching/filtering network. In the receive direction, this block converts the RF signal from the antenna to a digital bit stream after performing GFSK demodulation. In the transmit direction, this block performs GFSK modulation and then converts a digital baseband signal to a radio frequency before transmitting it to air through the antenna.

Key features of BLESS are as follows:

- Master and slave single-mode protocol stack with logical link control and adaptation protocol (L2CAP), attribute (ATT), and security manager (SM) protocols
- API access to generic attribute profile (GATT), generic access profile (GAP), and L2CAP
- L2CAP connection-oriented channel (Bluetooth 4.1 feature)
- GAP features
  - Broadcaster, Observer, Peripheral, and Central roles
  - Security mode 1: Level 1, 2, and 3
  - User-defined advertising data
  - Multiple bond support
- GATT features
  - GATT client and server
  - Supports GATT sub-procedures
  - 32-bit universally unique identifier (UUID) (Bluetooth 4.1 feature)
- Security Manager (SM)
  - Pairing methods: Just works, Passkey Entry, and Out of Band
  - LE Secure Connection Pairing model
  - Authenticated man-in-the-middle (MITM) protection and data signing
- Link Layer (LL)
  - Master and Slave roles
  - 128-bit AES engine
  - Low-duty cycle advertising
  - LE Ping
- Supports all SIG-adopted BLE profiles
- Power levels for Adv (1.28s, 31 bytes, 0 dBm) and Con (300 ms, 0 byte, 0 dBm) are 42 µW and 70 µW respectively

Analog Blocks

12-bit SAR ADC

The 12-bit, 1-Msps SAR ADC can operate at a maximum clock rate of 18 MHz and requires a minimum of 18 clocks at that frequency to do a 12-bit conversion.

The block functionality is augmented for the user by adding a reference buffer to it (trimmable to ±1%) and by providing the choice of three internal voltage references, V_{DD}, $V_{DD}/2$, and V_{REF} (nominally 1.024 V), as well as an external reference through a GPIO pin. The Sample-and-Hold (S/H) aperture is programmable; it allows the gain bandwidth requirements of the amplifier driving the SAR inputs, which determine its settling time, to be relaxed if required. System performance will be 65 dB for true 12-bit precision provided appropriate references are used and system noise levels permit it. To improve the performance in noisy conditions, it is possible to provide an external bypass (through a fixed pin location) for the internal reference amplifier.

The SAR is connected to a fixed set of pins through an 8-input sequencer. The sequencer cycles through the selected channels autonomously (sequencer scan) and does so with zero switching overhead (that is, the aggregate sampling bandwidth is equal to 1 Msps whether it is for a single channel or distributed over several channels). The sequencer switching is effected through a state machine or through firmware-driven switching. A feature provided by the sequencer is the buffering of each channel to reduce CPU interrupt-service requirements. To accommodate signals with varying source impedances and frequencies, it is possible to have different sample times programmable for each channel. Also, the signal range specification through a pair of range registers (low and high range values) is implemented with a corresponding out-of-range interrupt if the digitized value exceeds the programmed range; this allows fast detection of out-of-range values without having to wait for a sequencer scan to be completed and the CPU to read the values and check for out-of-range values in software. There are 16 channels of which any 13 can be sampled in a single scan.

The SAR is able to digitize the output of the on-chip temperature sensor for calibration and other temperature-dependent functions. The SAR is not available in Deep Sleep and Hibernate modes as it requires a high-speed clock (up to 18 MHz). The SAR operating range is 1.71 V to 3.6 V.

Temperature Sensor

PSoC 63 has an on-chip temperature sensor. This consists of a diode, which is biased by a current source that can be disabled to save power. The temperature sensor is connected to the ADC, which digitizes the reading and produces a temperature value by using a Cypress-supplied software that includes calibration and linearization.

12-bit Digital-Analog Converter

There is a 12-bit voltage mode DAC on the chip, which can settle in less than 5 µs. The DAC may be driven by the DMA controllers to generate user-defined waveforms. The DAC output from the chip can either be the resistive ladder output (highly linear near ground) or a buffered output.

Continuous Time Block (CTBm) with Two Opamps

This block consists of two opamps, which have their inputs and outputs connected to fixed pins and have three power modes and a comparator mode. The outputs of these opamps can be used as buffers for the SAR inputs. The non-inverting inputs of these opamps can be connected to either of two pins, thus allowing independent sensors to be used at different times. The pin selection can be made via firmware. The opamps can be set to one of the four power levels; the lowest level allowing operation in Deep Sleep mode in order to preserve lower performance Continuous-Time functionality in Deep Sleep mode. The DAC output can be buffered through an opamp.

Low-Power Comparators

PSoC 63 has a pair of low-power comparators, which can also operate in Deep Sleep and Hibernate modes. This allows the analog system blocks to be disabled while retaining the ability to monitor external voltage levels during Deep Sleep and Hibernate modes. The comparator outputs are normally synchronized to avoid metastability unless operating in an asynchronous power mode (Hibernate) where the system wake-up circuit is activated by a comparator-switch event.

Programmable Digital

Smart I/O

There are two Smart I/O blocks, which allow Boolean operations on signals going to the GPIO pins from the subsystems of the chip or on signals coming into the chip. Operation can be synchronous or asynchronous and the blocks operate in low-power modes, such as Deep Sleep and Hibernate.This allows, for example, detection of logic conditions that can indicate that the CPU should wake up instead of waking up on general I/O interrupts, which consume more power and can generate spurious wake-ups.

Universal Digital Blocks (UDBs) and Port Interfaces

PSoC 63 has 12 UDBs; the UDB array also provides a switched Digital System Interconnect (DSI) fabric that allows signals from peripherals and ports to be routed to and through the UDBs for communication and control.

Fixed-Function Digital

Timer/Counter/PWM Block

The timer/counter/PWM block consists of 32 counters with user-programmable period length. There is a Capture register to record the count value at the time of an event (which may be an I/O event), a period register which is used to either stop or auto-reload the counter when its count is equal to the period register, and compare registers to generate compare value signals which are used as PWM duty cycle outputs. The block also provides true and complementary outputs with programmable offset between them to allow the use as deadband programmable complementary PWM outputs. It also has a Kill input to force outputs to a predetermined state; for example, this is used in motor-drive systems when an overcurrent state is indicated and the PWMs driving the FETs need to be shut off immediately with no time for software intervention. There are eight 32-bit counters and 24 16-bit counters.

Serial Communication Blocks (SCB)

PSoC 63 has nine SCBs, which can each implement an I^2C, UART, or SPI interface. One SCB will operate in Deep Sleep with an external clock, this SCB will only operate in Slave mode (requires external clock).

I^2C Mode: The hardware I^2C block implements a full multi-master and slave interface (it is capable of multimaster arbitration). This block is capable of operating at speeds of up to 1 Mbps (Fast Mode Plus) and has flexible buffering options to reduce the interrupt overhead and latency for the CPU. It also supports EzI^2C that creates a mailbox address range in the memory of PSoC 63 and effectively reduces the I^2C communication to reading from and writing to an array in the memory. In addition, the block supports a 256 byte FIFO for receive and transmit, which, by increasing the time given for the CPU to read the data, greatly reduces the need for clock stretching caused by the CPU not having read the data on time. The FIFO mode is available in all channels and is very useful in the absence of DMA.

The I^2C peripheral is compatible with I^2C Standard-mode, Fast-mode, and Fast-Mode Plus devices as defined in the NXP I^2C-bus specification and user manual (UM10204). The I^2C bus I/O is implemented with GPIO in open-drain modes.

UART Mode: This is a full-feature UART operating at up to 8 Mbps. It supports automotive single-wire interface (LIN), infrared interface (IrDA), and SmartCard (ISO7816) protocols, all of which are minor variants of the basic UART protocol. In addition, it supports the 9-bit multiprocessor mode that allows the addressing of peripherals connected over common RX and TX lines. Common UART functions such as parity error, break detect, and frame error are supported. A 256 byte FIFO allows much greater CPU service latencies to be tolerated.

SPI Mode: The SPI mode supports full Motorola SPI, TI Secure Simple Pairing (SSP) (essentially adds a start pulse that is used to synchronize SPI Codecs), and National Microwire (half-duplex form of SPI). The SPI block can use the FIFO and supports an EzSPI mode in which the data interchange is reduced to reading and writing an array in memory. The SPI interface operates with up to a 25-MHz SPI clock.

USB Full-Speed Dual Role Host and Device Interface

PSoC 63 incorporates a dual-role USB Host and Device interface. The device can have up to eight endpoints. A 512byte SRAM buffer is provided and DMA is supported.

QSPI Interface

A Quad SPI (QSPI) interface is provided running at 80 MHz. This block also supports on-the-fly encryption and decryption to support Execute-In-Place operation at reasonable speeds. It supports Single/dual/quad/octal SPI and dual-quad SPI modes.

GPIO

PSoC 63 has up to 78 GPIOs. The GPIO block implements the following:

- Eight drive strength modes:
  - Analog input mode (input and output buffers disabled)
  - Input only
  - Weak pull-up with strong pull-down
  - Strong pull-up with weak pull-down
  - Open drain with strong pull-down
  - Open drain with strong pull-up
  - Strong pull-up with strong pull-down
  - Weak pull-up with weak pull-down
- Input threshold select (CMOS or LVTTL)
- Hold mode for latching previous state (used for retaining the I/O state in Deep Sleep and Hibernate modes)
- Selectable slew rates for dV/dt-related noise control to improve EMI

The pins are organized in logical entities called ports, which are 8-bit in width. During power-on and reset, the blocks are forced to the disable state so as not to crowbar any inputs and/or cause excess turn-on current. A multiplexing network known as a high-speed I/O matrix (HSIOM) is used to multiplex between various signals that may connect to an I/O pin. Data output and pin state registers store, respectively, the values to be driven on the pins and the states of the pins themselves.

Every I/O pin can generate an interrupt if so enabled and each I/O port has an interrupt request (IRQ) and interrupt service routine (ISR) vector associated with it. Six GPIO pins are capable of overvoltage tolerant (OVT) operation where the input voltage may be higher than VDD (these may be used for I^2C functionality to allow powering the chip off while maintaining physical connection to an operating I^2C bus without affecting its functionality).

GPIO pins can be ganged to sink 16 mA or higher values of sink current. GPIO pins, including OVT pins, may not be pulled up higher than 3.6 V.

Special-Function Peripherals

CapSense

CapSense is supported on all pins in the PSoC 63 through a CapSense Sigma-Delta (CSD) block that can be connected to an analog multiplexed bus. Any GPIO pin can be connected to this AMUX bus through an analog switch. CapSense function can thus be provided on any pin or a group of pins in a system under software control. Cypress provides a software component for the CapSense block for ease-of-use.

Shield voltage can be driven on another mux bus to provide water-tolerance capability. Water tolerance is provided by driving the shield electrode in phase with the sense electrode to keep the shield capacitance from attenuating the sensed input. Proximity sensing can also be implemented.

The CapSense block is an advanced, low-noise, programmable block with programmable voltage references and current source ranges for improved sensitivity and flexibility. It can also use an external reference voltage. It has a full-wave CSD mode that alternates sensing to VDDA and ground to null out power-supply related noise.

The CapSense block has two 7-bit IDACs, which can be used for general purposes if CapSense is not being used (both IDACs are available in that case) or if CapSense is used without water tolerance (one IDAC is available). A (slow) 10-bit Slope ADC may be realized by using one of the IDACs.

The block can implement Swipe, Tap, Wake-up on Touch (< 3 µA at 1.8 V), mutual capacitance, and other types of sensing functions.

Audio Subsystem

This subsystem consists of an I2S block and two PDM channels. The PDM channels interface to a PDM microphone's bit-stream output. The PDM processing channel provides droop correction and can operate with clock speeds ranging from 384 kHz to 3.072 MHz and produce word lengths of 16 to 24 bits at audio sample rates of up to 48 ksps.

The I2S interface supports both Master and Slave modes with Word Clock rates of up to 192 ksps (8-bit to 32-bit words).

Each Port Pin has multiple alternate functions. These are defined in Table 2.

Table 2. Multiple Alternate Functions

Port/ Pin	ACT #0	ACT #1	DS #2	ACT #4	ACT #5	ACT #6	ACT #7	ACT #8	ACT #9	ACT #10	ACT #12	ACT #13	ACT #14	ACT #15	DS #4	DS #5	DS #6
P0.0	tcpwm[0].line[0]:0	tcpwm[1].line[0]:0		srss.ext_clk:0				scb[0].spi_select1:0			peri.tr_io_input[0]:0						
P0.1	tcpwm[0].line_compl[0]:0	tcpwm[1].line_compl[0]:0						scb[0].spi_select2:0			peri.tr_io_input[1]:0					cpuss.swj_trstn	
P0.2	tcpwm[0].line[1]:0	tcpwm[1].line[1]:0				scb[0].uart_rx:0	scb[0].i2c_scl:0	scb[0].spi_mosi:0									
P0.3	tcpwm[0].line_compl[1]:0	tcpwm[1].line_compl[1]:0				scb[0].uart_tx:0	scb[0].i2c_sda:0	scb[0].spi_miso:0									
P0.4	tcpwm[0].line[2]:0	tcpwm[1].line[2]:0				scb[0].uart_rts:0		scb[0].spi_clk:0				peri.tr_io_output[0]:2					
P0.5	tcpwm[0].line_compl[2]:0	tcpwm[1].line_compl[2]:0		srss.ext_clk:1		scb[0].uart_cts:0		scb[0].spi_select0:0				peri.tr_io_output[1]:2					
P1.0	tcpwm[0].line[3]:0	tcpwm[1].line[3]:0				scb[7].uart_rx:0	scb[7].i2c_scl:0	scb[7].spi_mosi:0			peri.tr_io_input[2]:0						
P1.1	tcpwm[0].line_compl[3]:0	tcpwm[1].line_compl[3]:0				scb[7].uart_tx:0	scb[7].i2c_sda:0	scb[7].spi_miso:0			peri.tr_io_input[3]:0						
P1.2	tcpwm[0].line[4]:4	tcpwm[1].line[12]:1				scb[7].uart_rts:0		scb[7].spi_clk:0									
P1.3	tcpwm[0].line_compl[4]:4	tcpwm[1].line_compl[12]:1				scb[7].uart_cts:0		scb[7].spi_select0:0									
P1.4	tcpwm[0].line[5]:4	tcpwm[1].line[13]:1						scb[7].spi_select1:0									
P1.5	tcpwm[0].line_compl[5]:4	tcpwm[1].line_compl[14]:1						scb[7].spi_select2:0									
P5.0	tcpwm[0].line[4]:0	tcpwm[1].line[4]:0				scb[5].uart_rx:0	scb[5].i2c_scl:0	scb[5].spi_mosi:0		audioss.clk_i2s_if	peri.tr_io_input[10]:0						
P5.1	tcpwm[0].line_compl[4]:0	tcpwm[1].line_compl[4]:0				scb[5].uart_tx:0	scb[5].i2c_sda:0	scb[5].spi_miso:0		audioss.tx_sck	peri.tr_io_input[11]:0						
P5.2	tcpwm[0].line[5]:0	tcpwm[1].line[5]:0				scb[5].uart_rts:0		scb[5].spi_clk:0		audioss.tx_ws							
P5.3	tcpwm[0].line_compl[5]:0	tcpwm[1].line_compl[5]:0				scb[5].uart_cts:0		scb[5].spi_select0:0		audioss.tx_sdo							
P5.4	tcpwm[0].line[6]:0	tcpwm[1].line[6]:0						scb[5].spi_select1:0		audioss.rx_sck							
P5.5	tcpwm[0].line_compl[6]:0	tcpwm[1].line_compl[6]:0						scb[5].spi_select2:0		audioss.rx_ws							

Table 2. Multiple Alternate Functions *(continued)*

Port/ Pin	ACT #0	ACT #1	DS #2	ACT #4	ACT #5	ACT #6	ACT #7	ACT #8	ACT #9	ACT #10	ACT #12	ACT #13	ACT #14	ACT #15	DS #4	DS #5	DS #6
P8.0	tcpwm[0].line[0]:2	tcpwm[1].line[16]:0				scb[4].uart_rx:0	scb[4].i2c_scl:0	scb[4].spi_mosi:0			peri.tr_io_input[16]:0						
P8.1	tcpwm[0].line_compl[0]:2	tcpwm[1].line_compl[16]:0				scb[4].uart_tx:0	scb[4].i2c_sda:0	scb[4].spi_miso:0			peri.tr_io_input[17]:0						
P8.2	tcpwm[0].line[1]:2	tcpwm[1].line[17]:0				scb[4].uart_rts:0		scb[4].spi_clk:0									
P8.3	tcpwm[0].line_compl[1]:2	tcpwm[1].line_compl[17]:0				scb[4].uart_cts:0		scb[4].spi_select0:0									
P8.4	tcpwm[0].line[2]:2	tcpwm[1].line[18]:0						scb[4].spi_select1:0									
P8.5	tcpwm[0].line_compl[2]:2	tcpwm[1].line_compl[18]:0						scb[4].spi_select2:0									
P8.6	tcpwm[0].line[3]:2	tcpwm[1].line[19]:0						scb[4].spi_select3:0									
P8.7	tcpwm[0].line_compl[3]:2	tcpwm[1].line_compl[19]:0						scb[3].spi_select2:0									
P9.0	tcpwm[0].line[4]:2	tcpwm[1].line[20]:0				scb[2].uart_rx:0	scb[2].i2c_scl:0	scb[2].spi_mosi:0			peri.tr_io_input[18]:0			cpuss.trace_data[3]:0			
P9.1	tcpwm[0].line_compl[4]:2	tcpwm[1].line_compl[20]:0				scb[2].uart_tx:0	scb[2].i2c_sda:0	scb[2].spi_miso:0			peri.tr_io_input[19]:0			cpuss.trace_data[2]:0			
P9.2	tcpwm[0].line[5]:2	tcpwm[1].line[21]:0				scb[2].uart_rts:0		scb[2].spi_clk:0		pass.dsi_ctb_cmp0:1				cpuss.trace_data[1]:0			
P9.3	tcpwm[0].line_compl[5]:2	tcpwm[1].line_compl[21]:0				scb[2].uart_cts:0		scb[2].spi_select0:0		pass.dsi_ctb_cmp1:1				cpuss.trace_data[0]:0			
P9.4	tcpwm[0].line[7]:5	tcpwm[1].line[0]:2						scb[2].spi_select1:0									
P9.5	tcpwm[0].line_compl[7]:5	tcpwm[1].line_compl[0]:2						scb[2].spi_select2:0									
P9.6	tcpwm[0].line[0]:6	tcpwm[1].line[1]:2						scb[2].spi_select3:0									
P9.7	tcpwm[0].line_compl[0]:6	tcpwm[1].line_compl[1]:2															
P10.0	tcpwm[0].line[6]:2	tcpwm[1].line[22]:0				scb[1].uart_rx:1	scb[1].i2c_scl:1	scb[1].spi_mosi:1			peri.tr_io_input[20]:0			cpuss.trace_data[3]:1			
P10.1	tcpwm[0].line_compl[6]:2	tcpwm[1].line_compl[22]:0				scb[1].uart_tx:1	scb[1].i2c_sda:1	scb[1].spi_miso:1			peri.tr_io_input[21]:0			cpuss.trace_data[2]:1			

Table 2. Multiple Alternate Functions *(continued)*

Port/ Pin	ACT #0	ACT #1	DS #2	ACT #4	ACT #5	ACT #6	ACT #7	ACT #8	ACT #9	ACT #10	ACT #12	ACT #13	ACT #14	ACT #15	DS #4	DS #5	DS #6
P10.2	tcpwm[0].line[7]:2	tcpwm[1].line[23]:0				scb[1].uart_rts:1		scb[1].spi_clk:1						cpuss.trace_data[1]:1			
P10.3	tcpwm[0].line_compl[7]:2	tcpwm[1].line_compl[23]:0				scb[1].uart_cts:1		scb[1].spi_select0:1						cpuss.trace_data[0]:1			
P10.4	tcpwm[0].line[0]:3	tcpwm[1].line[0]:1						scb[1].spi_select1:1	audioss.pdm_clk								
P10.5	tcpwm[0].line_compl[0]:3	tcpwm[1].line_compl[0]:1						scb[1].spi_select2:1	audioss.pdm_data								
P10.6	tcpwm[0].line[1]:6	tcpwm[1].line[2]:2						scb[1].spi_select3:1									
P10.7	tcpwm[0].line_compl[1]:6	tcpwm[1].line_compl[2]:2															
P11.0	tcpwm[0].line[1]:3	tcpwm[1].line[1]:1			smif.spi_select2	scb[5].uart_rx:1	scb[5].i2c_scl:1	scb[5].spi_mosi:1			peri.tr_io_input[22]:0						
P11.1	tcpwm[0].line_compl[1]:3	tcpwm[1].line_compl[1]:1			smif.spi_select1	scb[5].uart_tx:1	scb[5].i2c_sda:1	scb[5].spi_miso:1			peri.tr_io_input[23]:0						
P11.2	tcpwm[0].line[2]:3	tcpwm[1].line[2]:1			smif.spi_select0	scb[5].uart_rts:1		scb[5].spi_clk:1									
P11.3	tcpwm[0].line_compl[2]:3	tcpwm[1].line_compl[2]:1			smif.spi_data3	scb[5].uart_cts:1		scb[5].spi_select0:1				peri.tr_io_output[0]:0					
P11.4	tcpwm[0].line[3]:3	tcpwm[1].line[3]:1			smif.spi_data2			scb[5].spi_select1:1				peri.tr_io_output[1]:0					
P11.5	tcpwm[0].line_compl[3]:3	tcpwm[1].line_compl[3]:1			smif.spi_data1			scb[5].spi_select2:1									
P11.6					smif.spi_data0			scb[5].spi_select3:1									
P11.7					smif.spi_clk												
P12.0	tcpwm[0].line[4]:3	tcpwm[1].line[4]:1			smif.spi_data4	scb[6].uart_rx:0	scb[6].i2c_scl:0	scb[6].spi_mosi:0			peri.tr_io_input[24]:0						
P12.1	tcpwm[0].line_compl[4]:3	tcpwm[1].line_compl[4]:1			smif.spi_data5	scb[6].uart_tx:0	scb[6].i2c_sda:0	scb[6].spi_miso:0			peri.tr_io_input[25]:0						
P12.2	tcpwm[0].line[5]:3	tcpwm[1].line[5]:1			smif.spi_data6	scb[6].uart_rts:0		scb[6].spi_clk:0									
P12.3	tcpwm[0].line_compl[5]:3	tcpwm[1].line_compl[5]:1			smif.spi_data7	scb[6].uart_cts:0		scb[6].spi_select0:0									
P12.4	tcpwm[0].line[6]:3	tcpwm[1].line[6]:1			smif.spi_select3			scb[6].spi_select1:0	audioss.pdm_clk								

Table 5. Power Supply Range, CPU Current, and Transition Time Specifications *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SID7F	V_{DDUSB}	Supply for Port 14 (USB or GPIO) when present	1.7	–	3.6	V	Min supply is 2.85 V for USB
SID6B	V_{BACKUP}	Backup Power and GPIO Port 0 supply when present	1.7	–	3.6	V	Min is 1.4 V in Backup mode
SID8	V_{CCD1}	Output voltage (for core logic bypass)	–	1.1	–	V	High-speed mode
SID9	V_{CCD2}	Output voltage (for core logic bypass)	–	0.9	–		ULP mode. Valid for –20 to 85 °C
SID10	C_{EFC}	External regulator voltage (V_{CCD}) bypass	3.8	4.7	5.6	µF	X5R ceramic or better
SID11	C_{EXC}	Power supply decoupling capacitor	–	10	–	µF	X5R ceramic or better
LP RANGE POWER SPECIFICATIONS (for V_{CCD} = 1.1 V with Buck and LDO)							
Cortex M4. Active Mode							
Execute with Cache Disabled (Flash)							
SIDF1	I_{DD1}	Execute from Flash; CM4 Active 50 MHz, CM0+ Sleep 25 MHz. With IMO & FLL. While(1).	–	2.3	3.2	mA	V_{DDD} = 3.3 V, Buck ON, max at 60 °C
			–	3.1	3.6		V_{DDD} = 1.8 V, Buck ON, max at 60 °C
			–	4.2	5.1		V_{DDD} = 1.8 to 3.3 V, LDO, max at 60 °C
SIDF2	I_{DD2}	Execute from Flash; CM4 Active 8 MHz, CM0+ Sleep 8 MHz.With IMO. While(1)	–	0.9	1.5	mA	V_{DDD} = 3.3 V, Buck ON, max at 60 °C
			–	1.2	1.6		V_{DDD} = 1.8 V, Buck ON, max at 60 °C
			–	1.6	2.4		V_{DDD} = 1.8 to 3.3 V, LDO, max at 60 °C
Execute with Cache Enabled							
SIDC1	I_{DD3}	Execute from Cache;CM4 Active 150 MHz, CM0+ Sleep 75 MHz. IMO & FLL. Dhrystone.	–	6.3	7	mA	V_{DDD} = 3.3 V, Buck ON, max at 60 °C
			–	9.7	11.2		V_{DDD} = 1.8 V, Buck ON, max at 60 °C
			–	13.2	13.7		V_{DDD} = 1.8 to 3.3 V, LDO, max at 60 °C
SIDC2	I_{DD4}	Execute from Cache;CM4 Active 100 MHz, CM0+ Sleep 100MHz. IMO & FLL. Dhrystone.	–	4.8	5.8	mA	V_{DDD} = 3.3 V, Buck ON, max at 60 °C
			–	7.4	8.4		V_{DDD} = 1.8 V, Buck ON, max at 60 °C
			–	10.1	10.7		V_{DDD} = 1.8 to 3.3 V, LDO, max at 60 °C
SIDC3	I_{DD5}	Execute from Cache;CM4 Active 50 MHz, CM0+ Sleep 25MHz. IMO & FLL. Dhrystone	–	2.4	3.4	mA	V_{DDD}=3.3 V, Buck ON, max at 60 °C
			–	3.7	4.1		V_{DDD} = 1.8V, Buck ON, max at 60 °C
			–	5.1	5.8		V_{DDD} = 1.8 to 3.3 V, LDO, max at 60 °C
SIDC4	I_{DD6}	Execute from Cache;CM4 Active 8 MHz, CM0+ Sleep 8 MHz. IMO. Dhrystone	–	0.90	1.5	mA	V_{DDD} = 3.3 V, Buck ON, max at 60 °C
			–	1.27	1.75		V_{DDD} = 1.8 V, Buck ON, max at 60 °C
			–	1.8	2.6		V_{DDD} = 1.8 to 3.3 V, LDO, max at 60 °C

Table 5. Power Supply Range, CPU Current, and Transition Time Specifications *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
Cortex M0+. Low Power Sleep (LPS) Mode							
SIDLPS3	I_{DD22}	CM4 Off, CM0+ LPS 8 MHz. With IMO.	–	0.64	1.1	mA	V_{DDD} = 3.3 V, Buck ON, max at 60 °C
			–	0.93	1.45		V_{DDD} = 1.8 V, Buck ON, max at 60 °C
			–	1.29	2		V_{DDD} = 1.8 to 3.3 V, LDO, max at 60 °C
ULP RANGE POWER SPECIFICATIONS (for V_{CCD} = 0.9 V using the Buck). ULP mode is valid from –20 to +85 °C.							
Cortex M4. Active Mode							
Execute with Cache Disabled (Flash)							
SIDF5	I_{DD3}	Execute from Flash; CM4 Active 50 MHz, CM0+ Sleep 25 MHz. With IMO & FLL. While(1).	–	1.7	2.2	mA	V_{DDD} = 3.3 V, Buck ON, max at 60 °C
			–	2.1	2.4		V_{DDD} = 1.8 V, Buck ON, max at 60 °C
SIDF6	I_{DD4}	Execute from Flash; CM4 Active 8 MHz, CM0+ Sleep 8 MHz. With IMO. While (1)	–	0.56	0.8	mA	V_{DDD} = 3.3 V, Buck ON, max at 60 °C
			–	0.75	1		V_{DDD} = 1.8 V, Buck ON, max at 60 °C
Execute with Cache Enabled							
SIDC8	I_{DD10}	Execute from Cache; CM4 Active 50 MHz, CM0+ Sleep 25 MHz. With IMO & FLL. Dhrystone.	–	1.6	2.2	mA	V_{DDD} = 3.3 V, Buck ON, max at 60 °C
			–	2.4	2.7		V_{DDD} = 1.8 V, Buck ON, max at 60 °C
SIDC9	I_{DD11}	Execute from Cache; CM4 Active 8 MHz, CM0+ Sleep 8 MHz. With IMO. Dhrystone.	–	0.65	0.8	mA	V_{DDD} = 3.3 V, Buck ON, max at 60 °C
			–	0.8	1.1		V_{DDD} = 1.8 V, Buck ON, max at 60 °C
Cortex M0+. Active Mode							
Execute with Cache Disabled (Flash)							
SIDF7	I_{DD16}	Execute from Flash; CM4 Off, CM0+ Active 25 MHz. With IMO & FLL. Write(1).	–	1.00	1.4	mA	V_{DDD} = 3.3 V, Buck ON, max at 60 °C
			–	1.34	1.6		V_{DDD} = 1.8 V, Buck ON, max at 60 °C
SIDF8	I_{DD17}	Execute from Flash; CM4 Off, CM0+ Active 8 MHz. With IMO. While(1)	–	0.54	0.75	mA	V_{DDD} = 3.3 V, Buck ON, max at 60 °C
			–	0.73	1		V_{DDD} = 1.8 V, Buck ON, max at 60 °C
Execute with Cache Enabled							
SIDC10	I_{DD18}	Execute from Cache; CM4 Off, CM0+ Active 25 MHz. With IMO & FLL. Dhrystone.	–	0.91	1.25	mA	V_{DDD} = 3.3 V, Buck ON, max at 60 °C
			–	1.34	1.6		V_{DDD} = 1.8 V, Buck ON, max at 60 °C
SIDC11	I_{DD19}	Execute from Cache; CM4 Off, CM0+ Active 8 MHz. With IMO. Dhrystone.	–	0.51	0.72	mA	V_{DDD} = 3.3 V, Buck ON, max at 60 °C
			–	0.73	0.95		V_{DDD} = 1.8 V, Buck ON, max at 60 °C

GPIO

Table 7. GPIO Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
GPIO DC Specifications							
SID57	V_{IH}	Input voltage high threshold	0.7 * V_{DD}	–	–	V	CMOS Input
SID57A	I_{IHS}	Input current when Pad > VDDIO for OVT inputs	–	–	10	µA	Per I^2C Spec
SID58	V_{IL}	Input voltage low threshold	–	–	0.3 * V_{DD}	V	CMOS Input
SID241	V_{IH}	LVTTL input, V_{DD} < 2.7 V	0.7 * V_{DD}	–	–	V	
SID242	V_{IL}	LVTTL input, V_{DD} < 2.7 V	–	–	0.3*V_{DD}	V	
SID243	V_{IH}	LVTTL input, V_{DD} ≥ 2.7 V	2.0	–	–	V	
SID244	V_{IL}	LVTTL input, V_{DD} ≥ 2.7 V	–	–	0.8	V	
SID59	V_{OH}	Output voltage high level	V_{DD} – 0.5	–	–	V	I_{OH} = 8 mA
SID62A	V_{OL}	Output voltage low level	–	–	0.4	V	I_{OL} = 8 mA
SID63	R_{PULLUP}	Pull-up resistor	3.5	5.6	8.5	kΩ	
SID64	$R_{PULLDOWN}$	Pull-down resistor	3.5	5.6	8.5	kΩ	
SID65	I_{IL}	Input leakage current (absolute value)	–	–	2	nA	25 °C, V_{DD} = 3.0 V
SID65A	I_{IL_CTBM}	Input leakage on CTBm input pins	–	–	4	nA	
SID66	C_{IN}	Input Capacitance	–	–	5	pF	
SID67	V_{HYSTTL}	Input hysteresis LVTTL V_{DD} > 2.7 V	100	0	–	mV	
SID68	$V_{HYSCMOS}$	Input hysteresis CMOS	0.05 * V_{DD}	–	–	mV	
SID69	I_{DIODE}	Current through protection diode to V_{DD}/V_{SS}	–	–	100	µA	
SID69A	I_{TOT_GPIO}	Maximum Total Source or Sink Chip Current	–	–	200	mA	
GPIO AC Specifications							
SID70	T_{RISEF}	Rise time in Fast Strong Mode. 10% to 90% of V_{DD}	–	–	2.5	ns	Cload = 15 pF, 8 mA drive strength
SID71	T_{FALLF}	Fall time in Fast Strong Mode. 10% to 90% of V_{DD}	–	–	2.5	ns	Cload = 15 pF, 8 mA drive strength
SID72	T_{RISES_1}	Rise time in Slow Strong Mode. 10% to 90% of V_{DD}	52	–	142	ns	Cload = 15 pF, 8 mA drive strength, V_{DD} ≤ 2.7 V
SID72A	T_{RISES_2}	Rise time in Slow Strong Mode. 10% to 90% of V_{DD}	48	–	102	ns	Cload = 15 pF, 8 mA drive strength, 2.7 V < V_{DD} ≤ 3.6 V
SID73	T_{FALLS_1}	Fall time in Slow Strong Mode. 10% to 90% of V_{DD}	44	–	211	ns	Cload = 15 pF, 8 mA drive strength, V_{DD} ≤ 2.7 V
SID73A	T_{FALLS_2}	Fall time in Slow Strong Mode. 10% to 90% of V_{DD}	42	–	93	ns	Cload = 15 pF, 8 mA drive strength, 2.7 V < V_{DD} ≤ 3.6 V
SID73G	T_{FALL_I2C}	Fall time (30% to 70% of V_{DD}) in Slow Strong mode	20 * V_{DDIO} / 5.5	–	250	ns	Cload = 10 pF to 400 pF, 8-mA drive strength
SID74	$F_{GPIOUT1}$	GPIO Fout. Fast Strong mode.	–	–	100	MHz	90/10%, 15-pF load, 60/40 duty cycle

Table 7. GPIO Specifications *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SID75	$F_{GPIOUT2}$	GPIO Fout; Slow Strong mode.	–	–	16.7	MHz	90/10%, 15-pF load, 60/40 duty cycle
SID76	$F_{GPIOUT3}$	GPIO Fout; Fast Strong mode.	–	–	7	MHz	90/10%, 25-pF load, 60/40 duty cycle
SID245	$F_{GPIOUT4}$	GPIO Fout; Slow Strong mode.	–	–	3.5	MHz	90/10%, 25-pF load, 60/40 duty cycle
SID246	F_{GPIOIN}	GPIO input operating frequency;1.71 V ≤ V_{DD} ≤ 3.6 V	–	–	100	MHz	90/10% V_{IO}

Analog Peripherals

Opamp

Table 8. Opamp Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
	I_{DD}	Opamp Block current. No load.	–	–	–		–
SID269	I_{DD_HI}	Power = Hi	–	1300	1500	µA	–
SID270	I_{DD_MED}	Power = Med	–	450	600	µA	–
SID271	I_{DD_LOW}	Power = Lo	–	250	350	µA	–
	GBW	Load = 20 pF, 0.1 mA. V_{DDA} = 2.7 V	–	–	–		–
SID272	G_{BW_HI}	Power = Hi	6	–	–	MHz	–
SID273	G_{BW_MED}	Power = Med	4	–	–	MHz	–
SID274	G_{BW_LO}	Power = Lo	–	1	–	MHz	–
	I_{OUT_MAX}	V_{DDA} ≥ 2.7 V, 500 mV from rail	–	–	–		–
SID275	$I_{OUT\_MAX\_HI}$	Power = Hi	10	–	–	mA	–
SID276	$I_{OUT\_MAX\_MID}$	Power = Mid	10	–	–	mA	–
SID277	$I_{OUT\_MAX\_LO}$	Power = Lo	–	5	–	mA	–
	I_{OUT}	V_{DDA} = 1.71 V, 500 mV from rail	–	–	–		–
SID278	$I_{OUT\_MAX\_HI}$	Power = Hi	4	–	–	mA	–
SID279	$I_{OUT\_MAX\_MID}$	Power = Mid	4	–	–	mA	–
SID280	$I_{OUT\_MAX\_LO}$	Power = Lo	–	2	–	mA	–
SID281	V_{IN}	Input voltage range	0	–	V_{DDA} – 0.2	V	–
SID282	V_{CM}	Input common mode voltage	0	–	V_{DDA} – 0.2	V	–
	V_{OUT}	V_{DDA} ≥ 2.7 V	–	–	–		–
SID283	V_{OUT_1}	Power = hi, Iload = 10 mA	0.5	–	V_{DDA} – 0.5	V	–
SID284	V_{OUT_2}	Power = hi, Iload = 1 mA	0.2	–	V_{DDA} – 0.2	V	–
SID285	V_{OUT_3}	Power = med, Iload = 1 mA	0.2	–	V_{DDA} – 0.2	V	–
SID286	V_{OUT_4}	Power = lo, Iload = 0.1 mA	0.2	–	V_{DDA} – 0.2	V	–
SID287	V_{OS_UNTR}	Offset voltage, untrimmed	–	–	–	mV	–
SID288	V_{OS_TR}	Offset voltage, trimmed	–1	±0.5	1	mV	High mode, 0.2 to V_{DDA} – 0.2
SID288A	V_{OS_TR}	Offset voltage, trimmed	–	±1	–	mV	Medium mode
SID288B	V_{OS_TR}	Offset voltage, trimmed	–	±2	–	mV	Low mode
SID289	$V_{OS\_DR\_UNTR}$	Offset voltage drift, untrimmed	–	–	–	µV/°C	–

Table 8. Opamp Specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID290	$V_{OS\_DR\_TR}$	Offset voltage drift, trimmed	–10	±3	10	µV/°C	High mode, 0.2 to V_{DDA} – 0.2
SID290A	$V_{OS\_DR\_TR}$	Offset voltage drift, trimmed	–	±10	–	µV/°C	Medium mode
SID290B	$V_{OS\_DR\_TR}$	Offset voltage drift, trimmed	–	±10	–	µV/°C	Low mode
SID291	CMRR	DC Common mode rejection ratio	67	80	–	dB	V_{DDD} = 3.3 V
SID292	PSRR	Power supply rejection ratio at 1 kHz, 10-mV ripple	70	85	–	dB	V_{DDD} = 3.3 V
Noise			–	–	–		–
SID293	VN1	Input-referred, 1 Hz–1 GHz, power = Hi	–	100	–	µVrms	–
SID294	VN2	Input-referred, 1 kHz, power = Hi	–	180	–	nV/rtHz	–
SID295	VN3	Input-referred, 10 kHz, power = Hi	–	70	–	nV/rtHz	–
SID296	VN4	Input-referred, 100 kHz, power = Hi	–	38	–	nV/rtHz	–
SID297	CLOAD	Stable up to max. load. Performance specs at 50 pF.	–	–	125	pF	–
SID298	SLEW_RATE	Output slew rate	6	–	–	V/µs	Cload = 50 pF, Power = High, $V_{DDA} \geq 2.7$ V
SID299	T_OP_WAKE	From disable to enable, no external RC dominating	–	25	–	µs	–
	COMP_MODE	Comparator mode; 50-mV overdrive, Trise = Tfall (approx.)	–		–		–
SID300	T_{PD1}	Response time; power = hi	–	150	–	ns	–
SID301	T_{PD2}	Response time; power = med	–	400	–	ns	–
SID302	T_{PD3}	Response time; power = lo	–	2000	–	ns	–
SID303	V_{HYST_OP}	Hysteresis	–	10	–	mV	–
Deep Sleep Mode		Mode 2 is lowest current range. Mode 1 has higher GBW.					Deep Sleep mode operation: $V_{DDA} \geq 2.7$ V. V_{IN} is 0.2 to V_{DDA} – 1.5 V
SID_DS_1	$I_{DD\_HI\_M1}$	Mode 1, High current	–	1300	1500	µA	Typ at 25 °C
SID_DS_2	$I_{DD\_MED\_M1}$	Mode 1, Medium current	–	460	600	µA	Typ at 25 °C
SID_DS_3	$I_{DD\_LOW\_M1}$	Mode 1, Low current	–	230	350	µA	Typ at 25 °C
SID_DS_4	$I_{DD\_HI\_M2}$	Mode 2, High current	–	120	–	µA	25 °C
SID_DS_5	$I_{DD\_MED\_M2}$	Mode 2, Medium current	–	60	–	µA	25 °C
SID_DS_6	$I_{DD\_LOW\_M2}$	Mode 2, Low current	–	15	–	µA	25 °C
SID_DS_7	GBW_HI_M1	Mode 1, High current	–	4	–	MHz	25 °C
SID_DS_8	GBW_MED_M1	Mode 1, Medium current	–	2	–	MHz	25 °C
SID_DS_9	GBW_LOW_M1	Mode 1, Low current	–	0.5	–	MHz	25 °C
SID_DS_10	GBW_HI_M2	Mode 2, High current	–	0.5	–	MHz	20-pF load, no DC load 0.2 V to V_{DDA} – 1.5 V
SID_DS_11	GBW_MED_M2	Mode 2, Medium current	–	0.2	–	MHz	20-pF load, no DC load 0.2 V to V_{DDA} – 1.5 V

Table 8. Opamp Specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID_DS_12	GBW_LOW_M2	Mode 2, Low current	–	0.1	–	MHz	20-pF load, no DC load 0.2 V to V_{DDA} – 1.5 V
SID_DS_13	$V_{OS\_HI\_M1}$	Mode 1, High current	–	5	–	mV	With trim 25 °C, 0.2 V to V_{DDA} – 1.5 V
SID_DS_14	$V_{OS\_MED\_M1}$	Mode 1, Medium current	–	5	–	mV	With trim 25 °C, 0.2 V to V_{DDA} – 1.5 V
SID_DS_15	$V_{OS\_LOW\_M1}$	Mode 1, Low current	–	5	–	mV	With trim 25 °C, 0.2 V to V_{DDA} – 1.5 V
SID_DS_16	$V_{OS\_HI\_M2}$	Mode 2, High current	–	5	–	mV	With trim 25 °C, 0.2 V to V_{DDA} – 1.5 V
SID_DS_17	$V_{OS\_MED\_M2}$	Mode 2, Medium current	–	5	–	mV	With trim 25 °C, 0.2 V to V_{DDA} – 1.5 V
SID_DS_18	$V_{OS\_LOW\_M2}$	Mode 2, Low current	–	5	–	mV	With trim 25 °C, 0.2 V to V_{DDA} – 1.5 V
SID_DS_19	$I_{OUT\_HI\_M1}$	Mode 1, High current	–	10	–	mA	Output is 0.5 V to V_{DDA} – 0.5 V
SID_DS_20	$I_{OUT\_MED\_M1}$	Mode 1, Medium current	–	10	–	mA	Output is 0.5 V to V_{DDA} – 0.5 V
SID_DS_21	$I_{OUT\_LOW\_M1}$	Mode 1, Low current	–	4	–	mA	Output is 0.5 V to V_{DDA} – 0.5 V
SID_DS_22	$I_{OUT\_HI\_M2}$	Mode 2, High current	–	1	–	mA	Output is 0.5 V to V_{DDA} – 0.5 V
SID_DS_23	$I_{OUT\_MED\_M2}$	Mode 2, Medium current	–	1	–	mA	Output is 0.5 V to V_{DDA} – 0.5 V
SID_DS_24	$I_{OUT\_LOW\_M2}$	Mode 2, Low current	–	0.5	–	mA	Output is 0.5 V to V_{DDA} – 0.5 V

Table 9. Low-Power (LP) Comparator Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
LP Comparator DC Specifications							
SID84	$V_{OFFSET1}$	Input offset voltage for COMP1. Normal power mode.	–10	–	10	mV	COMP0 offset is ±25 mV
SID85A	$V_{OFFSET2}$	Input offset voltage. Low-power mode.	–25	±12	25	mV	–
SID85B	$V_{OFFSET3}$	Input offset voltage. Ultra low-power mode.	–25	±12	25	mV	–
SID86	V_{HYST1}	Hysteresis when enabled in Normal mode	–	–	60	mV	–
SID86A	V_{HYST2}	Hysteresis when enabled in Low-power mode	–	–	80	mV	–
SID87	V_{ICM1}	Input common mode voltage in Normal mode	0	–	V_{DDIO1} – 0.1	V	–
SID247	V_{ICM2}	Input common mode voltage in Low power mode	0	–	V_{DDIO1} – 0.1	V	–
SID247A	V_{ICM3}	Input common mode voltage in Ultra low power mode	0	–	V_{DDIO1} – 0.1	V	–

Table 9. Low-Power (LP) Comparator Specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID88	CMRR	Common mode rejection ratio in Normal power mode	50	–	–	dB	–
SID89	I_{CMP1}	Block Current, Normal mode	–	–	150	µA	–
SID248	I_{CMP2}	Block Current, Low power mode	–	–	10	µA	–
SID259	I_{CMP3}	Block Current in Ultra low-power mode	–	0.3	0.85	µA	–
SID90	ZCMP	DC Input impedance of comparator	35	–	–	MΩ	–
LP Comparator AC Specifications							
SID91	T_{RESP1}	Response time, Normal mode, 100 mV overdrive	–	–	100	ns	–
SID258	T_{RESP2}	Response time, Low power mode, 100 mV overdrive	–	–	1000	ns	–
SID92	T_{RESP3}	Response time, Ultra-low power mode, 100 mV overdrive	–	–	20	µs	–
SID92E	T_CMP_EN1	Time from Enabling to operation	–	–	10	µs	Normal and Low-power modes
SID92F	T_CMP_EN2	Time from Enabling to operation	–	–	50	µs	Ultra low-power mode

Table 10. Temperature Sensor Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID93	$T_{SENSACC}$	Temperature sensor accuracy	–5	±1	5	°C	–40 to +85 °C

Table 11. Internal Reference Specification

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID93R	V_{REFBG}	–	1.188	1.2	1.212	V	–

SAR ADC

Table 12. 12-bit SAR ADC DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID94	A_RES	SAR ADC Resolution	–	–	12	bits	–
SID95	A_CHNLS_S	Number of channels - single ended	–	–	16	–	8 full speed.
SID96	A-CHNKS_D	Number of channels - differential	–	–	8	–	Diff inputs use neighboring I/O
SID97	A-MONO	Monotonicity	–	–	–	–	Yes
SID98	A_GAINERR	Gain error	–	–	±0.2	%	With external reference.
SID99	A_OFFSET	Input offset voltage	–	–	2	mV	Measured with 1-V reference
SID100	A_ISAR_1	Current consumption at 1 Msps	–	–	1	mA	At 1 Msps. External Bypass Cap.
SID100A	A_ISAR_2	Current consumption at 1 Msps. Reference = V_{DD}	–	–	1.25	mA	At 1 Msps. External Bypass Cap.
SID101	A_VINS	Input voltage range - single-ended	V_{SS}	–	V_{DDA}	V	–
SID102	A_VIND	Input voltage range - differential	V_{SS}	–	V_{DDA}	V	–

Table 15. CapSense Sigma-Delta (CSD) Specifications *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SID314A	$I_{DAC1CRT2}$	Output current of IDAC1(7 bits) in medium range	33.7		45.6	µA	LSB = 300-nA typ.
SID314B	$I_{DAC1CRT3}$	Output current of IDAC1(7 bits) in high range	270		365	µA	LSB = 2.4-µA typ.
SID314C	$I_{DAC1CRT12}$	Output current of IDAC1 (7 bits) in low range, 2X mode	8		11.4	µA	LSB = 37.5-nA typ. 2X output stage
SID314D	$I_{DAC1CRT22}$	Output current of IDAC1(7 bits) in medium range, 2X mode	67		91	µA	LSB = 300-nA typ. 2X output stage
SID314E	$I_{DAC1CRT32}$	Output current of IDAC1(7 bits) in high range, 2X mode. V_{DDA} > 2 V	540		730	µA	LSB = 2.4-µA typ.2X output stage
SID315	$I_{DAC2CRT1}$	Output current of IDAC2 (7 bits) in low range	4.2		5.7	µA	LSB = 37.5-nA typ.
SID315A	$I_{DAC2CRT2}$	Output current of IDAC2 (7 bits) in medium range	33.7		45.6	µA	LSB = 300-nA typ.
SID315B	$I_{DAC2CRT3}$	Output current of IDAC2 (7 bits) in high range	270		365	µA	LSB = 2.4-µA typ.
SID315C	$I_{DAC2CRT12}$	Output current of IDAC2 (7 bits) in low range, 2X mode	8		11.4	µA	LSB = 37.5-nA typ. 2X output stage
SID315D	$I_{DAC2CRT22}$	Output current of IDAC2(7 bits) in medium range, 2X mode	67		91	µA	LSB = 300-nA typ. 2X output stage
SID315E	$I_{DAC2CRT32}$	Output current of IDAC2(7 bits) in high range, 2X mode. V_{DDA} > 2V	540		730	µA	LSB = 2.4-µA typ.2X output stage
SID315F	$I_{DAC3CRT13}$	Output current of IDAC in 8-bit mode in low range	8		11.4	µA	LSB = 37.5-nA typ.
SID315G	$I_{DAC3CRT23}$	Output current of IDAC in 8-bit mode in medium range	67		91	µA	LSB = 300-nA typ.
SID315H	$I_{DAC3CRT33}$	Output current of IDAC in 8-bit mode in high range. V_{DDA} > 2V	540		730	µA	LSB = 2.4-µA typ.
SID320	$I_{DACOFFSET}$	All zeroes input	–	–	1	LSB	Polarity set by Source or Sink
SID321	$I_{DACGAIN}$	Full-scale error less offset	–	–	±15	%	LSB = 2.4-µA typ.
SID322	$I_{DACMISMATCH1}$	Mismatch between IDAC1 and IDAC2 in Low mode	–	–	9.2	LSB	LSB = 37.5-nA typ.
SID322A	$I_{DACMISMATCH2}$	Mismatch between IDAC1 and IDAC2 in Medium mode	–	–	6	LSB	LSB = 300-nA typ.
SID322B	$I_{DACMISMATCH3}$	Mismatch between IDAC1 and IDAC2 in High mode	–	–	5.8	LSB	LSB = 2.4-µA typ.
SID323	$I_{DACSET8}$	Settling time to 0.5 LSB for 8-bit IDAC	–	–	10	µs	Full-scale transition. No external load.
SID324	$I_{DACSET7}$	Settling time to 0.5 LSB for 7-bit IDAC	–	–	10	µs	Full-scale transition. No external load.
SID325	CMOD	External modulator capacitor.	–	2.2	–	nF	5-V rating, X7R or NP0 cap.

LCD Specifications

Table 19. LCD Direct Drive DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID154	I_{LCDLOW}	Operating current in low-power mode	–	5	–	µA	16 × 4 small segment display at 50 Hz
SID155	C_{LCDCAP}	LCD capacitance per segment/common driver	–	500	5000	pF	–
SID156	LCD_{OFFSET}	Long-term segment offset	–	20	–	mV	–
SID157	I_{LCDOP1}	PWM Mode current. 3.3-V bias. 8-MHz IMO. 25 °C.	–	0.6	–	mA	32 × 4 segments 50 Hz
SID158	I_{LCDOP2}	PWM Mode current. 3.3-V bias. 8-MHz IMO. 25 °C.	–	0.5	–	mA	32 × 4 segments 50 Hz

Table 20. LCD Direct Drive AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID159	F_{LCD}	LCD frame rate	10	50	150	Hz	–

Memory

Table 21. Flash Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
Flash DC Specifications							
SID173	VPE	Erase and program voltage	1.71	–	3.6	V	
Flash AC Specifications							
SID174	$T_{ROWWRITE}$	Row (Block) write time (erase & program)	–	–	16	ms	Row (Block) = 512 bytes
SID175	$T_{ROWERASE}$	Row erase time	–	–	11	ms	
SID176	$T_{ROWPROGRAM}$	Row program time after erase	–	–	5	ms	
SID178	$T_{BULKERASE}$	Bulk erase time (1024 KB)	–	–	11	ms	
SID179	$T_{SECTORERASE}$	Sector erase time (256 KB)	–	–	11	ms	512 rows per sector
SID178S	$T_{SSERIAE}$	Sub-sector erase time	–	–	11	ms	8 rows per sub-sector
SID179S	$T_{SSWRITE}$	Sub-sector write time; 1 erase plus 8 program times	_	_	51	ms	
SID180S	T_{SWRITE}	Sector write time; 1 erase plus 512 program times	_	_	2.6	seconds	
SID180	$T_{DEVPROG}$	Total device program time	–	–	15	seconds	
SID181	F_{END}	Flash Endurance	100 k	–	–	cycles	
SID182	F_{RET1}	Flash Retention. Ta ≤ 25 °C, 100 k P/E cycles	10	_	_	years	
SID182A	F_{RET2}	Flash Retention. Ta ≤ 85 °C, 10 k P/E cycles	10	_	_	years	
SID182B	F_{RET3}	Flash Retention. Ta ≤ 55 °C, 20 k P/E cycles	20	_	_	years	
SID256	T_{WS100}	Number of Wait states at 100 MHz	3	–	–		
SID257	T_{WS50}	Number of Wait states at 50 MHz	2	–	–		

Note
4. It can take as much as 16 milliseconds to write to flash. During this time, the device should not be reset, or flash operations will be interrupted and cannot be relied on to have completed. Reset sources include the XRES pin, software resets, CPU lockup states and privilege violations, improper power supply levels, and watchdogs. Make certain that these are not inadvertently activated.

System Resources

Table 22. PSoC 6 System Resources

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
Power-On-Reset with Brown-out DC Specifications							
Precise POR(PPOR)							
SID190	$V_{FALLPPOR}$	BOD trip voltage in Active and Sleep modes. V_{DDD}.	1.54	–	–	V	BOD Reset guaranteed for levels below 1.54 V
SID192	$V_{FALLDPSLP}$	BOD trip voltage in Deep Sleep. V_{DDD}	1.54	–	–	V	–
SID192A	V_{DDRAMP}	Maximum power supply ramp rate (any supply)	–	–	100	mV/µs	Active Mode
POR with Brown-out AC Specification							
SID194A	V_{DDRAMP_DS}	Maximum power supply ramp rate (any supply) in Deep Sleep	–	–	10	mV/µs	BOD operation guaranteed
Voltage Monitors DC Specifications							
SID195R	V_{HVD0}		1.18	1.23	1.27	V	–
SID195	V_{HVDI1}		1.38	1.43	1.47	V	–
SID196	V_{HVDI2}		1.57	1.63	1.68	V	–
SID197	V_{HVDI3}		1.76	1.83	1.89	V	–
SID198	V_{HVDI4}		1.95	2.03	2.1	V	–
SID199	V_{HVDI5}		2.05	2.13	2.2	V	–
SID200	V_{HVDI6}		2.15	2.23	2.3	V	–
SID201	V_{HVDI7}		2.24	2.33	2.41	V	–
SID202	V_{HVDI8}		2.34	2.43	2.51	V	–
SID203	V_{HVDI9}		2.44	2.53	2.61	V	–
SID204	V_{HVDI10}		2.53	2.63	2.72	V	–
SID205	V_{HVDI11}		2.63	2.73	2.82	V	–
SID206	V_{HVDI12}		2.73	2.83	2.92	V	–
SID207	V_{HVDI13}		2.82	2.93	3.03	V	–
SID208	V_{HVDI14}		2.92	3.03	3.13	V	–
SID209	V_{HVDI15}		3.02	3.13	3.23	V	–
SID211	LVI_IDD	Block current	–	5	15	µA	–
Voltage Monitors AC Specification							
SID212	$T_{MONTRIP}$	Voltage monitor trip time	–	–	170	ns	–

SWD Interface

Table 23. SWD and Trace Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SWD and Trace Interface							
SID214	F_SWDCLK2	1.7 V ≤ V_{DDD} ≤ 3.6 V	–	–	25	MHz	LP Mode; V_{CCD} = 1.1 V
SID214L	F_SWDCLK2L	1.7 V ≤ V_{DDD} ≤ 3.6 V	–	–	12	MHz	ULP Mode. V_{CCD} = 0.9 V.
SID215	T_SWDI_SETUP	T = 1/f SWDCLK	0.25 * T	–	–	ns	
SID216	T_SWDI_HOLD	T = 1/f SWDCLK	0.25 * T	–	–	ns	
SID217	T_SWDO_VALID	T = 1/f SWDCLK	–	–	0.5 * T	ns	
SID217A	T_SWDO_HOLD	T = 1/f SWDCLK	1	–	–	ns	
SID214T	F_TRCLK_LP1	With Trace Data setup/hold times of 2/1 ns respectively	–	–	75	MHz	LP Mode. V_{DD} = 1.1 V
SID215T	F_TRCLK_LP2	With Trace Data setup/hold times of 3/2 ns respectively	–	–	70	MHz	LP Mode. V_{DD} = 1.1 V
SID216T	F_TRCLK_ULP	With Trace Data setup/hold times of 3/2 ns respectively	–	–	25	MHz	ULP Mode. V_{DD} = 0.9 V

Internal Main Oscillator

Table 24. IMO DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID218	I_{IMO1}	IMO operating current at 8 MHz	–	9	15	µA	–

Table 25. IMO AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID223	$F_{IMOTOL1}$	Frequency variation centered on 8 MHz	–	–	±2	%	–
SID227	T_{JITR}	Cycle-to-Cycle and Period jitter	–	±250	–	ps	–

Internal Low-Speed Oscillator

Table 26. ILO DC Specification

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID231	I_{ILO2}	ILO operating current at 32 kHz	–	0.3	0.7	µA	–

Table 27. ILO AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID234	$T_{STARTILO1}$	ILO startup time	–	–	7	µs	Startup time to 95% of final frequency
SID236	$T_{LIODUTY}$	ILO Duty cycle	45	50	55	%	–
SID237	$F_{ILOTRIM1}$	32-kHz trimmed frequency	28.8	32	35.2	kHz	±10% variation

Ordering Information

Table 41 lists the PSoC 63 part numbers and features. The following table shows Marketing Part Numbers (MPNs) for products including the BLE Radio. The packages are 104 M CSP and 116 BGA.

Table 41. BLE Series Part Numbers

Family	MPN	CPU Speed (M4)	CPU Speed (M0+)	Single core/Dual core	ULP/LP	Flash	SRAM	No. of CTBMs	No. of UDBs	CapSense	GPIOs	CRYPTO	Package
63	CY8C6336BZI-BLF03	150	–	Single	LP	512	128	0	0	No	78	No	116-BGA
	CY8C6316BZI-BLF03	50	–	Single	ULP	512	128	0	0	No	78	No	116-BGA
	CY8C6316BZI-BLF53	50	–	Single	ULP	512	128	1	12	Yes	78	Yes	116-BGA
	CY8C6337BZI-BLF13	150	–	Single	LP	1024	288	0	0	Yes	78	No	116-BGA
	CY8C6336BZI-BLD13	150	100	Double	LP	512	128	0	0	Yes	78	No	116-BGA
	CY8C6347BZI-BLD43	150/50	100/25	Double	FLEX	1024	288	0	0	Yes	78	Yes	116-BGA
	CY8C6347BZI-BLD33	150/50	100/25	Double	FLEX	1024	288	1	12	Yes	78	No	116-BGA
	CY8C6347BZI-BLD53	150/50	100/25	Double	FLEX	1024	288	1	12	Yes	78	Yes	116-BGA
	CY8C6347FMI-BLD13	150/50	100/25	Double	FLEX	1024	288	0	0	Yes	70	No	104-MCSP
	CY8C6347FMI-BLD43	150/50	100/25	Double	FLEX	1024	288	0	0	Yes	70	Yes	104-MCSP
	CY8C6347FMI-BLD33	150/50	100/25	Double	FLEX	1024	288	1	12	Yes	70	No	104-MCSP
	CY8C6347FMI-BLD53	150/50	100/25	Double	FLEX	1024	288	1	12	Yes	70	Yes	104-MCSP

Table 42 lists the field values.

Table 42. MPN Nomenclature

Field	Description	Values	Meaning
CY8C	Cypress Prefix		
6	Architecture	6	PSoC 6
A	Family	0	Value
		1	Programmable
		2	Performance
		3	Connectivity
B	Speed	1	50 MHz
		2	100 MHz
		3	150 MHz
		4	150/50 MHz
C	Flash Capacity	4	128 KB
		5	256 KB
		6	512 KB
		7	1024 KB

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