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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4/M0
Core Size	32-Bit Dual-Core
Speed	100MHz, 150MHz
Connectivity	I²C, LINbus, QSPI, SPI, UART/USART, USB
Peripherals	Bluetooth, Brown-out Detect/Reset, Cap Sense, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	78
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	32K x 8
RAM Size	288K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 8x12b SAR; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	116-WFBGA
Supplier Device Package	116-BGA (5.2x6.4)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c6347bzi-bld43

Blocks and Functionality

The PSoC 63 block diagram is shown in Figure 2. There are five major subsystems: CPU subsystem, BLE subsystem, system resources, peripheral blocks, and I/O subsystem.

Figure 2. Block Diagram

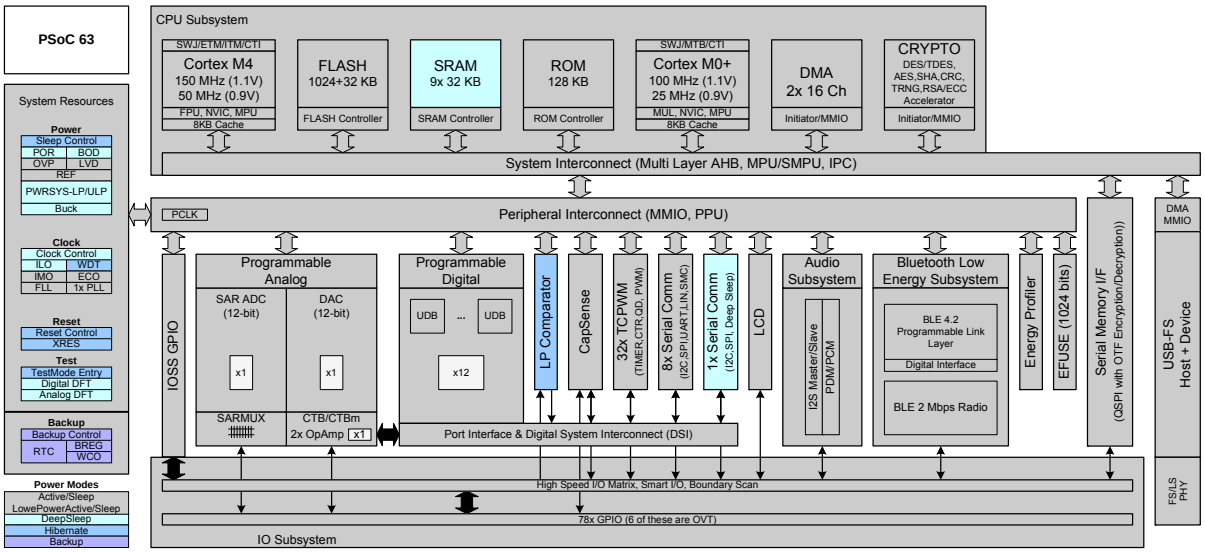


Figure 2 shows the subsystems of the chip and gives a very simplified view of their inter-connections (Multi-layer AHB is used in practice). The color-coding shows the lowest power mode where the particular block is still functional (for example, LP Comparator is functional in Deep Sleep mode).

PSoC 63 devices include extensive support for programming, testing, debugging, and tracing both hardware and firmware.

Complete debug-on-chip functionality enables full device debugging in the final system using the standard production device. It does not require special interfaces, debugging pods, simulators, or emulators. Only the standard programming connections are required to fully support debug.

The PSoC Creator Integrated Development Environment (IDE) provides fully integrated programming and debug support for PSoC 63 devices. The SWJ (SWD and JTAG) interface is fully compatible with industry-standard third party probes. With the ability to disable debug features, with very robust flash protection, and by allowing customer-proprietary functionality to be implemented in on-chip programmable blocks, the PSoC 63 family provides a very high level of security.

The debug circuits are enabled by default and can only be disabled in firmware. If not enabled, the only way to re-enable them is to erase the entire device, clear flash protection, and reprogram the device with new firmware that enables debugging.

Additionally, all device interfaces can be permanently disabled (device security) for applications concerned about phishing attacks due to a maliciously reprogrammed device or attempts to defeat security by starting and interrupting flash programming sequences. All programming, debug, and test interfaces are disabled when maximum device security is enabled. The security level is a trade-off the customer can make.

The SAR is able to digitize the output of the on-chip temperature sensor for calibration and other temperature-dependent functions. The SAR is not available in Deep Sleep and Hibernate modes as it requires a high-speed clock (up to 18 MHz). The SAR operating range is 1.71 V to 3.6 V.

Temperature Sensor

PSoC 63 has an on-chip temperature sensor. This consists of a diode, which is biased by a current source that can be disabled to save power. The temperature sensor is connected to the ADC, which digitizes the reading and produces a temperature value by using a Cypress-supplied software that includes calibration and linearization.

12-bit Digital-Analog Converter

There is a 12-bit voltage mode DAC on the chip, which can settle in less than 5 µs. The DAC may be driven by the DMA controllers to generate user-defined waveforms. The DAC output from the chip can either be the resistive ladder output (highly linear near ground) or a buffered output.

Continuous Time Block (CTBm) with Two Opamps

This block consists of two opamps, which have their inputs and outputs connected to fixed pins and have three power modes and a comparator mode. The outputs of these opamps can be used as buffers for the SAR inputs. The non-inverting inputs of these opamps can be connected to either of two pins, thus allowing independent sensors to be used at different times. The pin selection can be made via firmware. The opamps can be set to one of the four power levels; the lowest level allowing operation in Deep Sleep mode in order to preserve lower performance Continuous-Time functionality in Deep Sleep mode. The DAC output can be buffered through an opamp.

Low-Power Comparators

PSoC 63 has a pair of low-power comparators, which can also operate in Deep Sleep and Hibernate modes. This allows the analog system blocks to be disabled while retaining the ability to monitor external voltage levels during Deep Sleep and Hibernate modes. The comparator outputs are normally synchronized to avoid metastability unless operating in an asynchronous power mode (Hibernate) where the system wake-up circuit is activated by a comparator-switch event.

Programmable Digital

Smart I/O

There are two Smart I/O blocks, which allow Boolean operations on signals going to the GPIO pins from the subsystems of the chip or on signals coming into the chip. Operation can be synchronous or asynchronous and the blocks operate in low-power modes, such as Deep Sleep and Hibernate.This allows, for example, detection of logic conditions that can indicate that the CPU should wake up instead of waking up on general I/O interrupts, which consume more power and can generate spurious wake-ups.

Universal Digital Blocks (UDBs) and Port Interfaces

PSoC 63 has 12 UDBs; the UDB array also provides a switched Digital System Interconnect (DSI) fabric that allows signals from peripherals and ports to be routed to and through the UDBs for communication and control.

Fixed-Function Digital

Timer/Counter/PWM Block

The timer/counter/PWM block consists of 32 counters with user-programmable period length. There is a Capture register to record the count value at the time of an event (which may be an I/O event), a period register which is used to either stop or auto-reload the counter when its count is equal to the period register, and compare registers to generate compare value signals which are used as PWM duty cycle outputs. The block also provides true and complementary outputs with programmable offset between them to allow the use as deadband programmable complementary PWM outputs. It also has a Kill input to force outputs to a predetermined state; for example, this is used in motor-drive systems when an overcurrent state is indicated and the PWMs driving the FETs need to be shut off immediately with no time for software intervention. There are eight 32-bit counters and 24 16-bit counters.

Serial Communication Blocks (SCB)

PSoC 63 has nine SCBs, which can each implement an I^2C, UART, or SPI interface. One SCB will operate in Deep Sleep with an external clock, this SCB will only operate in Slave mode (requires external clock).

I^2C Mode: The hardware I^2C block implements a full multi-master and slave interface (it is capable of multimaster arbitration). This block is capable of operating at speeds of up to 1 Mbps (Fast Mode Plus) and has flexible buffering options to reduce the interrupt overhead and latency for the CPU. It also supports EzI^2C that creates a mailbox address range in the memory of PSoC 63 and effectively reduces the I^2C communication to reading from and writing to an array in the memory. In addition, the block supports a 256 byte FIFO for receive and transmit, which, by increasing the time given for the CPU to read the data, greatly reduces the need for clock stretching caused by the CPU not having read the data on time. The FIFO mode is available in all channels and is very useful in the absence of DMA.

The I^2C peripheral is compatible with I^2C Standard-mode, Fast-mode, and Fast-Mode Plus devices as defined in the NXP I^2C-bus specification and user manual (UM10204). The I^2C bus I/O is implemented with GPIO in open-drain modes.

UART Mode: This is a full-feature UART operating at up to 8 Mbps. It supports automotive single-wire interface (LIN), infrared interface (IrDA), and SmartCard (ISO7816) protocols, all of which are minor variants of the basic UART protocol. In addition, it supports the 9-bit multiprocessor mode that allows the addressing of peripherals connected over common RX and TX lines. Common UART functions such as parity error, break detect, and frame error are supported. A 256 byte FIFO allows much greater CPU service latencies to be tolerated.

SPI Mode: The SPI mode supports full Motorola SPI, TI Secure Simple Pairing (SSP) (essentially adds a start pulse that is used to synchronize SPI Codecs), and National Microwire (half-duplex form of SPI). The SPI block can use the FIFO and supports an EzSPI mode in which the data interchange is reduced to reading and writing an array in memory. The SPI interface operates with up to a 25-MHz SPI clock.

Table 1. Pinouts for 116-BGA and 104-MCSP Packages *(continued)*

104-MCSP-BLE		116-BGA-BLE	
Pin	Name	Pin	Name
N1	P7.0	J10	P7.0
G6	P7.1	H10	P7.1
H4	P7.2	H8	P7.2
G5	P7.3	H7	P7.3
H3	P7.4	H6	P7.4
H2	P7.5	G9	P7.5
G3	P7.6	G8	P7.6
G2	P7.7	G7	P7.7
D1	VDDIO1	G10	VDDIO1
G4	P8.0	F10	P8.0
G1	P8.1	F9	P8.1
F3	P8.2	F8	P8.2
F2	P8.3	F7	P8.3
F1	P8.4	G6	P8.4
E3	P8.5	E9	P8.5
E1	P8.6	E8	P8.6
E2	P8.7	E7	P8.7
A1	VDDA	A9	VDDA
D2	P9.0	D10	P9.0
C1	P9.1	D9	P9.1
D3	P9.2	D8	P9.2
B1	P9.3	D7	P9.3
		C10	P9.4
		C9	P9.5
		C8	P9.6
		C7	P9.7
C4	P11.0	F5	P11.0
C5	P11.1	E5	P11.1
D6	P11.2	D5	P11.2
		B10	VREF
A1	VDDA	A9	VDDA
A1	VDDA	A9	VDDA
C2	P10.0	B8	P10.0
B4	P11.3	C6	P11.3
A4	P11.4	B6	P11.4
B5	P11.5	A6	P11.5
A5	P11.6	B5	P11.6
A6	P11.7	A5	P11.7
B6	VDDIO0	B3	VDDIO0
D7, D4, F4, G7	VSS	B2, B9, H2, H9, D1	VSS
B7	P12.0	A4	P12.0
A7	P12.1	B4	P12.1
B8	P12.2	C4	P12.2
A8	P12.3	A3	P12.3
C8	P12.4	C5	P12.4
		D4	P12.5
		G5	P12.6
		H5	P12.7
A9	P13.0	H4	P13.0
B9	P13.1	G4	P13.1
		F4	P13.6
		C3	P13.7

Note: Balls H5 and J9 are No-Connects (NC) in the 104-MCSP package.

The correspondence of power supplies to ports by package type is as follows:

- P0: VBACKUP
- P1: VDDD. Port 1 Pins are Over-Voltage Tolerant (OVT).
- P5, P6, P7, P8: VDDIO1
- P9, P10: VDDA
- P11, P12, P13: VDDIO0

Each Port Pin has multiple alternate functions. These are defined in Table 2.

Table 2. Multiple Alternate Functions

Port/ Pin	ACT #0	ACT #1	DS #2	ACT #4	ACT #5	ACT #6	ACT #7	ACT #8	ACT #9	ACT #10	ACT #12	ACT #13	ACT #14	ACT #15	DS #4	DS #5	DS #6
P0.0	tcpwm[0].line[0]:0	tcpwm[1].line[0]:0		srss.ext_clk:0				scb[0].spi_select1:0			peri.tr_io_input[0]:0						
P0.1	tcpwm[0].line_compl[0]:0	tcpwm[1].line_compl[0]:0						scb[0].spi_select2:0			peri.tr_io_input[1]:0					cpuss.swj_trstn	
P0.2	tcpwm[0].line[1]:0	tcpwm[1].line[1]:0				scb[0].uart_rx:0	scb[0].i2c_scl:0	scb[0].spi_mosi:0									
P0.3	tcpwm[0].line_compl[1]:0	tcpwm[1].line_compl[1]:0				scb[0].uart_tx:0	scb[0].i2c_sda:0	scb[0].spi_miso:0									
P0.4	tcpwm[0].line[2]:0	tcpwm[1].line[2]:0				scb[0].uart_rts:0		scb[0].spi_clk:0				peri.tr_io_output[0]:2					
P0.5	tcpwm[0].line_compl[2]:0	tcpwm[1].line_compl[2]:0		srss.ext_clk:1		scb[0].uart_cts:0		scb[0].spi_select0:0				peri.tr_io_output[1]:2					
P1.0	tcpwm[0].line[3]:0	tcpwm[1].line[3]:0				scb[7].uart_rx:0	scb[7].i2c_scl:0	scb[7].spi_mosi:0			peri.tr_io_input[2]:0						
P1.1	tcpwm[0].line_compl[3]:0	tcpwm[1].line_compl[3]:0				scb[7].uart_tx:0	scb[7].i2c_sda:0	scb[7].spi_miso:0			peri.tr_io_input[3]:0						
P1.2	tcpwm[0].line[4]:4	tcpwm[1].line[12]:1				scb[7].uart_rts:0		scb[7].spi_clk:0									
P1.3	tcpwm[0].line_compl[4]:4	tcpwm[1].line_compl[12]:1				scb[7].uart_cts:0		scb[7].spi_select0:0									
P1.4	tcpwm[0].line[5]:4	tcpwm[1].line[13]:1						scb[7].spi_select1:0									
P1.5	tcpwm[0].line_compl[5]:4	tcpwm[1].line_compl[14]:1						scb[7].spi_select2:0									
P5.0	tcpwm[0].line[4]:0	tcpwm[1].line[4]:0				scb[5].uart_rx:0	scb[5].i2c_scl:0	scb[5].spi_mosi:0		audioss.clk_i2s_if	peri.tr_io_input[10]:0						
P5.1	tcpwm[0].line_compl[4]:0	tcpwm[1].line_compl[4]:0				scb[5].uart_tx:0	scb[5].i2c_sda:0	scb[5].spi_miso:0		audioss.tx_sck	peri.tr_io_input[11]:0						
P5.2	tcpwm[0].line[5]:0	tcpwm[1].line[5]:0				scb[5].uart_rts:0		scb[5].spi_clk:0		audioss.tx_ws							
P5.3	tcpwm[0].line_compl[5]:0	tcpwm[1].line_compl[5]:0				scb[5].uart_cts:0		scb[5].spi_select0:0		audioss.tx_sdo							
P5.4	tcpwm[0].line[6]:0	tcpwm[1].line[6]:0						scb[5].spi_select1:0		audioss.rx_sck							
P5.5	tcpwm[0].line_compl[6]:0	tcpwm[1].line_compl[6]:0						scb[5].spi_select2:0		audioss.rx_ws							

Table 2. Multiple Alternate Functions *(continued)*

Port/ Pin	ACT #0	ACT #1	DS #2	ACT #4	ACT #5	ACT #6	ACT #7	ACT #8	ACT #9	ACT #10	ACT #12	ACT #13	ACT #14	ACT #15	DS #4	DS #5	DS #6
P5.6	tcpwm[0].line[7]:0	tcpwm[1].line[7]:0						scb[5].spi_select3:0		audioss.rx_sdi							
P5.7	tcpwm[0].line_compl[7]:0	tcpwm[1].line_compl[7]:0						scb[3].spi_select3:0									
P6.0	tcpwm[0].line[0]:1	tcpwm[1].line[8]:0	scb[8].i2c_scl:0			scb[3].uart_rx:0	scb[3].i2c_scl:0	scb[3].spi_mosi:0				cpuss.fault_out[0]					scb[8].spi_mosi:0
P6.1	tcpwm[0].line_compl[0]:1	tcpwm[1].line_compl[8]:0	scb[8].i2c_sda:0			scb[3].uart_tx:0	scb[3].i2c_sda:0	scb[3].spi_miso:0				cpuss.fault_out[1]					scb[8].spi_miso:0
P6.2	tcpwm[0].line[1]:1	tcpwm[1].line[9]:0				scb[3].uart_rts:0		scb[3].spi_clk:0									scb[8].spi_clk:0
P6.3	tcpwm[0].line_compl[1]:1	tcpwm[1].line_compl[9]:0				scb[3].uart_cts:0		scb[3].spi_select0:0									scb[8].spi_select0:0
P6.4	tcpwm[0].line[2]:1	tcpwm[1].line[10]:0	scb[8].i2c_scl:1			scb[6].uart_rx:2	scb[6].i2c_scl:2	scb[6].spi_mosi:2			peri.tr_io_input[12]:0	peri.tr_io_output[0]:1				cpuss.swj_swo_tdo	scb[8].spi_mosi:1
P6.5	tcpwm[0].line_compl[2]:1	tcpwm[1].line_compl[10]:0	scb[8].i2c_sda:1			scb[6].uart_tx:2	scb[6].i2c_sda:2	scb[6].spi_miso:2			peri.tr_io_input[13]:0	peri.tr_io_output[1]:1				cpuss.swj_swdoe_tdi	scb[8].spi_miso:1
P6.6	tcpwm[0].line[3]:1	tcpwm[1].line[11]:0				scb[6].uart_rts:2		scb[6].spi_clk:2								cpuss.swj_swdio_tms	scb[8].spi_clk:1
P6.7	tcpwm[0].line_compl[3]:1	tcpwm[1].line_compl[11]:0				scb[6].uart_cts:2		scb[6].spi_select0:2								cpuss.swj_swclk_tclk	scb[8].spi_select0:1
P7.0	tcpwm[0].line[4]:1	tcpwm[1].line[12]:0				scb[4].uart_rx:1	scb[4].i2c_scl:1	scb[4].spi_mosi:1			peri.tr_io_input[14]:0		cpuss.trace_clock				
P7.1	tcpwm[0].line_compl[4]:1	tcpwm[1].line_compl[12]:0				scb[4].uart_tx:1	scb[4].i2c_sda:1	scb[4].spi_miso:1			peri.tr_io_input[15]:0						
P7.2	tcpwm[0].line[5]:1	tcpwm[1].line[13]:0				scb[4].uart_rts:1		scb[4].spi_clk:1									
P7.3	tcpwm[0].line_compl[5]:1	tcpwm[1].line_compl[13]:0				scb[4].uart_cts:1		scb[4].spi_select0:1									
P7.4	tcpwm[0].line[6]:1	tcpwm[1].line[14]:0						scb[4].spi_select1:1					bless.ext_lna_rx_ctl_out	cpuss.trace_data[3]:2			
P7.5	tcpwm[0].line_compl[6]:1	tcpwm[1].line_compl[14]:0						scb[4].spi_select2:1					bless.ext_pa_tx_ctl_out	cpuss.trace_data[2]:2			
P7.6	tcpwm[0].line[7]:1	tcpwm[1].line[15]:0						scb[4].spi_select3:1					bless.ext_pa_lna_chip_en_out	cpuss.trace_data[1]:2			
P7.7	tcpwm[0].line_compl[7]:1	tcpwm[1].line_compl[15]:0						scb[3].spi_select1:0	cpuss.clk_fm_pump					cpuss.trace_data[0]:2			

Analog, Smart I/O, and DSI alternate Port Pin functionality is provided in Table 3.

Table 3. Port Pin Analog, Smart I/O, and DSI Functions

Port/Pin	Name	Analog	Digital HV	DSI	SMARTIO
P0.0	P0.0	wco_in		dsi[0].port_if[0]	
P0.1	P0.1	wco_out		dsi[0].port_if[1]	
P0.2	P0.2			dsi[0].port_if[2]	
P0.3	P0.3			dsi[0].port_if[3]	
P0.4	P0.4		pmic_wakeup_in hibernate_wakeup[1]	dsi[0].port_if[4]	
P0.5	P0.5		pmic_wakeup_out	dsi[0].port_if[5]	
P1.0	P1.0			dsi[1].port_if[0]	
P1.1	P1.1			dsi[1].port_if[1]	
P1.2	P1.2			dsi[1].port_if[2]	
P1.3	P1.3			dsi[1].port_if[3]	
P1.4	P1.4		hibernate_wakeup[0]	dsi[1].port_if[4]	
P1.5	P1.5			dsi[1].port_if[5]	
P2.0	P2.0			dsi[2].port_if[0]	
P2.1	P2.1			dsi[2].port_if[1]	
P2.2	P2.2			dsi[2].port_if[2]	
P2.3	P2.3			dsi[2].port_if[3]	
P2.4	P2.4			dsi[2].port_if[4]	
P2.5	P2.5			dsi[2].port_if[5]	
P2.6	P2.6			dsi[2].port_if[6]	
P2.7	P2.7			dsi[2].port_if[7]	
P3.0	P3.0				
P3.1	P3.1				
P3.2	P3.2				
P3.3	P3.3				
P3.4	P3.4				
P3.5	P3.5				
P4.0	P4.0			dsi[0].port_if[6]	
P4.1	P4.1			dsi[0].port_if[7]	
P4.2	P4.2			dsi[1].port_if[6]	
P4.3	P4.3			dsi[1].port_if[7]	
P5.0	P5.0			dsi[3].port_if[0]	
P5.1	P5.1			dsi[3].port_if[1]	
P5.2	P5.2			dsi[3].port_if[2]	
P5.3	P5.3			dsi[3].port_if[3]	
P5.4	P5.4			dsi[3].port_if[4]	
P5.5	P5.5			dsi[3].port_if[5]	
P5.6	P5.6	lpcomp.inp_comp0		dsi[3].port_if[6]	
P5.7	P5.7	lpcomp.inn_comp0		dsi[3].port_if[7]	
P6.0	P6.0			dsi[4].port_if[0]	
P6.1	P6.1			dsi[4].port_if[1]	
P6.2	P6.2	lpcomp.inp_comp1		dsi[4].port_if[2]	

Figure 3 shows the power supply pins to the PSoC and the connections between the PSoC and the radio. It also shows which pins need bypass capacitors.

Description of power pins is as follows:

1. VBACKUP is the supply to the backup domain. The backup domain includes the 32-kHz WCO, RTC, and backup registers. It can generate a wake-up interrupt to the chip via the RTC timers or an external input. It can also generate an output to wakeup external circuitry. It is connected to VDDD when not used as a separate battery backup domain. VBACKUP provides the supply for Port 0.
2. VDDD is the main digital supply input (1.7 to 3.6 V). It provides the inputs for the internal Regulators and for Port 1.
3. VDDA is the supply for analog peripherals (1.7 to 3.6 V). It must be connected to VDDIOA on the PCB.
4. VDDIOA is the supply to for Ports 9 and 10. It must be connected to VDDA on the PCB when present. Ports 9 and 10 are supplied by VDDA when VDDIOA is not present.
5. VDD_NS is the supply input to the Buck and should be at the same potential as VDDD. The bypass capacitor between VDD_NS and ground should be 10 µF.
6. VDDIO0 is the Supply for Ports 11 to 13 when present. When not present, these ports are supplied by VDDD.
7. VDDIO1 is the Supply for Ports 5 to 8 when present. When not present, these ports are supplied by VDDA.
8. VDDIOR is the Supply for Ports 2 to 4 on the 124 BGA only.

All the pins above may be shorted to VDDD as shown in Figure 3.

9. VRF is the output of the SIMO buck going to the Radio and should be connected to VDCDC and decoupled.
10. VDCDC is the digital supply input to the Radio and should be connected to VRF.
11. The VDDR1, VDDR2, and VDDR3 pins are for the radio sub-systems and need to be decoupled individually and connected to VDCDC through a bead for filtering high frequency power supply noise.
12. VDDR_HVL is the regulated output to the Radio from the PSoC 63 subsystem and needs to be decoupled.
13. DVDD is a Digital LDO output from the Radio and needs to be decoupled.
14. VBUCK1 is the SIMO buck output to the internal core logic and is to be connected to VCCD.
15. VCCD is the internal core logic and needs to be connected to VBUCK1 and decoupled.

The supply voltage range is 1.71 to 3.6 V with all functions and circuits operating over that range. All grounds must be shorted together on the PCB. Bypass capacitors must be used from VDDD and VDDA to ground and wherever indicated in the diagram. Typical practice for systems in this frequency range is to use a capacitor in the 10-µF range in parallel with a smaller capacitor (0.1 µF, for example). Note that these are simply rules of thumb and that, for critical applications, the PCB layout, lead inductance, and the bypass capacitor parasitic should be simulated to design and obtain optimal bypassing. Recommended Buck output capacitor values are 10 µF for Vrf and 4.7 µF for VBUCK1. The capacitor connected to Vind2 should be 100 nF. All capacitors should be ±20% or better; the recommended inductor value is 2.2 µH ±20% (for example, TDK MLP2012H2R2MT0S1).

Development Support

The PSoC 63 family has a rich set of documentation, development tools, and online resources to assist you during your development process. Visit http://www.cypress.com/products/32-bit-arm-cortex-m4-psoc-6 to find out more.

Documentation

A suite of documentation supports the PSoC 63 family to ensure that you can find answers to your questions quickly. This section contains a list of some of the key documents.

Software User Guide: A step-by-step guide for using PSoC Creator. The software user guide shows you how the PSoC Creator build process works in detail, how to use source control with PSoC Creator, and much more.

Component Datasheets: The flexibility of PSoC allows the creation of new peripherals (Components) long after the device has gone into production. Component datasheets provide all of the information needed to select and use a particular Component, including a functional description, API documentation, example code, and AC/DC specifications.

Technical Reference Manual: The Technical Reference Manual (TRM) contains all the technical detail you need to use a PSoC device, including a complete description of all PSoC registers. The TRM is available in the Documentation section at http://www.cypress.com/products/32-bit-arm-cortex-m4-psoc-6.

Online

In addition to print documentation, the Cypress PSoC forums connect you with fellow PSoC users and experts in PSoC from around the world, 24 hours a day, 7 days a week.

Tools

With industry standard cores, programming, and debugging interfaces, the PSoC 63 family is part of a development tool ecosystem. Visit us at www.cypress.com/products/psoc-creator-integrated-design-environment-ide for the latest information on the revolutionary, easy to use PSoC Creator IDE, supported third party compilers, programmers, debuggers, and development kits.

Table 5. Power Supply Range, CPU Current, and Transition Time Specifications *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SIDDS1_B	I_{DD33A_B}	With internal Buck enabled and 64 KB SRAM retention	–	7	–	µA	Max value is at 60 °C
SIDDS2	I_{DD33B}	With internal Buck enabled and 256 KB SRAM retention	–	9	–	µA	Max value is at 85 °C
SIDDS2_B	I_{DD33B_B}	With internal Buck enabled and 256 KB SRAM retention	–	9	–	µA	Max value is at 60 °C
Hibernate Mode							
SIDHIB1	I_{DD34}	V_{DDD} = 1.8 V	–	300	–	nA	No clocks running
SIDHIB2	I_{DD34A}	V_{DDD} = 3.3 V	–	800	–	nA	No clocks running
Power Mode Transition Times							
SID12	T_{LPACT_ACT}	Low Power Active to Active transition time	–	–	35	µs	Including PLL lock time
SID13[2]	T_{DS_LPACT}	Deep Sleep to LP Active transition time	–	–	25	µs	Guaranteed by design
SID13A[3]	T_{DS_ACT}	Deep Sleep to Active transition time	–	–	25	µs	Guaranteed by design
SID14	T_{HIB_ACT}	Hibernate to Active transition time	–	500	–	µs	Including PLL lock time

XRES

Table 6. XRES

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
XRES (Active Low) Specifications							
XRES AC Specifications							
SID15	T_{XRES_ACT}	POR or XRES release to Active transition time	–	750	–	µs	Normal mode, 50 MHz M0+.
SID16	T_{XRES_PW}	XRES Pulse width	5	–	–	µs	
XRES DC Specifications							
SID17	T_{XRES_IDD}	IDD when XRES asserted	–	300	–	nA	V_{DDD} = 1.8 V
SID17A	$T_{XRES\_IDD\_1}$	IDD when XRES asserted	–	800	–	nA	V_{DDD} = 3.3 V
SID77	V_{IH}	Input Voltage high threshold	0.7 * V_{DD}	–	–	V	CMOS Input
SID78	V_{IL}	Input Voltage low threshold	–	–	0.3 * V_{DD}	V	CMOS Input
SID80	C_{IN}	Input Capacitance	–	3	–	pF	
SID81	$V_{HYSXRES}$	Input voltage hysteresis	–	100	–	mV	
SID82	I_{DIODE}	Current through protection diode to V_{DD}/V_{SS}	–	–	100	µA	

Notes
2. Cypress-supplied software wakeup routines take approximately 100 CPU clock cycles after hardware wakeup (the 25 µs) before transition to Application code. With an 8-MHz CPU clock (LP Active), the time before user code executes is 25 + 12.5 = 37.5 µs.
3. Cypress-supplied software wakeup routines take approximately 100 CPU clock cycles after hardware wakeup (the 25 µs) before transition to Application code. With a 25-MHz CPU clock (FLL), the time before user code executes is 25 + 4 = 29 µs. With a 100-MHz CPU clock, the time is 25 + 1 = 26 µs.

GPIO

Table 7. GPIO Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
GPIO DC Specifications							
SID57	V_{IH}	Input voltage high threshold	0.7 * V_{DD}	–	–	V	CMOS Input
SID57A	I_{IHS}	Input current when Pad > VDDIO for OVT inputs	–	–	10	µA	Per I^2C Spec
SID58	V_{IL}	Input voltage low threshold	–	–	0.3 * V_{DD}	V	CMOS Input
SID241	V_{IH}	LVTTL input, V_{DD} < 2.7 V	0.7 * V_{DD}	–	–	V	
SID242	V_{IL}	LVTTL input, V_{DD} < 2.7 V	–	–	0.3*V_{DD}	V	
SID243	V_{IH}	LVTTL input, V_{DD} ≥ 2.7 V	2.0	–	–	V	
SID244	V_{IL}	LVTTL input, V_{DD} ≥ 2.7 V	–	–	0.8	V	
SID59	V_{OH}	Output voltage high level	V_{DD} – 0.5	–	–	V	I_{OH} = 8 mA
SID62A	V_{OL}	Output voltage low level	–	–	0.4	V	I_{OL} = 8 mA
SID63	R_{PULLUP}	Pull-up resistor	3.5	5.6	8.5	kΩ	
SID64	$R_{PULLDOWN}$	Pull-down resistor	3.5	5.6	8.5	kΩ	
SID65	I_{IL}	Input leakage current (absolute value)	–	–	2	nA	25 °C, V_{DD} = 3.0 V
SID65A	I_{IL_CTBM}	Input leakage on CTBm input pins	–	–	4	nA	
SID66	C_{IN}	Input Capacitance	–	–	5	pF	
SID67	V_{HYSTTL}	Input hysteresis LVTTL V_{DD} > 2.7 V	100	0	–	mV	
SID68	$V_{HYSCMOS}$	Input hysteresis CMOS	0.05 * V_{DD}	–	–	mV	
SID69	I_{DIODE}	Current through protection diode to V_{DD}/V_{SS}	–	–	100	µA	
SID69A	I_{TOT_GPIO}	Maximum Total Source or Sink Chip Current	–	–	200	mA	
GPIO AC Specifications							
SID70	T_{RISEF}	Rise time in Fast Strong Mode. 10% to 90% of V_{DD}	–	–	2.5	ns	Cload = 15 pF, 8 mA drive strength
SID71	T_{FALLF}	Fall time in Fast Strong Mode. 10% to 90% of V_{DD}	–	–	2.5	ns	Cload = 15 pF, 8 mA drive strength
SID72	T_{RISES_1}	Rise time in Slow Strong Mode. 10% to 90% of V_{DD}	52	–	142	ns	Cload = 15 pF, 8 mA drive strength, V_{DD} ≤ 2.7 V
SID72A	T_{RISES_2}	Rise time in Slow Strong Mode. 10% to 90% of V_{DD}	48	–	102	ns	Cload = 15 pF, 8 mA drive strength, 2.7 V < V_{DD} ≤ 3.6 V
SID73	T_{FALLS_1}	Fall time in Slow Strong Mode. 10% to 90% of V_{DD}	44	–	211	ns	Cload = 15 pF, 8 mA drive strength, V_{DD} ≤ 2.7 V
SID73A	T_{FALLS_2}	Fall time in Slow Strong Mode. 10% to 90% of V_{DD}	42	–	93	ns	Cload = 15 pF, 8 mA drive strength, 2.7 V < V_{DD} ≤ 3.6 V
SID73G	T_{FALL_I2C}	Fall time (30% to 70% of V_{DD}) in Slow Strong mode	20 * V_{DDIO} / 5.5	–	250	ns	Cload = 10 pF to 400 pF, 8-mA drive strength
SID74	$F_{GPIOUT1}$	GPIO Fout. Fast Strong mode.	–	–	100	MHz	90/10%, 15-pF load, 60/40 duty cycle

Table 7. GPIO Specifications *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SID75	$F_{GPIOUT2}$	GPIO Fout; Slow Strong mode.	–	–	16.7	MHz	90/10%, 15-pF load, 60/40 duty cycle
SID76	$F_{GPIOUT3}$	GPIO Fout; Fast Strong mode.	–	–	7	MHz	90/10%, 25-pF load, 60/40 duty cycle
SID245	$F_{GPIOUT4}$	GPIO Fout; Slow Strong mode.	–	–	3.5	MHz	90/10%, 25-pF load, 60/40 duty cycle
SID246	F_{GPIOIN}	GPIO input operating frequency;1.71 V ≤ V_{DD} ≤ 3.6 V	–	–	100	MHz	90/10% V_{IO}

Analog Peripherals

Opamp

Table 8. Opamp Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
	I_{DD}	Opamp Block current. No load.	–	–	–		–
SID269	I_{DD_HI}	Power = Hi	–	1300	1500	µA	–
SID270	I_{DD_MED}	Power = Med	–	450	600	µA	–
SID271	I_{DD_LOW}	Power = Lo	–	250	350	µA	–
	GBW	Load = 20 pF, 0.1 mA. V_{DDA} = 2.7 V	–	–	–		–
SID272	G_{BW_HI}	Power = Hi	6	–	–	MHz	–
SID273	G_{BW_MED}	Power = Med	4	–	–	MHz	–
SID274	G_{BW_LO}	Power = Lo	–	1	–	MHz	–
	I_{OUT_MAX}	V_{DDA} ≥ 2.7 V, 500 mV from rail	–	–	–		–
SID275	$I_{OUT\_MAX\_HI}$	Power = Hi	10	–	–	mA	–
SID276	$I_{OUT\_MAX\_MID}$	Power = Mid	10	–	–	mA	–
SID277	$I_{OUT\_MAX\_LO}$	Power = Lo	–	5	–	mA	–
	I_{OUT}	V_{DDA} = 1.71 V, 500 mV from rail	–	–	–		–
SID278	$I_{OUT\_MAX\_HI}$	Power = Hi	4	–	–	mA	–
SID279	$I_{OUT\_MAX\_MID}$	Power = Mid	4	–	–	mA	–
SID280	$I_{OUT\_MAX\_LO}$	Power = Lo	–	2	–	mA	–
SID281	V_{IN}	Input voltage range	0	–	V_{DDA} – 0.2	V	–
SID282	V_{CM}	Input common mode voltage	0	–	V_{DDA} – 0.2	V	–
	V_{OUT}	V_{DDA} ≥ 2.7 V	–	–	–		–
SID283	V_{OUT_1}	Power = hi, Iload = 10 mA	0.5	–	V_{DDA} – 0.5	V	–
SID284	V_{OUT_2}	Power = hi, Iload = 1 mA	0.2	–	V_{DDA} – 0.2	V	–
SID285	V_{OUT_3}	Power = med, Iload = 1 mA	0.2	–	V_{DDA} – 0.2	V	–
SID286	V_{OUT_4}	Power = lo, Iload = 0.1 mA	0.2	–	V_{DDA} – 0.2	V	–
SID287	V_{OS_UNTR}	Offset voltage, untrimmed	–	–	–	mV	–
SID288	V_{OS_TR}	Offset voltage, trimmed	–1	±0.5	1	mV	High mode, 0.2 to V_{DDA} – 0.2
SID288A	V_{OS_TR}	Offset voltage, trimmed	–	±1	–	mV	Medium mode
SID288B	V_{OS_TR}	Offset voltage, trimmed	–	±2	–	mV	Low mode
SID289	$V_{OS\_DR\_UNTR}$	Offset voltage drift, untrimmed	–	–	–	µV/°C	–

Table 8. Opamp Specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID290	$V_{OS\_DR\_TR}$	Offset voltage drift, trimmed	–10	±3	10	µV/°C	High mode, 0.2 to V_{DDA} – 0.2
SID290A	$V_{OS\_DR\_TR}$	Offset voltage drift, trimmed	–	±10	–	µV/°C	Medium mode
SID290B	$V_{OS\_DR\_TR}$	Offset voltage drift, trimmed	–	±10	–	µV/°C	Low mode
SID291	CMRR	DC Common mode rejection ratio	67	80	–	dB	V_{DDD} = 3.3 V
SID292	PSRR	Power supply rejection ratio at 1 kHz, 10-mV ripple	70	85	–	dB	V_{DDD} = 3.3 V
Noise			–	–	–		–
SID293	VN1	Input-referred, 1 Hz–1 GHz, power = Hi	–	100	–	µVrms	–
SID294	VN2	Input-referred, 1 kHz, power = Hi	–	180	–	nV/rtHz	–
SID295	VN3	Input-referred, 10 kHz, power = Hi	–	70	–	nV/rtHz	–
SID296	VN4	Input-referred, 100 kHz, power = Hi	–	38	–	nV/rtHz	–
SID297	CLOAD	Stable up to max. load. Performance specs at 50 pF.	–	–	125	pF	–
SID298	SLEW_RATE	Output slew rate	6	–	–	V/µs	Cload = 50 pF, Power = High, $V_{DDA} \geq 2.7$ V
SID299	T_OP_WAKE	From disable to enable, no external RC dominating	–	25	–	µs	–
	COMP_MODE	Comparator mode; 50-mV overdrive, Trise = Tfall (approx.)	–		–		–
SID300	T_{PD1}	Response time; power = hi	–	150	–	ns	–
SID301	T_{PD2}	Response time; power = med	–	400	–	ns	–
SID302	T_{PD3}	Response time; power = lo	–	2000	–	ns	–
SID303	V_{HYST_OP}	Hysteresis	–	10	–	mV	–
Deep Sleep Mode		Mode 2 is lowest current range. Mode 1 has higher GBW.					Deep Sleep mode operation: $V_{DDA} \geq 2.7$ V. V_{IN} is 0.2 to V_{DDA} – 1.5 V
SID_DS_1	$I_{DD\_HI\_M1}$	Mode 1, High current	–	1300	1500	µA	Typ at 25 °C
SID_DS_2	$I_{DD\_MED\_M1}$	Mode 1, Medium current	–	460	600	µA	Typ at 25 °C
SID_DS_3	$I_{DD\_LOW\_M1}$	Mode 1, Low current	–	230	350	µA	Typ at 25 °C
SID_DS_4	$I_{DD\_HI\_M2}$	Mode 2, High current	–	120	–	µA	25 °C
SID_DS_5	$I_{DD\_MED\_M2}$	Mode 2, Medium current	–	60	–	µA	25 °C
SID_DS_6	$I_{DD\_LOW\_M2}$	Mode 2, Low current	–	15	–	µA	25 °C
SID_DS_7	GBW_HI_M1	Mode 1, High current	–	4	–	MHz	25 °C
SID_DS_8	GBW_MED_M1	Mode 1, Medium current	–	2	–	MHz	25 °C
SID_DS_9	GBW_LOW_M1	Mode 1, Low current	–	0.5	–	MHz	25 °C
SID_DS_10	GBW_HI_M2	Mode 2, High current	–	0.5	–	MHz	20-pF load, no DC load 0.2 V to V_{DDA} – 1.5 V
SID_DS_11	GBW_MED_M2	Mode 2, Medium current	–	0.2	–	MHz	20-pF load, no DC load 0.2 V to V_{DDA} – 1.5 V

Table 16. CSD ADC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
CSDv2 ADC Specifications							
SIDA94	A_RES	Resolution	–	–	10	bits	Auto-zeroing is required every milli-second
SID95	A_CHNLS_S	Number of channels - single ended	–	–	–	16	
SIDA97	A-MONO	Monotonicity	–	–	Yes	–	V_{REF} mode
SIDA98	A_GAINERR_VREF	Gain error	–	0.6	–	%	Reference Source: SRSS (V_{REF} = 1.20 V, V_{DDA} < 2.2 V), (V_{REF} = 1.6 V, 2.2 V < V_{DDA}<2.7 V), (V_{REF} = 2.13 V, V_{DDA}>2.7 V)
SIDA98A	A_GAINERR_VDDA	Gain error	–	0.2	–	%	Reference Source: SRSS (V_{REF} = 1.20 V, V_{DDA}< 2.2V), (V_{REF} = 1.6 V, 2.2 V < V_{DDA} < 2.7 V), (V_{REF} = 2.13 V, V_{DDA} > 2.7 V)
SIDA99	A_OFFSET_VREF	Input offset voltage	–	0.5	–	LSb	After ADC calibration, Ref. Src = SRSS, (V_{REF} = 1.20 V, V_{DDA} < 2.2 V), (V_{REF} = 1.6 V, 2.2 V<V_{DDA} < 2.7 V), (V_{REF} = 2.13 V, V_{DDA} > 2.7 V)
SIDA99A	A_OFFSET_VDDA	Input offset voltage	–	0.5	–	LSb	After ADC calibration, Ref. Src = SRSS, (V_{REF} = 1.20 V, V_{DDA} < 2.2 V), (V_{REF} = 1.6 V, 2.2 V<V_{DDA} < 2.7 V), (V_{REF} = 2.13 V, V_{DDA} > 2.7 V)
SIDA100	A_ISAR_VREF	Current consumption	–	0.3	–	mA	CSD ADC Block current
SIDA100A	A_ISAR_VDDA	Current consumption	–	0.3	–	mA	CSD ADC Block current
SIDA101	A_VINS_VREF	Input voltage range - single ended	V_{SSA}	–	V_{REF}	V	(V_{REF} = 1.20 V, V_{DDA} < 2.2 V), (V_{REF} =1.6 V, 2.2 V<V_{DDA} < 2.7 V), (V_{REF} = 2.13 V, V_{DDA} > 2.7 V)
SIDA101A	A_VINS_VDDA	Input voltage range - single ended	V_{SSA}	–	V_{DDA}	V	(V_{REF} = 1.20 V, V_{DDA} < 2.2 V), (V_{REF} = 1.6 V, 2.2 V<V_{DDA} < 2.7 V), (V_{REF} = 2.13 V, V_{DDA} > 2.7 V)
SIDA103	A_INRES	Input charging resistance	–	15	–	kΩ	
SIDA104	A_INCAP	Input capacitance	–	41	–	pF	
SIDA106	A_PSRR	Power supply rejection ratio (DC)	–	60	–	dB	
SIDA107	A_TACQ	Sample acquisition time	–	10	–	µs	Measured with 50-Ω source impedance. 10 µs is default software driver acquisition time setting. Settling to within 0.05%.
SIDA108	A_CONV8	Conversion time for 8-bit resolution at conversion rate = Fhclk/(2"(N+2)). Clock frequency = 50 MHz.	–	25	–	µs	Does not include acquisition time.
SIDA108A	A_CONV10	Conversion time for 10-bit resolution at conversion rate = Fhclk/(2"(N+2)). Clock frequency = 50 MHz.	–	60	–	µs	Does not include acquisition time.
SIDA109	A_SND_VRE	Signal-to-noise and Distortion ratio (SINAD)	–	57	–	dB	Measured with 50-Ω source impedance

Table 18. Serial Communication Block (SCB) Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
Fixed I^2C DC Specifications							
SID149	I_{I2C1}	Block current consumption at 100 kHz	–	–	30	µA	
SID150	I_{I2C2}	Block current consumption at 400 kHz	–	–	80	µA	
SID151	I_{I2C3}	Block current consumption at 1 Mbps	–	–	180	µA	
SID152	I_{I2C4}	I2C enabled in Deep Sleep mode	–	–	1.7	µA	At 60 °C
Fixed I^2C AC Specifications							
SID153	F_{I2C1}	Bit Rate	–	–	1	Mbps	
Fixed UART DC Specifications							
SID160	I_{UART1}	Block current consumption at 100 kbps	–	–	30	µA	
SID161	I_{UART2}	Block current consumption at 1000 kbps	–	–	180	µA	
Fixed UART AC Specifications							
SID162A	F_{UART1}	Bit Rate	–	–	3	Mbps	ULP Mode
SID162B	F_{UART2}		–	–	8		LP Mode
Fixed SPI DC Specifications							
SID163	I_{SPI1}	Block current consumption at 1Mbps	–	–	220	µA	
SID164	I_{SPI2}	Block current consumption at 4 Mbps	–	–	340	µA	
SID165	I_{SPI3}	Block current consumption at 8 Mbps	–	–	360	µA	
SID165A	I_{SP14}	Block current consumption at 25 Mbps	–	–	800	µA	
Fixed SPI AC Specifications for LP Mode (1.1 V) unless noted otherwise							
SID166	F_{SPI}	SPI Operating frequency Master and Externally Clocked Slave	–	–	25	MHz	14-MHz max for ULP (0.9 V) mode
SID166A	F_{SPI_IC}	SPI Slave Internally Clocked	–	–	15	MHz	5-MHz max for ULP (0.9 V) mode
Fixed SPI Master mode AC Specifications for LP Mode (1.1 V) unless noted otherwise							
SID167	T_{DMO}	MOSI Valid after SClock driving edge	–	–	12	ns	20-ns max for ULP (0.9 V) mode
SID168	T_{DSI}	MISO Valid before SClock capturing edge	5	–	–	ns	Full clock, late MISO sampling
SID169	T_{HMO}	MOSI data hold time	0	–	–	ns	Referred to Slave capturing edge
Fixed SPI Slave mode AC Specifications for LP Mode (1.1 V) unless noted otherwise							
SID170	T_{DMI}	MOSI Valid before Sclock Capturing edge	5	–	–	ns	
SID171A	T_{DSO_EXT}	MISO Valid after Sclock driving edge in Ext. Clk. mode	–	–	20	ns	35-ns max. for ULP (0.9 V) mode
SID171	T_{DSO}	MISO Valid after Sclock driving edge in Internally Clk. Mode	–	–	T_{DSO_EXT} + 3 * Tscb	ns	Tscb is Serial Comm Block clock period.
SID171B	T_{DSO}	MISO Valid after Sclock driving edge in Internally Clk. Mode with Median filter enabled.	–	–	T_{DSO_EXT} + 4 * Tscb	ns	Tscb is Serial Comm Block clock period.
SID172	T_{HSO}	Previous MISO data hold time	5	–	–	ns	
SID172A	$TSSEL_{SCK1}$	SSEL Valid to first SCK Valid edge	65	–	–	ns	
SID172B	$TSSEL_{SCK2}$	SSEL Hold after Last SCK Valid edge	65	–	–	ns	

Crystal Oscillator Specifications

Table 28. ECO Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
MHz ECO DC Specifications							
SID316	I_{DD_MHz}	Block operating current with Cload up to 18 pF	–	800	1600	µA	Max = 33 MHz, Type = 16 MHz
MHz ECO AC Specifications							
SID317	F_MHz	Crystal frequency range	4	–	33	MHz	–
kHz ECO DC Specification							
SID318	I_{DD_kHz}	Block operating current with 32-kHz crystal	–	0.38	1	µA	–
SID321E	ESR32K	Equivalent Series Resistance	–	80	–	kΩ	–
SID322E	PD32K	Drive level	–	–	1	µW	–
kHz ECO AC Specification							
SID319	F_kHz	32-kHz trimmed frequency	–	32.768	–	kHz	–
SID320	Ton_kHz	Startup time	–	–	500	ms	–
SID320E	F_{TOL32K}	Frequency tolerance	–	50	250	ppm	–

External Clock Specifications

Table 29. External Clock Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID305	$EXTCLK_{FREQ}$	External Clock input Frequency	0	–	100	MHz	–
SID306	$EXTCLK_{DUTY}$	Duty cycle; Measured at $V_{DD/2}$	45	–	55	%	–

Table 30. PLL Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID305P	PLL_LOCK	Time to achieve PLL Lock	–	16	35	µs	–
SID306P	PLL_OUT	Output frequency from PLL Block	–	–	150	MHz	–
SID307P	PLL_IDD	PLL Current	–	0.55	1.1	mA	Typ at 100 MHz out.
SID308P	PLL_JTR	Period Jitter	–	–	150	ps	100-MHz output frequency

Table 31. Clock Source Switching Time

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID262	$TCLK_{SWITCH}$	Clock switching from clk1 to clk2 in clock periods	–	–	4 clk1 + 3 clk2	periods	–

Table 32. Frequency Locked Loop (FLL) Specifications

SPEC ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
Frequency Locked Loop (FLL) Specifications							
SID450	FLL_RANGE	Input frequency range.	0.001	–	100	MHz	Lower limit allows lock to USB SOF signal (1 kHz). Upper limit is for External input.
SID451	FLL_OUT_DIV2	Output frequency range. V_{CCD} = 1.1 V	24.00	–	100.00	MHz	Output range of FLL divided-by-2 output
SID451A	FLL_OUT_DIV2	Output frequency range. V_{CCD} = 0.9 V	24.00	–	50.00	MHz	Output range of FLL divided-by-2 output
SID452	FLL_DUTY_DIV2	Divided-by-2 output; High or Low	47.00	–	53.00	%	
SID454	FLL_WAKEUP	Time from stable input clock to 1% of final value on deep sleep wakeup	–	–	7.50	µs	With IMO input, less than 10 °C change in temperature while in Deep Sleep, and Fout ≥ 50 MHz.
SID455	FLL_JITTER	Period jitter (1 sigma at 100 MHz)	–	–	35.00	ps	50 ps at 48 MHz, 35 ps at 100 MHz
SID456	FLL_CURRENT	CCO + Logic current	–	–	5.50	µA/MHz	

Table 33. UDB AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
Data Path Performance							
SID249	$F_{MAX-TIMER}$	Max frequency of 16-bit timer in a UDB pair	–	–	100	MHz	–
SID250	$F_{MAX-ADDER}$	Max frequency of 16-bit adder in a UDB pair	–	–	100	MHz	–
SID251	F_{MAX_CRC}	Max frequency of 16-bit CRC/PRS in a UDB pair	–	–	100	MHz	–
PLD Performance in UDB							
SID252	F_{MAX_PLD}	Max frequency of 2-pass PLD function in a UDB pair	–	–	100	MHz	–
Clock to Output Performance							
SID253	$T_{CLK\_OUT\_UDB1}$	Prop. delay for clock in to data out	–	5	–	ns	–
UDB Port Adaptor Specifications							
Conditions: 10-pF load, 3-V V_{DDIO} and V_{DDD}							
SID263	T_{LCLKDO}	LCLK to Output delay	–	–	11	ns	–
SID264	$T_{DINLCLK}$	Input setup time to LCLCK rising edge	–	–	7	ns	–
SID265	$T_{DINLCLKHLD}$	Input hold time from LCLK rising edge	5	–	–	ns	–
SID266	$T_{LCLKHIZ}$	LCLK to Output tristated	–	–	28	ns	–
SID267	T_{FLCLK}	LCLK frequency	–	–	33	MHz	–
SID268	$T_{LCLKDUTY}$	LCLK duty cycle (percentage high)	40%	–	60%	%	–

Note
5. The undivided output of the FLL must be a minimum of 2.5X the input frequency.

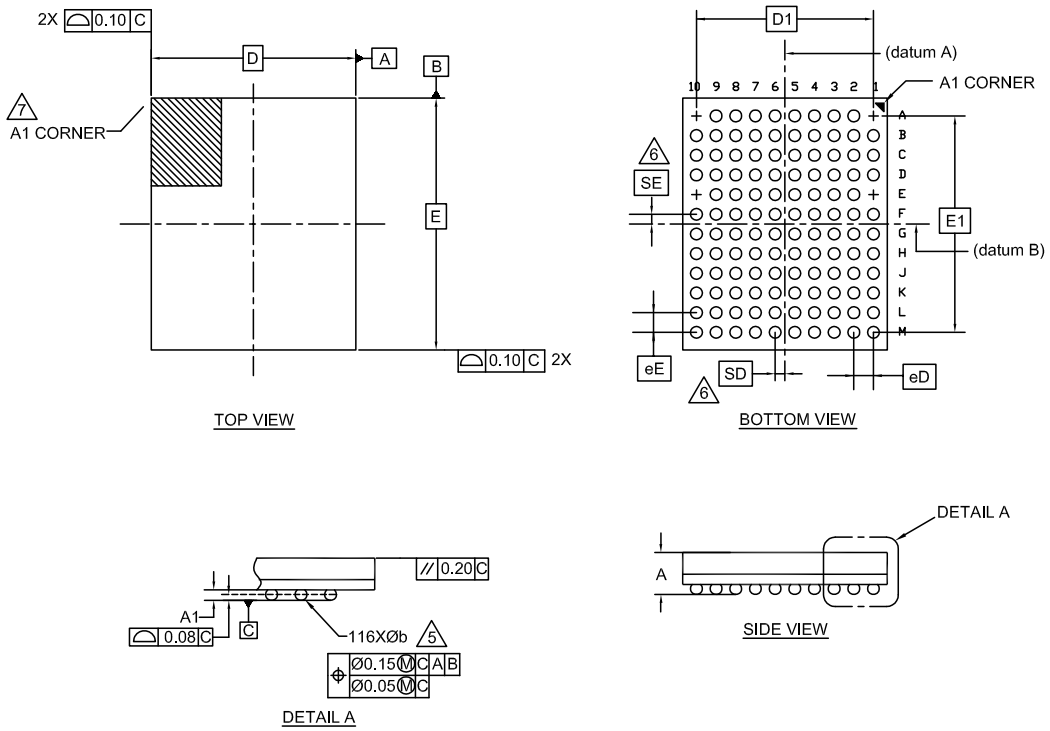
Table 36. Audio Subsystem Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
Audio Subsystem specifications							
PDM Specifications							
SID400P	PDM_IDD1	PDM Active current, Stereo operation, 1-MHz clock	–	175	–	µA	16-bit audio at 16 ksps
SID401	PDM_IDD2	PDM Active current, Stereo operation, 3-MHz clock	–	600	–	µA	24-bit audio at 48 ksps
SID402	PDM_JITTER	RMS Jitter in PDM clock	–200	–	200	ps	
SID403	PDM_CLK	PDM Clock speed	0.384	–	3.072	MHz	
SID403A	PDM_BLK_CLK	PDM Block input clock	1.024	–	49.152	MHz	
SID403B	PDM_SETUP	Data input set-up time to PDM_CLK edge	10	–	–	ns	
SID403C	PDM_HOLD	Data input hold time to PDM_CLK edge	10	–	–	ns	
SID404	PDM_OUT	Audio sample rate	8	–	48	ksps	
SID405	PDM_WL	Word Length	16	–	24	bits	
SID406	PDM_SNR	Signal-to-Noise Ratio (A-weighted0	–	100	–	dB	PDM input, 20 Hz to 20 kHz BW
SID407	PDM_DR	Dynamic Range (A-weighted)	–	100	–	dB	20 Hz to 20 kHz BW, –60 dB FS
SID408	PDM_FR	Frequency Response	–0.2	–	0.2	dB	DC to 0.45. DC Blocking filter off.
SID409	PDM_SB	Stop Band	–	0.566	–	f	
SID410	PDM_SBA	Stop Band Attenuation	–	60	–	dB	
SID411	PDM_GAIN	Adjustable Gain	–12	–	10.5	dB	PDM to PCM, 1.5 dB/step
SID412	PDM_ST	Startup time	–	48	–		WS (Word Select) cycles
I2S Specifications. The same for LP and ULP modes unless stated otherwise.							
SID413	I2S_WORD	Length of I2S Word	8	–	32	bits	
SID414	I2S_WS	Word Clock frequency in LP mode	–	–	192	kHz	12.288-MHz bit clock with 32-bit word
SID414M	I2S_WS_U	Word Clock frequency in ULP mode	–	–	48	kHz	3.072-MHz bit clock with 32-bit word
SID414A	I2S_WS_TDM	Word Clock frequency in TDM mode for LP	–	–	48	kHz	8 32-bit channels
SID414X	I2S_WS_TDM_U	Word Clock frequency in TDM mode for ULP	–	–	12	kHz	8 32-bit channels
I2S Slave Mode							
SID430	TS_WS	WS Setup Time to the Following Rising Edge of SCK for LP Mode	5	–	–	ns	
SID430U	TS_WS	WS Setup Time to the Following Rising Edge of SCK for ULP Mode	11	–	–	ns	
SID430A	TH_WS	WS Hold Time to the Following Edge of SCK	TMCLK_SOC + 5	–	–	ns	

Table 40. Precision ILO (PILO) Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID 430R	I_{PILO}	Operating current	–	1.2	4	µA	–
SID431	F_PILO	PILO nominal frequency	–	32768	–	Hz	T = 25 °C with 20-ppm crystal
SID432R	ACC_PILO	PILO accuracy with periodic calibration	–500	–	500	ppm	–

Figure 5. 116-BGA 5.2 × 6.4 × 0.70 mm



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	-	-	0.70
A1	0.16	0.21	0.26
D	5.20 BSC		
E	6.40 BSC		
D1	4.50 BSC		
E1	5.50 BSC		
MD	10		
ME	12		
N	116		
Ø b	0.25	0.30	0.35
eD	0.50 BSC		
eE	0.50 BSC		
SD	0.25 BSC		
SE	0.25 BSC		

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. SOLDER BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.
3. "e" REPRESENTS THE SOLDER BALL GRID PITCH.
4. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
   N IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
5. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
6. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW "SD" OR "SE" = 0.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
7. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK METALIZED MARK, INDENTATION OR OTHER MEANS.
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED SOLDER BALLS.
9. JEDEC SPECIFICATION NO. REF: N/A

002-16574 *B

Table 47. Acronyms Used in this Document *(continued)*

Acronym	Description
PCB	printed circuit board
PGA	programmable gain amplifier
PHUB	peripheral hub
PHY	physical layer
PICU	port interrupt control unit
PLA	programmable logic array
PLD	programmable logic device, see also PAL
PLL	phase-locked loop
PMDD	package material declaration data sheet
POR	power-on reset
PRES	precise power-on reset
PRS	pseudo random sequence
PS	port read data register
PSoC®	Programmable System-on-Chip™
PSRR	power supply rejection ratio
PWM	pulse-width modulator
RAM	random-access memory
RISC	reduced-instruction-set computing
RMS	root-mean-square
RTC	real-time clock
RTL	register transfer language
RTR	remote transmission request
RX	receive
SAR	successive approximation register
SC/CT	switched capacitor/continuous time
SCL	I^2C serial clock
SDA	I^2C serial data
S/H	sample and hold
SINAD	signal to noise and distortion ratio
SIO	special input/output, GPIO with advanced features. See GPIO.
SOC	start of conversion
SOF	start of frame
SPI	Serial Peripheral Interface, a communications protocol
SR	slew rate
SRAM	static random access memory
SRES	software reset
SWD	serial wire debug, a test protocol
SWV	single-wire viewer

Table 47. Acronyms Used in this Document *(continued)*

Acronym	Description
TD	transaction descriptor, see also DMA
THD	total harmonic distortion
TIA	transimpedance amplifier
TRM	technical reference manual
TTL	transistor-transistor logic
TX	transmit
UART	Universal Asynchronous Transmitter Receiver, a communications protocol
UDB	universal digital block
USB	Universal Serial Bus
USBIO	USB input/output, PSoC pins used to connect to a USB port
VDAC	voltage DAC, see also DAC, IDAC
WDT	watchdog timer
WOL	write once latch, see also NVL
WRES	watchdog timer reset
XRES	external reset I/O pin
XTAL	crystal