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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4/M0
Core Size	32-Bit Dual-Core
Speed	100MHz, 150MHz
Connectivity	I²C, LINbus, QSPI, SPI, UART/USART, USB
Peripherals	Bluetooth, Brown-out Detect/Reset, Cap Sense, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	78
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	32K x 8
RAM Size	288K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 8x12b SAR; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	116-WFBGA
Supplier Device Package	116-BGA (5.2x6.4)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c6347bzi-bld53

Functional Definition

CPU and Memory Subsystem

CPU

The CPU subsystem in the PSoC 63 consists of two Arm Cortex cores and their associated busses and memories: M4 with Floating-point unit and Memory Protection Units (FPU and MPU) and an M0+ with an MPU. The Cortex M4 and M0+ have 8 KB Instruction Caches (I-Cache) with 4-way set associativity. This subsystem also includes independent DMA controllers with 32 channels each, a Cryptographic accelerator block, 1 MB of on-chip Flash, 288 KB of SRAM, and 128 KB of ROM.

The Cortex M0+ provides a secure, un-interruptible Boot function. This guarantees that post-Boot, system integrity is checked and privileges enforced. Shared resources can be accessed through the normal Arm multi-layer bus arbitration and exclusive accesses are supported by an Inter-Processor Communication (IPC) scheme, which implements hardware semaphores and protection. Active power consumption for the Cortex M4 is 22 µA/MHz and 15 µA/MHz for the Cortex M0+, both at 3.3 V chip supply voltage with the internal buck enabled and at 0.9 V internal supply. Note that at Cortex M4 speeds above 100 MHz, the M0+ and Peripheral subsystem are limited to half the M4 speed. If the M4 is running at 150 Mhz, the M0+and peripheral subsystem is limited to 75 MHz.

DMA Controllers

There are two DMA controllers with 16 channels each. They support independent accesses to peripherals using the AHB Multi-layer bus.

Flash

PSoC 63 has a 1 MB flash module with additional 32 KB of Flash that can be used for EEPROM emulation for longer retention and a separate 32 KB block of Flash that can be securely locked and is only accessible via a key lock that cannot be changed (one Time Programmable).

SRAM with 32 KB Retention Granularity

There is 288 KB of SRAM memory, which can be fully retained or retained in increments of user-designated 32 KB blocks.

SROM

There is a supervisory 128 KB ROM that contains boot and configuration routines. This ROM will guarantee Secure Boot if authentication of User Flash is required.

One-Time-Programmable (OTP) eFuse

The 1024-bit OTP memory can provide a unique and unalterable Identifier on a per-chip basis. This unalterable key can be used to access Secured Flash.

System Resources

Power System

The power system provides assurance that voltage levels are as required for each respective mode and will either delay mode entry (on power-on reset (POR), for example) until voltage levels are as required for proper function or generate resets (Brown-Out Detect (BOD)) when the power supply drops below specified levels. The design will guaranteed safe chip operation between power supply voltage dropping below specified levels (for example, below 1.7 V) and the Reset occurring. There are no voltage sequencing requirements. The VDD core logic supply (1.7 to 3.6 V) will feed an on-chip buck, which will produce the core logic supply of either 1.1 V or 0.9 V selectable. Depending on the frequency of operation, the buck converter will have a quiescent current of <1 µA. A separate power domain called Backup is provided; note this is not a power mode. This domain is powered from the VBACKUP domain and includes the 32-kHz WCO, RTC, and backup registers. It is connected to VDD when not used as a backup domain. Port 0 is powered from this supply. Pin 5 of Port 0 (P0.5) can be assigned as a PMIC wakeup output (timed by the RTC); P0.5 is driven to the resistive pull-up mode by default.

Clock System

The PSoC 63 clock system is responsible for providing clocks to all subsystems that require clocks and for switching between different clock sources without glitching. In addition, the clock system ensures that no metastable conditions occur.

The clock system for PSoC 63 consists of the Internal Main Oscillator (IMO) and the Internal Low-speed Oscillator (ILO), crystal oscillators (ECO and WCO), PLL, FLL, and provision for an external clock. An FLL will provide fast wake-up at high clock speeds without waiting for a PLL lock event (which can take up to 50 µs). Clocks may be buffered and brought out to a pin on a Smart I/O port.

The 32-kHz oscillator is trimmable to within 2 ppm using a higher accuracy clock. The ECO will deliver ±20 ppm accuracy and will use an external crystal.

IMO Clock Source

The IMO is the primary source of internal clocking in PSoC 63. It is trimmed during testing to achieve the specified accuracy. The IMO default frequency is 8 MHz. IMO tolerance is ±2% and its current consumption is less than 10 µA.

ILO Clock Source

The ILO is a very low power oscillator, nominally 32 kHz, which may be used to generate clocks for peripheral operation in Deep Sleep mode. ILO-driven counters can be calibrated to the IMO to improve accuracy. Cypress provides a software component, which does the calibration.

Watchdog Timer

A watchdog timer is implemented in the clock block running from the ILO or from the WCO; this allows watchdog operation during Deep Sleep and Hibernate modes, and generates a watchdog reset if not serviced before the timeout occurs. The watchdog reset is recorded in the Reset Cause register.

Clock Dividers

Integer and Fractional clock dividers are provided for peripheral use and timing purposes. There are eight 8-bit integer and sixteen 16-bit integer clock dividers. There is also one 24.5-bit fractional and four 16.5-bit fractional clock dividers.

Reset

The PSoC 63 can be reset from a variety of sources including a software reset. Reset events are asynchronous and guarantee reversion to a known state. The reset cause is recorded in a register, which is sticky through reset and allows software to determine the cause of the Reset. An XRES pin is reserved for external reset to avoid complications with configuration and multiple pin functions during power-on or reconfiguration.

BLE Radio and Subsystem

PSoC 63 incorporates a Bluetooth Smart subsystem that contains the Physical Layer (PHY) and Link Layer (LL) engines with an embedded security engine. The physical layer consists of the digital PHY and the RF transceiver that transmits and receives GFSK packets at 2 Mbps over a 2.4-GHz ISM band, which is compliant with Bluetooth Smart Bluetooth Specification 5.0. The baseband controller is a composite hardware and firmware implementation that supports both master and slave modes. Key protocol elements, such as HCI and link control, are implemented in firmware. Time-critical functional blocks, such as encryption, CRC, data whitening, and access code correlation, are implemented in hardware (in the LL engine).

The RF transceiver contains an integrated balun, which provides a single-ended RF port pin to drive a 50-Ω antenna via a matching/filtering network. In the receive direction, this block converts the RF signal from the antenna to a digital bit stream after performing GFSK demodulation. In the transmit direction, this block performs GFSK modulation and then converts a digital baseband signal to a radio frequency before transmitting it to air through the antenna.

Key features of BLESS are as follows:

- Master and slave single-mode protocol stack with logical link control and adaptation protocol (L2CAP), attribute (ATT), and security manager (SM) protocols
- API access to generic attribute profile (GATT), generic access profile (GAP), and L2CAP
- L2CAP connection-oriented channel (Bluetooth 4.1 feature)
- GAP features
  - Broadcaster, Observer, Peripheral, and Central roles
  - Security mode 1: Level 1, 2, and 3
  - User-defined advertising data
  - Multiple bond support
- GATT features
  - GATT client and server
  - Supports GATT sub-procedures
  - 32-bit universally unique identifier (UUID) (Bluetooth 4.1 feature)
- Security Manager (SM)
  - Pairing methods: Just works, Passkey Entry, and Out of Band
  - LE Secure Connection Pairing model
  - Authenticated man-in-the-middle (MITM) protection and data signing
- Link Layer (LL)
  - Master and Slave roles
  - 128-bit AES engine
  - Low-duty cycle advertising
  - LE Ping
- Supports all SIG-adopted BLE profiles
- Power levels for Adv (1.28s, 31 bytes, 0 dBm) and Con (300 ms, 0 byte, 0 dBm) are 42 µW and 70 µW respectively

Analog Blocks

12-bit SAR ADC

The 12-bit, 1-Msps SAR ADC can operate at a maximum clock rate of 18 MHz and requires a minimum of 18 clocks at that frequency to do a 12-bit conversion.

The block functionality is augmented for the user by adding a reference buffer to it (trimmable to ±1%) and by providing the choice of three internal voltage references, V_{DD}, $V_{DD}/2$, and V_{REF} (nominally 1.024 V), as well as an external reference through a GPIO pin. The Sample-and-Hold (S/H) aperture is programmable; it allows the gain bandwidth requirements of the amplifier driving the SAR inputs, which determine its settling time, to be relaxed if required. System performance will be 65 dB for true 12-bit precision provided appropriate references are used and system noise levels permit it. To improve the performance in noisy conditions, it is possible to provide an external bypass (through a fixed pin location) for the internal reference amplifier.

The SAR is connected to a fixed set of pins through an 8-input sequencer. The sequencer cycles through the selected channels autonomously (sequencer scan) and does so with zero switching overhead (that is, the aggregate sampling bandwidth is equal to 1 Msps whether it is for a single channel or distributed over several channels). The sequencer switching is effected through a state machine or through firmware-driven switching. A feature provided by the sequencer is the buffering of each channel to reduce CPU interrupt-service requirements. To accommodate signals with varying source impedances and frequencies, it is possible to have different sample times programmable for each channel. Also, the signal range specification through a pair of range registers (low and high range values) is implemented with a corresponding out-of-range interrupt if the digitized value exceeds the programmed range; this allows fast detection of out-of-range values without having to wait for a sequencer scan to be completed and the CPU to read the values and check for out-of-range values in software. There are 16 channels of which any 13 can be sampled in a single scan.

Each Port Pin has multiple alternate functions. These are defined in Table 2.

Table 2. Multiple Alternate Functions

Port/ Pin	ACT #0	ACT #1	DS #2	ACT #4	ACT #5	ACT #6	ACT #7	ACT #8	ACT #9	ACT #10	ACT #12	ACT #13	ACT #14	ACT #15	DS #4	DS #5	DS #6
P0.0	tcpwm[0].line[0]:0	tcpwm[1].line[0]:0		srss.ext_clk:0				scb[0].spi_select1:0			peri.tr_io_input[0]:0						
P0.1	tcpwm[0].line_compl[0]:0	tcpwm[1].line_compl[0]:0						scb[0].spi_select2:0			peri.tr_io_input[1]:0					cpuss.swj_trstn	
P0.2	tcpwm[0].line[1]:0	tcpwm[1].line[1]:0				scb[0].uart_rx:0	scb[0].i2c_scl:0	scb[0].spi_mosi:0									
P0.3	tcpwm[0].line_compl[1]:0	tcpwm[1].line_compl[1]:0				scb[0].uart_tx:0	scb[0].i2c_sda:0	scb[0].spi_miso:0									
P0.4	tcpwm[0].line[2]:0	tcpwm[1].line[2]:0				scb[0].uart_rts:0		scb[0].spi_clk:0				peri.tr_io_output[0]:2					
P0.5	tcpwm[0].line_compl[2]:0	tcpwm[1].line_compl[2]:0		srss.ext_clk:1		scb[0].uart_cts:0		scb[0].spi_select0:0				peri.tr_io_output[1]:2					
P1.0	tcpwm[0].line[3]:0	tcpwm[1].line[3]:0				scb[7].uart_rx:0	scb[7].i2c_scl:0	scb[7].spi_mosi:0			peri.tr_io_input[2]:0						
P1.1	tcpwm[0].line_compl[3]:0	tcpwm[1].line_compl[3]:0				scb[7].uart_tx:0	scb[7].i2c_sda:0	scb[7].spi_miso:0			peri.tr_io_input[3]:0						
P1.2	tcpwm[0].line[4]:4	tcpwm[1].line[12]:1				scb[7].uart_rts:0		scb[7].spi_clk:0									
P1.3	tcpwm[0].line_compl[4]:4	tcpwm[1].line_compl[12]:1				scb[7].uart_cts:0		scb[7].spi_select0:0									
P1.4	tcpwm[0].line[5]:4	tcpwm[1].line[13]:1						scb[7].spi_select1:0									
P1.5	tcpwm[0].line_compl[5]:4	tcpwm[1].line_compl[14]:1						scb[7].spi_select2:0									
P5.0	tcpwm[0].line[4]:0	tcpwm[1].line[4]:0				scb[5].uart_rx:0	scb[5].i2c_scl:0	scb[5].spi_mosi:0		audioss.clk_i2s_if	peri.tr_io_input[10]:0						
P5.1	tcpwm[0].line_compl[4]:0	tcpwm[1].line_compl[4]:0				scb[5].uart_tx:0	scb[5].i2c_sda:0	scb[5].spi_miso:0		audioss.tx_sck	peri.tr_io_input[11]:0						
P5.2	tcpwm[0].line[5]:0	tcpwm[1].line[5]:0				scb[5].uart_rts:0		scb[5].spi_clk:0		audioss.tx_ws							
P5.3	tcpwm[0].line_compl[5]:0	tcpwm[1].line_compl[5]:0				scb[5].uart_cts:0		scb[5].spi_select0:0		audioss.tx_sdo							
P5.4	tcpwm[0].line[6]:0	tcpwm[1].line[6]:0						scb[5].spi_select1:0		audioss.rx_sck							
P5.5	tcpwm[0].line_compl[6]:0	tcpwm[1].line_compl[6]:0						scb[5].spi_select2:0		audioss.rx_ws							

Table 2. Multiple Alternate Functions *(continued)*

Port/ Pin	ACT #0	ACT #1	DS #2	ACT #4	ACT #5	ACT #6	ACT #7	ACT #8	ACT #9	ACT #10	ACT #12	ACT #13	ACT #14	ACT #15	DS #4	DS #5	DS #6
P8.0	tcpwm[0].line[0]:2	tcpwm[1].line[16]:0				scb[4].uart_rx:0	scb[4].i2c_scl:0	scb[4].spi_mosi:0			peri.tr_io_input[16]:0						
P8.1	tcpwm[0].line_compl[0]:2	tcpwm[1].line_compl[16]:0				scb[4].uart_tx:0	scb[4].i2c_sda:0	scb[4].spi_miso:0			peri.tr_io_input[17]:0						
P8.2	tcpwm[0].line[1]:2	tcpwm[1].line[17]:0				scb[4].uart_rts:0		scb[4].spi_clk:0									
P8.3	tcpwm[0].line_compl[1]:2	tcpwm[1].line_compl[17]:0				scb[4].uart_cts:0		scb[4].spi_select0:0									
P8.4	tcpwm[0].line[2]:2	tcpwm[1].line[18]:0						scb[4].spi_select1:0									
P8.5	tcpwm[0].line_compl[2]:2	tcpwm[1].line_compl[18]:0						scb[4].spi_select2:0									
P8.6	tcpwm[0].line[3]:2	tcpwm[1].line[19]:0						scb[4].spi_select3:0									
P8.7	tcpwm[0].line_compl[3]:2	tcpwm[1].line_compl[19]:0						scb[3].spi_select2:0									
P9.0	tcpwm[0].line[4]:2	tcpwm[1].line[20]:0				scb[2].uart_rx:0	scb[2].i2c_scl:0	scb[2].spi_mosi:0			peri.tr_io_input[18]:0			cpuss.trace_data[3]:0			
P9.1	tcpwm[0].line_compl[4]:2	tcpwm[1].line_compl[20]:0				scb[2].uart_tx:0	scb[2].i2c_sda:0	scb[2].spi_miso:0			peri.tr_io_input[19]:0			cpuss.trace_data[2]:0			
P9.2	tcpwm[0].line[5]:2	tcpwm[1].line[21]:0				scb[2].uart_rts:0		scb[2].spi_clk:0		pass.dsi_ctb_cmp0:1				cpuss.trace_data[1]:0			
P9.3	tcpwm[0].line_compl[5]:2	tcpwm[1].line_compl[21]:0				scb[2].uart_cts:0		scb[2].spi_select0:0		pass.dsi_ctb_cmp1:1				cpuss.trace_data[0]:0			
P9.4	tcpwm[0].line[7]:5	tcpwm[1].line[0]:2						scb[2].spi_select1:0									
P9.5	tcpwm[0].line_compl[7]:5	tcpwm[1].line_compl[0]:2						scb[2].spi_select2:0									
P9.6	tcpwm[0].line[0]:6	tcpwm[1].line[1]:2						scb[2].spi_select3:0									
P9.7	tcpwm[0].line_compl[0]:6	tcpwm[1].line_compl[1]:2															
P10.0	tcpwm[0].line[6]:2	tcpwm[1].line[22]:0				scb[1].uart_rx:1	scb[1].i2c_scl:1	scb[1].spi_mosi:1			peri.tr_io_input[20]:0			cpuss.trace_data[3]:1			
P10.1	tcpwm[0].line_compl[6]:2	tcpwm[1].line_compl[22]:0				scb[1].uart_tx:1	scb[1].i2c_sda:1	scb[1].spi_miso:1			peri.tr_io_input[21]:0			cpuss.trace_data[2]:1			

Table 3. Port Pin Analog, Smart I/O, and DSI Functions *(continued)*

Port/Pin	Name	Analog	Digital HV	DSI	SMARTIO
P6.3	P6.3	lpcomp.inn_comp1		dsi[4].port_if[3]	
P6.4	P6.4			dsi[4].port_if[4]	
P6.5	P6.5			dsi[4].port_if[5]	
P6.6	P6.6		swd_data	dsi[4].port_if[6]	
P6.7	P6.7		swd_clk	dsi[4].port_if[7]	
P7.0	P7.0			dsi[5].port_if[0]	
P7.1	P7.1	csd.cmodpadd csd.cmodpads		dsi[5].port_if[1]	
P7.2	P7.2	csd.csh_tankpadd csd.csh_tankpads		dsi[5].port_if[2]	
P7.3	P7.3	csd.vref_ext		dsi[5].port_if[3]	
P7.4	P7.4			dsi[5].port_if[4]	
P7.5	P7.5			dsi[5].port_if[5]	
P7.6	P7.6			dsi[5].port_if[6]	
P7.7	P7.7	csd.cshieldpads		dsi[5].port_if[7]	
P8.0	P8.0			dsi[11].port_if[0]	smartio[8].io[0]
P8.1	P8.1			dsi[11].port_if[1]	smartio[8].io[1]
P8.2	P8.2			dsi[11].port_if[2]	smartio[8].io[2]
P8.3	P8.3			dsi[11].port_if[3]	smartio[8].io[3]
P8.4	P8.4			dsi[11].port_if[4]	smartio[8].io[4]
P8.5	P8.5			dsi[11].port_if[5]	smartio[8].io[5]
P8.6	P8.6			dsi[11].port_if[6]	smartio[8].io[6]
P8.7	P8.7			dsi[11].port_if[7]	smartio[8].io[7]
P9.0	P9.0	ctb_oa0+		dsi[10].port_if[0]	smartio[9].io[0]
P9.1	P9.1	ctb_oa0-		dsi[10].port_if[1]	smartio[9].io[1]
P9.2	P9.2	ctb_oa0_out		dsi[10].port_if[2]	smartio[9].io[2]
P9.3	P9.3	ctb_oa1_out		dsi[10].port_if[3]	smartio[9].io[3]
P9.4	P9.4	ctb_oa1-		dsi[10].port_if[4]	smartio[9].io[4]
P9.5	P9.5	ctb_oa1+		dsi[10].port_if[5]	smartio[9].io[5]
P9.6	P9.6	ctb_oa0+		dsi[10].port_if[6]	smartio[9].io[6]
P9.7	P9.7	ctb_oa1+ or ext_vref		dsi[10].port_if[7]	smartio[9].io[7]
P10.0	P10.0	sarmux[0]		dsi[9].port_if[0]	
P10.1	P10.1	sarmux[1]		dsi[9].port_if[1]	
P10.2	P10.2	sarmux[2]		dsi[9].port_if[2]	
P10.3	P10.3	sarmux[3]		dsi[9].port_if[3]	
P10.4	P10.4	sarmux[4]		dsi[9].port_if[4]	
P10.5	P10.5	sarmux[5]		dsi[9].port_if[5]	
P10.6	P10.6	sarmux[6]		dsi[9].port_if[6]	
P10.7	P10.7	sarmux[7]		dsi[9].port_if[7]	
P11.0	P11.0			dsi[8].port_if[0]	
P11.1	P11.1			dsi[8].port_if[1]	

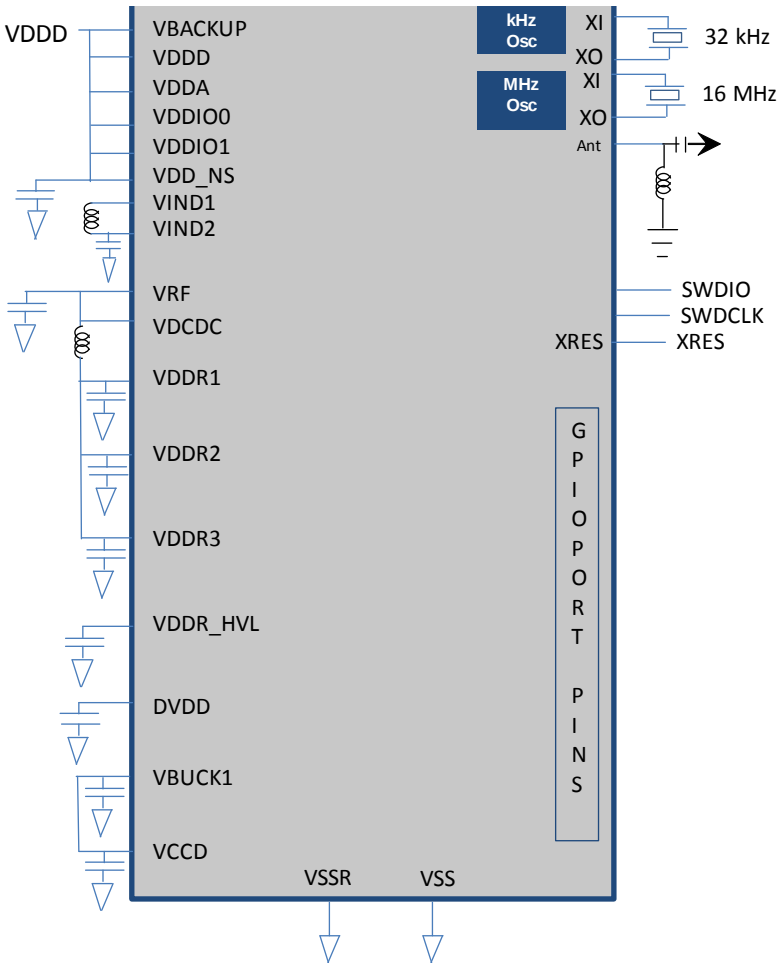
Power

The power system diagram (see Figure 3) shows the general requirements for power pins on the PSoC 63. The diagram also shows the radio pins that need to be decoupled. The PSoC 63 power scheme allows different VDDIO and VDDA connections. Since no sequencing requirements need to be analyzed and specified, customers may bring up the power supplies in any order and the power system is responsible for ensuring power is good in all domains before allowing operation. VDDD, VDDA, and VDDIO may be separate nets, which are not ohmically connected on chip. Depending on different package requirements, these may be required to be connected off chip.

The power system will have a buck regulator in addition to an LDO. A Single Input Multiple Output (SIMO) Buck regulator with multiple outputs allows saving an inductor and also providing a high-efficiency supply to the radio.

The preliminary diagram is shown in Figure 3.

Figure 3. SOC Power Connections with Radio (For 104-CSP and 116-BGA Packages)



Electrical Specifications

Note: These are preliminary and subject to change.

Absolute Maximum Ratings

Table 4. Absolute Maximum Ratings[1]

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SID1	V_{DD_ABS}	Analog or digital supply relative to V_{SS} (V_{SSD} = V_{SSA})	–0.5	–	4	V	Absolute Maximum
SID2	V_{CCD_ABS}	Direct digital core voltage input relative to Vssd	–0.5	–	1.2	V	Absolute Maximum
SID3	V_{GPIO_ABS}	GPIO voltage; V_{DDD} or V_{DDA}	–0.5	–	V_{DD} + 0.5	V	Absolute Maximum
SID4	I_{GPIO_ABS}	Current per GPIO	–25	–	25	mA	Absolute Maximum
SID5	$I_{GPIO\_injection}$	GPIO injection current per pin	–0.5	–	0.5	mA	Absolute Maximum
SID3A	ESD_HBM	Electrostatic discharge Human Body Model	2200	–	–	V	Absolute Maximum
SID3B	ESD_HBM_ ANT	Electrostatic discharge Human Body Model; Antenna Pin	500	–	–	V	Absolute Maximum; RF pin
SID4A	ESD_CDM	Electrostatic discharge Charged Device Model	500	–	–	V	Absolute Maximum
SID4B	ESD_CDM_ ANT	Electrostatic discharge Charged Device Model; Antenna Pin	200	–	–	V	Absolute Maximum; RF pin
SID5A	LU	Pin current for latchup-free operation	–100	–	100	mA	Absolute Maximum

Device-Level Specifications

All specifications are valid for –40 °C ≤ TA ≤ 85 °C and for 1.71 V to 3.6 V except where noted.

Table 5. Power Supply Range, CPU Current, and Transition Time Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
DC Specifications							
SID6	V_{DDD}	Internal regulator and Port 1 GPIO supply	1.7	–	3.6	V	Also supplies Port 0 in 56 QFN
SID7	V_{DDA}	Analog power supply voltage. Shorted to V_{DDIOA} on PCB.	1.7	–	3.6	V	Internally unregulated Supply
SID7A	V_{DDIO1}	GPIO Supply for Ports 5 to 8 when present	1.7	–	3.6	V	V_{DDIO_1} must be ≥ to V_{DDA}.
SID7B	V_{DDIO0}	GPIO Supply for Ports 11 to 13 when present	1.7	–	3.6	V	
SID7E	V_{DDIO0}	Supply for E-Fuse Programming	2.38	2.5	2.62	V	E-Fuse Programming Voltage
SID7C	V_{DDIOR}	GPIO supply for Ports 2 to 4 on BGA 124 only	1.7	–	3.6	V	
SID7D	V_{DDIOA}	GPIO Supply for Ports 9 to 10. Shorted to V_{DDA} on PCB.	1.7	–	3.6	V	Also supplies Ports 5 to 7 in 56 QFN

Note
1. Usage above the absolute maximum conditions listed in Table 4 may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods of time may affect device reliability. The maximum storage temperature is 150 °C in compliance with JEDEC Standard JESD22-A103, High Temperature Storage Life. When used below absolute maximum conditions but above normal operating conditions, the device may not operate to specification.

Table 5. Power Supply Range, CPU Current, and Transition Time Specifications *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SID7F	V_{DDUSB}	Supply for Port 14 (USB or GPIO) when present	1.7	–	3.6	V	Min supply is 2.85 V for USB
SID6B	V_{BACKUP}	Backup Power and GPIO Port 0 supply when present	1.7	–	3.6	V	Min is 1.4 V in Backup mode
SID8	V_{CCD1}	Output voltage (for core logic bypass)	–	1.1	–	V	High-speed mode
SID9	V_{CCD2}	Output voltage (for core logic bypass)	–	0.9	–		ULP mode. Valid for –20 to 85 °C
SID10	C_{EFC}	External regulator voltage (V_{CCD}) bypass	3.8	4.7	5.6	µF	X5R ceramic or better
SID11	C_{EXC}	Power supply decoupling capacitor	–	10	–	µF	X5R ceramic or better
LP RANGE POWER SPECIFICATIONS (for V_{CCD} = 1.1 V with Buck and LDO)							
Cortex M4. Active Mode							
Execute with Cache Disabled (Flash)							
SIDF1	I_{DD1}	Execute from Flash; CM4 Active 50 MHz, CM0+ Sleep 25 MHz. With IMO & FLL. While(1).	–	2.3	3.2	mA	V_{DDD} = 3.3 V, Buck ON, max at 60 °C
			–	3.1	3.6		V_{DDD} = 1.8 V, Buck ON, max at 60 °C
			–	4.2	5.1		V_{DDD} = 1.8 to 3.3 V, LDO, max at 60 °C
SIDF2	I_{DD2}	Execute from Flash; CM4 Active 8 MHz, CM0+ Sleep 8 MHz.With IMO. While(1)	–	0.9	1.5	mA	V_{DDD} = 3.3 V, Buck ON, max at 60 °C
			–	1.2	1.6		V_{DDD} = 1.8 V, Buck ON, max at 60 °C
			–	1.6	2.4		V_{DDD} = 1.8 to 3.3 V, LDO, max at 60 °C
Execute with Cache Enabled							
SIDC1	I_{DD3}	Execute from Cache;CM4 Active 150 MHz, CM0+ Sleep 75 MHz. IMO & FLL. Dhrystone.	–	6.3	7	mA	V_{DDD} = 3.3 V, Buck ON, max at 60 °C
			–	9.7	11.2		V_{DDD} = 1.8 V, Buck ON, max at 60 °C
			–	13.2	13.7		V_{DDD} = 1.8 to 3.3 V, LDO, max at 60 °C
SIDC2	I_{DD4}	Execute from Cache;CM4 Active 100 MHz, CM0+ Sleep 100MHz. IMO & FLL. Dhrystone.	–	4.8	5.8	mA	V_{DDD} = 3.3 V, Buck ON, max at 60 °C
			–	7.4	8.4		V_{DDD} = 1.8 V, Buck ON, max at 60 °C
			–	10.1	10.7		V_{DDD} = 1.8 to 3.3 V, LDO, max at 60 °C
SIDC3	I_{DD5}	Execute from Cache;CM4 Active 50 MHz, CM0+ Sleep 25MHz. IMO & FLL. Dhrystone	–	2.4	3.4	mA	V_{DDD}=3.3 V, Buck ON, max at 60 °C
			–	3.7	4.1		V_{DDD} = 1.8V, Buck ON, max at 60 °C
			–	5.1	5.8		V_{DDD} = 1.8 to 3.3 V, LDO, max at 60 °C
SIDC4	I_{DD6}	Execute from Cache;CM4 Active 8 MHz, CM0+ Sleep 8 MHz. IMO. Dhrystone	–	0.90	1.5	mA	V_{DDD} = 3.3 V, Buck ON, max at 60 °C
			–	1.27	1.75		V_{DDD} = 1.8 V, Buck ON, max at 60 °C
			–	1.8	2.6		V_{DDD} = 1.8 to 3.3 V, LDO, max at 60 °C

Table 5. Power Supply Range, CPU Current, and Transition Time Specifications *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
Cortex M0+. Sleep Mode							
SIDS4	I_{DD14}	CM4 Off, CM0+ Sleep 50 MHz. With IMO & FLL.	–	1.3	2	mA	V_{DDD} = 3.3 V, Buck ON, max at 60 °C
			–	1.94	2.4		V_{DDD} = 1.8 V, Buck ON, max at 60 °C
			–	2.57	3.2		V_{DDD} = 1.8 to 3.3 V, LDO, max at 60 °C
SIDS5	I_{DD15}	CM4 Off, CM0+ Sleep 8 MHz. With IMO.	–	0.7	1.3	mA	V_{DDD} = 3.3V, Buck ON, max at 60 °C
			–	0.95	1.5		V_{DDD} = 1.8 V, Buck ON, max at 60 °C
			–	1.25	2		V_{DDD} = 1.8 to 3.3 V, LDO, max at 60 °C
Cortex M4. Low Power Active (LPA) Mode							
SIDLPA1	I_{DD16}	Execute from Flash; CM4 LPA 8 MHz, CM0+ Sleep 8 MHz. With IMO. While (1).	–	0.85	1.5	mA	V_{DDD} = 3.3 V, Buck ON, max at 60 °C
			–	1.18	1.65		V_{DDD} = 1.8 V, Buck ON, max at 60 °C
			–	1.63	2.4		V_{DDD} = 1.8 to 3.3 V, LDO, max at 60 °C
SIDLPA2	I_{DD17}	Execute from Cache; CM4 LPA 8 MHz, CM0+ Sleep 8 MHz. With IMO. Dhrystone.	–	0.90	1.5	mA	V_{DDD} = 3.3 V, Buck ON, max at 60 °C
			–	1.27	1.75		V_{DDD} = 1.8 V, Buck ON, max at 60 °C
			–	1.77	2.5		V_{DDD} = 1.8 to 3.3 V, LDO, max at 60 °C
Cortex M0+. Low Power Active (LPA) Mode							
SIDLPA3	I_{DD18}	Execute from Flash; CM4 Off, CM0+ LPA 8 MHz. With IMO. While (1)	–	0.8	1.4	mA	V_{DDD} = 3.3 V, Buck ON, max at 60 °C
			–	1.14	1.6		V_{DDD} = 1.8 V, Buck ON, max at 60 °C
			–	1.6	2.4		V_{DDD} = 1.8 to 3.3 V, LDO, max at 60 °C
SIDLPA4	I_{DD19}	Execute from Cache; CM4 Off, CM0+ LPA 8 MHz. With IMO. Dhrystone.	–	0.8	1.4	mA	V_{DDD} = 3.3 V, Buck ON, max at 60 °C
			–	1.15	1.65		V_{DDD} = 1.8 V, Buck ON, max at 60 °C
			–	1.62	2.4		V_{DDD} = 1.8 to 3.3 V, LDO, max at 60 °C
Cortex M4. Low Power Sleep (LPS) Mode							
SIDLPS1	I_{DD20}	CM4 LPS 8 MHz, CM0+ LPS 8 MHz. With IMO.	–	0.65	1.1	mA	V_{DDD}=3.3 V, Buck ON, max at 60 °C
			–	0.95	1.5		V_{DDD}=1.8 V, Buck ON, max at 60 °C
			–	1.31	2.1		V_{DDD} = 1.8 to 3.3 V, LDO, max at 60 °C

Table 5. Power Supply Range, CPU Current, and Transition Time Specifications *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SIDDS1_B	I_{DD33A_B}	With internal Buck enabled and 64 KB SRAM retention	–	7	–	µA	Max value is at 60 °C
SIDDS2	I_{DD33B}	With internal Buck enabled and 256 KB SRAM retention	–	9	–	µA	Max value is at 85 °C
SIDDS2_B	I_{DD33B_B}	With internal Buck enabled and 256 KB SRAM retention	–	9	–	µA	Max value is at 60 °C
Hibernate Mode							
SIDHIB1	I_{DD34}	V_{DDD} = 1.8 V	–	300	–	nA	No clocks running
SIDHIB2	I_{DD34A}	V_{DDD} = 3.3 V	–	800	–	nA	No clocks running
Power Mode Transition Times							
SID12	T_{LPACT_ACT}	Low Power Active to Active transition time	–	–	35	µs	Including PLL lock time
SID13[2]	T_{DS_LPACT}	Deep Sleep to LP Active transition time	–	–	25	µs	Guaranteed by design
SID13A[3]	T_{DS_ACT}	Deep Sleep to Active transition time	–	–	25	µs	Guaranteed by design
SID14	T_{HIB_ACT}	Hibernate to Active transition time	–	500	–	µs	Including PLL lock time

XRES

Table 6. XRES

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
XRES (Active Low) Specifications							
XRES AC Specifications							
SID15	T_{XRES_ACT}	POR or XRES release to Active transition time	–	750	–	µs	Normal mode, 50 MHz M0+.
SID16	T_{XRES_PW}	XRES Pulse width	5	–	–	µs	
XRES DC Specifications							
SID17	T_{XRES_IDD}	IDD when XRES asserted	–	300	–	nA	V_{DDD} = 1.8 V
SID17A	$T_{XRES\_IDD\_1}$	IDD when XRES asserted	–	800	–	nA	V_{DDD} = 3.3 V
SID77	V_{IH}	Input Voltage high threshold	0.7 * V_{DD}	–	–	V	CMOS Input
SID78	V_{IL}	Input Voltage low threshold	–	–	0.3 * V_{DD}	V	CMOS Input
SID80	C_{IN}	Input Capacitance	–	3	–	pF	
SID81	$V_{HYSXRES}$	Input voltage hysteresis	–	100	–	mV	
SID82	I_{DIODE}	Current through protection diode to V_{DD}/V_{SS}	–	–	100	µA	

Notes
2. Cypress-supplied software wakeup routines take approximately 100 CPU clock cycles after hardware wakeup (the 25 µs) before transition to Application code. With an 8-MHz CPU clock (LP Active), the time before user code executes is 25 + 12.5 = 37.5 µs.
3. Cypress-supplied software wakeup routines take approximately 100 CPU clock cycles after hardware wakeup (the 25 µs) before transition to Application code. With a 25-MHz CPU clock (FLL), the time before user code executes is 25 + 4 = 29 µs. With a 100-MHz CPU clock, the time is 25 + 1 = 26 µs.

Table 8. Opamp Specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID290	$V_{OS\_DR\_TR}$	Offset voltage drift, trimmed	–10	±3	10	µV/°C	High mode, 0.2 to V_{DDA} – 0.2
SID290A	$V_{OS\_DR\_TR}$	Offset voltage drift, trimmed	–	±10	–	µV/°C	Medium mode
SID290B	$V_{OS\_DR\_TR}$	Offset voltage drift, trimmed	–	±10	–	µV/°C	Low mode
SID291	CMRR	DC Common mode rejection ratio	67	80	–	dB	V_{DDD} = 3.3 V
SID292	PSRR	Power supply rejection ratio at 1 kHz, 10-mV ripple	70	85	–	dB	V_{DDD} = 3.3 V
Noise			–	–	–		–
SID293	VN1	Input-referred, 1 Hz–1 GHz, power = Hi	–	100	–	µVrms	–
SID294	VN2	Input-referred, 1 kHz, power = Hi	–	180	–	nV/rtHz	–
SID295	VN3	Input-referred, 10 kHz, power = Hi	–	70	–	nV/rtHz	–
SID296	VN4	Input-referred, 100 kHz, power = Hi	–	38	–	nV/rtHz	–
SID297	CLOAD	Stable up to max. load. Performance specs at 50 pF.	–	–	125	pF	–
SID298	SLEW_RATE	Output slew rate	6	–	–	V/µs	Cload = 50 pF, Power = High, $V_{DDA} \geq 2.7$ V
SID299	T_OP_WAKE	From disable to enable, no external RC dominating	–	25	–	µs	–
	COMP_MODE	Comparator mode; 50-mV overdrive, Trise = Tfall (approx.)	–		–		–
SID300	T_{PD1}	Response time; power = hi	–	150	–	ns	–
SID301	T_{PD2}	Response time; power = med	–	400	–	ns	–
SID302	T_{PD3}	Response time; power = lo	–	2000	–	ns	–
SID303	V_{HYST_OP}	Hysteresis	–	10	–	mV	–
Deep Sleep Mode		Mode 2 is lowest current range. Mode 1 has higher GBW.					Deep Sleep mode operation: $V_{DDA} \geq 2.7$ V. V_{IN} is 0.2 to V_{DDA} – 1.5 V
SID_DS_1	$I_{DD\_HI\_M1}$	Mode 1, High current	–	1300	1500	µA	Typ at 25 °C
SID_DS_2	$I_{DD\_MED\_M1}$	Mode 1, Medium current	–	460	600	µA	Typ at 25 °C
SID_DS_3	$I_{DD\_LOW\_M1}$	Mode 1, Low current	–	230	350	µA	Typ at 25 °C
SID_DS_4	$I_{DD\_HI\_M2}$	Mode 2, High current	–	120	–	µA	25 °C
SID_DS_5	$I_{DD\_MED\_M2}$	Mode 2, Medium current	–	60	–	µA	25 °C
SID_DS_6	$I_{DD\_LOW\_M2}$	Mode 2, Low current	–	15	–	µA	25 °C
SID_DS_7	GBW_HI_M1	Mode 1, High current	–	4	–	MHz	25 °C
SID_DS_8	GBW_MED_M1	Mode 1, Medium current	–	2	–	MHz	25 °C
SID_DS_9	GBW_LOW_M1	Mode 1, Low current	–	0.5	–	MHz	25 °C
SID_DS_10	GBW_HI_M2	Mode 2, High current	–	0.5	–	MHz	20-pF load, no DC load 0.2 V to V_{DDA} – 1.5 V
SID_DS_11	GBW_MED_M2	Mode 2, Medium current	–	0.2	–	MHz	20-pF load, no DC load 0.2 V to V_{DDA} – 1.5 V

Table 12. 12-bit SAR ADC DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID103	A_INRES	Input resistance	–	–	2.2	kΩ	–
SID104	A_INCAP	Input capacitance	–	–	10	pF	–

Table 13. 12-bit SAR ADC AC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
12-bit SAR ADC AC Specifications							
SID106	A_PSRR	Power supply rejection ratio	70	–	–	dB	
SID107	A_CMRR	Common mode rejection ratio	66	–	–	dB	Measured at 1 V
One Megasample per second mode:							
SID108	A_SAMP_1	Sample rate with external reference bypass cap.	–	–	1	Msps	
SID108A	A_SAMP_2	Sample rate with no bypass cap; Reference = V_{DD}	–	–	250	ksps	
SID108B	A_SAMP_3	Sample rate with no bypass cap. Internal reference.	–	–	100	ksps	
SID109	A_SINAD	Signal-to-noise and Distortion ratio (SINAD). V_{DDA} = 2.7 to 3.6 V, 1 Msps.	64	–	–	dB	Fin = 10 kHz
SID111A	A_INL	Integral Non Linearity. V_{DDA} = 2.7 to 3.6 V, 1 Msps	–2	–	2	LSB	Measured with internal V_{REF} = 1.2 V and bypass cap.
SID111B	A_INL	Integral Non Linearity. V_{DDA} = 2.7 to 3.6 V, 1 Msps	–4	–	4	LSB	Measured with external V_{REF} ≥ 1 V and V_{IN} common mode < 2*Vref
SID112A	A_DNL	Differential Non Linearity. V_{DDA} = 2.7 to 3.6 V, 1 Msps	–1	–	1.4	LSB	Measured with internal V_{REF} = 1.2 V and bypass cap.
SID112B	A_DNL	Differential Non Linearity. V_{DDA} = 2.7 to 3.6 V, 1 Msps	–1	–	1.7	LSB	Measured with external V_{REF} ≥ 1 V and V_{IN} common mode < 2*Vref
SID113	A_THD	Total harmonic distortion. V_{DDA} = 2.7 to 3.6 V, 1 Msps.	–	–	–65	dB	Fin = 10 kHz

Table 14. 12-bit DAC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
12-bit DAC DC Specifications							
SID108D	DAC_RES	DAC resolution	–	–	12	bits	
SID111D	DAC_INL	Integral Non-Linearity	–4	–	4	LSB	
SID112D	DAC_DNL	Differential Non Linearity	–2	–	2	LSB	Monotonic to 11 bits.
SID99D	DAC_OFFSET	Output Voltage zero offset error	–10	–	10	mV	For 000 (hex)
SID103D	DAC_OUT_RES	DAC Output Resistance	–	15	–	kΩ	
SID100D	DAC_IDD	DAC Current	–	–	125	µA	
SID101D	DAC_QIDD	DAC Current when DAC stopped	–	–	1	µA	
12-bit DAC AC Specifications							
SID109D	DAC_CONV	DAC Settling time	–	–	2	µs	Driving through CTBm buffer; 25-pF load
SID110D	DAC_Wakeup	Time from Enabling to ready for conversion	–	–	10	µs	

Table 15. CapSense Sigma-Delta (CSD) Specifications *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SID314A	$I_{DAC1CRT2}$	Output current of IDAC1(7 bits) in medium range	33.7		45.6	µA	LSB = 300-nA typ.
SID314B	$I_{DAC1CRT3}$	Output current of IDAC1(7 bits) in high range	270		365	µA	LSB = 2.4-µA typ.
SID314C	$I_{DAC1CRT12}$	Output current of IDAC1 (7 bits) in low range, 2X mode	8		11.4	µA	LSB = 37.5-nA typ. 2X output stage
SID314D	$I_{DAC1CRT22}$	Output current of IDAC1(7 bits) in medium range, 2X mode	67		91	µA	LSB = 300-nA typ. 2X output stage
SID314E	$I_{DAC1CRT32}$	Output current of IDAC1(7 bits) in high range, 2X mode. V_{DDA} > 2 V	540		730	µA	LSB = 2.4-µA typ.2X output stage
SID315	$I_{DAC2CRT1}$	Output current of IDAC2 (7 bits) in low range	4.2		5.7	µA	LSB = 37.5-nA typ.
SID315A	$I_{DAC2CRT2}$	Output current of IDAC2 (7 bits) in medium range	33.7		45.6	µA	LSB = 300-nA typ.
SID315B	$I_{DAC2CRT3}$	Output current of IDAC2 (7 bits) in high range	270		365	µA	LSB = 2.4-µA typ.
SID315C	$I_{DAC2CRT12}$	Output current of IDAC2 (7 bits) in low range, 2X mode	8		11.4	µA	LSB = 37.5-nA typ. 2X output stage
SID315D	$I_{DAC2CRT22}$	Output current of IDAC2(7 bits) in medium range, 2X mode	67		91	µA	LSB = 300-nA typ. 2X output stage
SID315E	$I_{DAC2CRT32}$	Output current of IDAC2(7 bits) in high range, 2X mode. V_{DDA} > 2V	540		730	µA	LSB = 2.4-µA typ.2X output stage
SID315F	$I_{DAC3CRT13}$	Output current of IDAC in 8-bit mode in low range	8		11.4	µA	LSB = 37.5-nA typ.
SID315G	$I_{DAC3CRT23}$	Output current of IDAC in 8-bit mode in medium range	67		91	µA	LSB = 300-nA typ.
SID315H	$I_{DAC3CRT33}$	Output current of IDAC in 8-bit mode in high range. V_{DDA} > 2V	540		730	µA	LSB = 2.4-µA typ.
SID320	$I_{DACOFFSET}$	All zeroes input	–	–	1	LSB	Polarity set by Source or Sink
SID321	$I_{DACGAIN}$	Full-scale error less offset	–	–	±15	%	LSB = 2.4-µA typ.
SID322	$I_{DACMISMATCH1}$	Mismatch between IDAC1 and IDAC2 in Low mode	–	–	9.2	LSB	LSB = 37.5-nA typ.
SID322A	$I_{DACMISMATCH2}$	Mismatch between IDAC1 and IDAC2 in Medium mode	–	–	6	LSB	LSB = 300-nA typ.
SID322B	$I_{DACMISMATCH3}$	Mismatch between IDAC1 and IDAC2 in High mode	–	–	5.8	LSB	LSB = 2.4-µA typ.
SID323	$I_{DACSET8}$	Settling time to 0.5 LSB for 8-bit IDAC	–	–	10	µs	Full-scale transition. No external load.
SID324	$I_{DACSET7}$	Settling time to 0.5 LSB for 7-bit IDAC	–	–	10	µs	Full-scale transition. No external load.
SID325	CMOD	External modulator capacitor.	–	2.2	–	nF	5-V rating, X7R or NP0 cap.

Table 16. CSD ADC Specifications *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SIDA109A	A_SND_VDDA	Signal-to-noise and Distortion ratio (SINAD)	–	52	–	dB	Measured with 50-Ω source impedance
SIDA111	A_INL_VREF	Integral Non Linearity. 11.6 ksps	–	–	2	LSB	Measured with 50-Ω source impedance
SIDA111A	A_INL_VDDA	Integral Non Linearity. 11.6 ksps	–	–	2	LSB	Measured with 50-Ω source impedance
SIDA112	A_DNL_VREF	Differential Non Linearity. 11.6 ksps	–	–	1	LSB	Measured with 50-Ω source impedance
SIDA112A	A_DNL_VDDA	Differential Non Linearity. 11.6 ksps	–	–	1	LSB	Measured with 50-Ω source impedance

Digital Peripherals

Table 17. Timer/Counter/PWM (TCPWM) Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.TCPWM.1	I_{TCPWM1}	Block current consumption at 8 MHz	–	–	70	µA	All modes (TCPWM)
SID.TCPWM.2	I_{TCPWM2}	Block current consumption at 24 MHz	–	–	180	µA	All modes (TCPWM)
SID.TCPWM.2A	I_{TCPWM3}	Block current consumption at 50 MHz	–	–	270	µA	All modes (TCPWM)
SID.TCPWM.2B	I_{TCPWM4}	Block current consumption at 100 MHz	–	–	540	µA	All modes (TCPWM)
SID.TCPWM.3	$TCPWM_{FREQ}$	Operating frequency	–	–	100	MHz	Fc max = Fcpu Maximum = 100 MHz
SID.TCPWM.4	$TPWM_{ENEXT}$	Input Trigger Pulse Width for all Trigger Events	2 / Fc	–	–	ns	Trigger Events can be Stop, Start, Reload, Count, Capture, or Kill depending on which mode of operation is selected. Fc is counter operating frequency.
SID.TCPWM.5	$TPWM_{EXT}$	Output Trigger Pulse widths	1.5 / Fc	–	–	ns	Minimum possible width of Overflow, Underflow, and CC (Counter equals Compare value) trigger outputs
SID.TCPWM.5A	TC_{RES}	Resolution of Counter	1 / Fc	–	–	ns	Minimum time between successive counts
SID.TCPWM.5B	PWM_{RES}	PWM Resolution	1 / Fc	–	–	ns	Minimum pulse width of PWM Output
SID.TCPWM.5C	Q_{RES}	Quadrature inputs resolution	2 / Fc	–	–	ns	Minimum pulse width between Quadrature phase inputs. Delays from pins should be similar.

SWD Interface

Table 23. SWD and Trace Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SWD and Trace Interface							
SID214	F_SWDCLK2	1.7 V ≤ V_{DDD} ≤ 3.6 V	–	–	25	MHz	LP Mode; V_{CCD} = 1.1 V
SID214L	F_SWDCLK2L	1.7 V ≤ V_{DDD} ≤ 3.6 V	–	–	12	MHz	ULP Mode. V_{CCD} = 0.9 V.
SID215	T_SWDI_SETUP	T = 1/f SWDCLK	0.25 * T	–	–	ns	
SID216	T_SWDI_HOLD	T = 1/f SWDCLK	0.25 * T	–	–	ns	
SID217	T_SWDO_VALID	T = 1/f SWDCLK	–	–	0.5 * T	ns	
SID217A	T_SWDO_HOLD	T = 1/f SWDCLK	1	–	–	ns	
SID214T	F_TRCLK_LP1	With Trace Data setup/hold times of 2/1 ns respectively	–	–	75	MHz	LP Mode. V_{DD} = 1.1 V
SID215T	F_TRCLK_LP2	With Trace Data setup/hold times of 3/2 ns respectively	–	–	70	MHz	LP Mode. V_{DD} = 1.1 V
SID216T	F_TRCLK_ULP	With Trace Data setup/hold times of 3/2 ns respectively	–	–	25	MHz	ULP Mode. V_{DD} = 0.9 V

Internal Main Oscillator

Table 24. IMO DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID218	I_{IMO1}	IMO operating current at 8 MHz	–	9	15	µA	–

Table 25. IMO AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID223	$F_{IMOTOL1}$	Frequency variation centered on 8 MHz	–	–	±2	%	–
SID227	T_{JITR}	Cycle-to-Cycle and Period jitter	–	±250	–	ps	–

Internal Low-Speed Oscillator

Table 26. ILO DC Specification

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID231	I_{ILO2}	ILO operating current at 32 kHz	–	0.3	0.7	µA	–

Table 27. ILO AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID234	$T_{STARTILO1}$	ILO startup time	–	–	7	µs	Startup time to 95% of final frequency
SID236	$T_{LIODUTY}$	ILO Duty cycle	45	50	55	%	–
SID237	$F_{ILOTRIM1}$	32-kHz trimmed frequency	28.8	32	35.2	kHz	±10% variation

Table 34. USB Specifications (USB requires LP Mode 1.1-V Internal Supply)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
USB Block Specifications							
SID322U	Vusb_3.3	Device supply for USB operation	3.15	–	3.6	V	USB Configured, USB Reg. bypassed
SID323U	Vusb_3.3	Device supply for USB operation (functional operation only)	2.85	–	3.6	V	USB Configured, USB Reg. bypassed
SID325U	Iusb_config	Device supply current in Active mode	–	8	–	mA	V_{DDD} = 3.3 V
SID328	Isub_suspend	Device supply current in Sleep mode	–	0.5	–	mA	V_{DDD} = 3.3 V, PICU wakeup
SID329	Isub_suspend	Device supply current in Sleep mode	–	0.3	–	mA	V_{DDD} = 3.3 V, Device disconnected
SID330U	USB_Drive_Res	USB driver impedance	28	–	44	Ω	Series resistors are on chip
SID331U	USB_Pulldown	USB pull-down resistors in Host mode	14.25	–	24.8	kΩ	–
SID332U	USB_Pullup_Idle	Idle mode range	900	–	1575	Ω	Bus idle
SID333U	USB_Pullup	Active mode	1425	–	3090	Ω	Upstream device transmitting

Table 35. QSPI Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SMIF QSPI Specifications. All specs with 15-pF load.							
SID390Q	Fsmifclock	SMIF QSPI output clock frequency	–	–	80	MHz	LP mode (1.1 V)
SID390QU	Fsmifclocku	SMIF QSPI output clock frequency	–	–	50	MHz	ULP mode (0.9 V). Guaranteed by Char.
SID397Q	Idd_qspi	Block current in LP mode (1.1 V)	–	–	1900	µA	LP mode (1.1 V)
SID398Q	Idd_qspi_u	Block current in ULP mode (0.9 V)	–	–	590	µA	ULP mode (0.9 V)
SID391Q	Tsetup	Input data set-up time with respect to clock capturing edge	4.5	–	–	ns	
SID392Q	Tdatahold	Input data hold time with respect to clock capturing edge	0	–	–	ns	
SID393Q	Tdataoutvalid	Output data valid time with respect to clock falling edge	–	–	3.7	ns	
SID394Q	Tholdtime	Output data hold time with respect to clock rising edge	3	–	–	ns	
SID395Q	Tseloutvalid	Output Select valid time with respect to clock rising edge	–	–	7.5	ns	
SID396Q	Tselouthold	Output Select hold time with respect to clock rising edge	Tsclk	–	–	ns	Tsclk = Fsmifclk cycle time

Table 38. BLE Subsystem Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
BLE Subsystem specifications							
RF Receiver Specifications (1 Mbps)							
SID317R	RXS,IDLE	RX Sensitivity with Ideal Transmitter	–	–95	–	dBm	Across RF Operating Frequency Range
SID317RR	RXS,IDLE	RX Sensitivity with Ideal Transmitter	–	–93	–	dBm	255-byte packet length, across Frequency Range
SID318R	RXS,DIRTY	RX Sensitivity with Dirty Transmitter	–	–92	–	dBm	RF-PHY Specification (RCV-LE/CA/01/C)
SID319R	PRXMAX	Maximum received signal strength at < 0.1% PER	–	0	–	dBm	RF-PHY Specification (RCV-LE/CA/06/C)
SID320R	CI1	Co-channel interference, Wanted Signal at –67 dBm and Interferer at FRX	–	9	21	dB	RF-PHY Specification (RCV-LE/CA/03/C)
SID321R	CI2	Adjacent channel interference Wanted Signal at –67 dBm and Interferer at FRX ± 1 MHz	–	3	15	dB	RF-PHY Specification (RCV-LE/CA/03/C)
SID322R	CI3	Adjacent channel interference Wanted Signal at –67 dBm and Interferer at FRX ± 2 MHz	–	–26	–17	dB	RF-PHY Specification (RCV-LE/CA/03/C)
SID323R	CI4	Adjacent channel interference Wanted Signal at –67 dBm and Interferer at ≥ FRX ± 3 MHz	–	–33	–27	dB	RF-PHY Specification (RCV-LE/CA/03/C)
SID324R	CI5	Adjacent channel interference Wanted Signal at –67 dBm and Interferer at Image frequency (FIMAGE)	–	–20	–9	dB	RF-PHY Specification (RCV-LE/CA/03/C)
SID325R	CI6	Adjacent channel interference Wanted Signal at –67 dBm and Interferer at Image frequency (FIMAGE ± 1 MHz)	–	–28	–15	dB	RF-PHY Specification (RCV-LE/CA/03/C)
RF Receiver Specifications (2 Mbps)							
SID326	RXS,IDLE	RX Sensitivity with Ideal Transmitter	–	–92	–	dBm	Across RF Operating Frequency Range
SID326R	RXS,IDLE	RX Sensitivity with Ideal Transmitter	–	–90	–	dBm	255-byte packet length, across Frequency Range
SID327	RXS,DIRTY	RX Sensitivity with Dirty Transmitter	–	–89	–	dBm	RF-PHY Specification (RCV-LE/CA/01/C)
SID328R	PRXMAX	Maximum received signal strength at < 0.1% PER	–	0	–	dBm	RF-PHY Specification (RCV-LE/CA/06/C)
SID329R	CI1	Co-channel interference, Wanted Signal at –67 dBm and Interferer at FRX	–	9	21	dB	RF-PHY Specification (RCV-LE/CA/03/C)
SID330	CI2	Adjacent channel interference Wanted Signal at –67 dBm and Interferer at FRX ± 2 MHz	–	3	15	dB	RF-PHY Specification (RCV-LE/CA/03/C)
SID331	CI3	Adjacent channel interference Wanted Signal at –67 dBm and Interferer at FRX ± 4 MHz	–	–26	–17	dB	RF-PHY Specification (RCV-LE/CA/03/C)

Ordering Information

Table 41 lists the PSoC 63 part numbers and features. The following table shows Marketing Part Numbers (MPNs) for products including the BLE Radio. The packages are 104 M CSP and 116 BGA.

Table 41. BLE Series Part Numbers

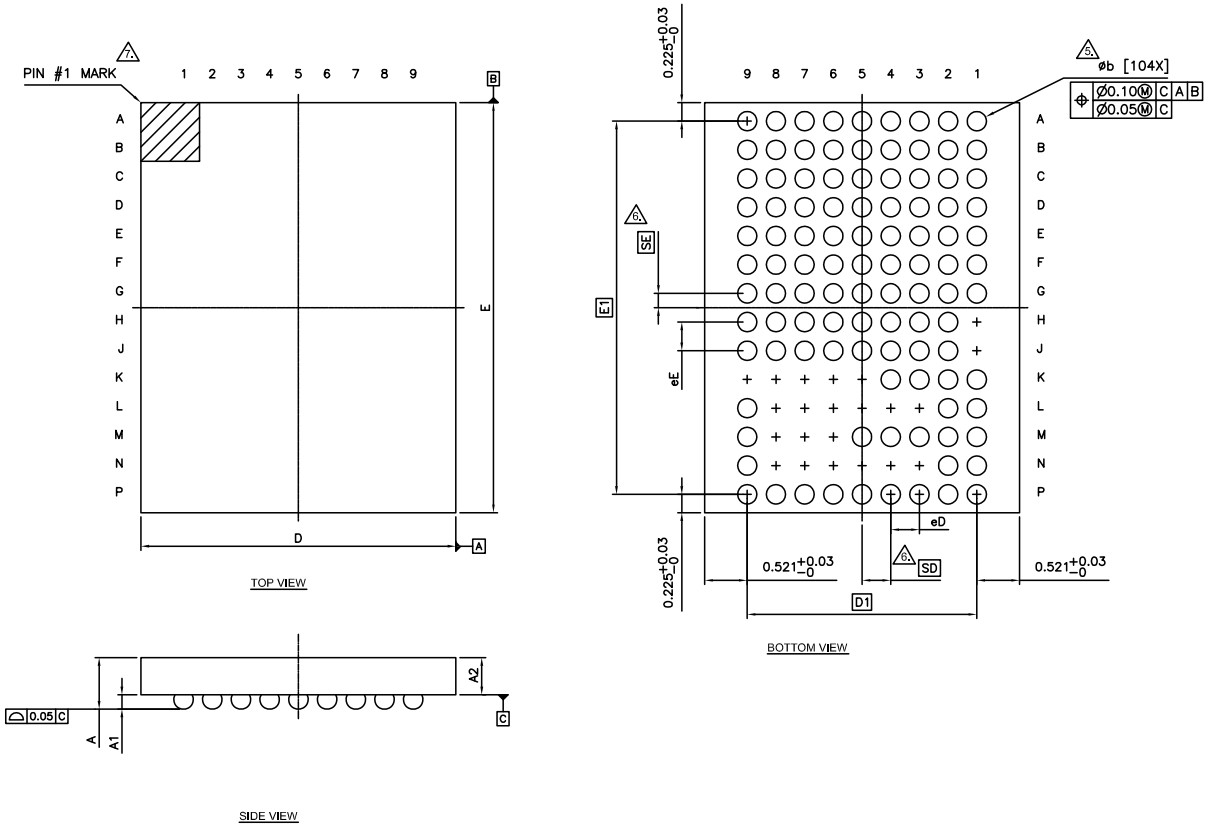
Family	MPN	CPU Speed (M4)	CPU Speed (M0+)	Single core/Dual core	ULP/LP	Flash	SRAM	No. of CTBMs	No. of UDBs	CapSense	GPIOs	CRYPTO	Package
63	CY8C6336BZI-BLF03	150	–	Single	LP	512	128	0	0	No	78	No	116-BGA
	CY8C6316BZI-BLF03	50	–	Single	ULP	512	128	0	0	No	78	No	116-BGA
	CY8C6316BZI-BLF53	50	–	Single	ULP	512	128	1	12	Yes	78	Yes	116-BGA
	CY8C6337BZI-BLF13	150	–	Single	LP	1024	288	0	0	Yes	78	No	116-BGA
	CY8C6336BZI-BLD13	150	100	Double	LP	512	128	0	0	Yes	78	No	116-BGA
	CY8C6347BZI-BLD43	150/50	100/25	Double	FLEX	1024	288	0	0	Yes	78	Yes	116-BGA
	CY8C6347BZI-BLD33	150/50	100/25	Double	FLEX	1024	288	1	12	Yes	78	No	116-BGA
	CY8C6347BZI-BLD53	150/50	100/25	Double	FLEX	1024	288	1	12	Yes	78	Yes	116-BGA
	CY8C6347FMI-BLD13	150/50	100/25	Double	FLEX	1024	288	0	0	Yes	70	No	104-MCSP
	CY8C6347FMI-BLD43	150/50	100/25	Double	FLEX	1024	288	0	0	Yes	70	Yes	104-MCSP
	CY8C6347FMI-BLD33	150/50	100/25	Double	FLEX	1024	288	1	12	Yes	70	No	104-MCSP
	CY8C6347FMI-BLD53	150/50	100/25	Double	FLEX	1024	288	1	12	Yes	70	Yes	104-MCSP

Table 42 lists the field values.

Table 42. MPN Nomenclature

Field	Description	Values	Meaning
CY8C	Cypress Prefix		
6	Architecture	6	PSoC 6
A	Family	0	Value
		1	Programmable
		2	Performance
		3	Connectivity
B	Speed	1	50 MHz
		2	100 MHz
		3	150 MHz
		4	150/50 MHz
C	Flash Capacity	4	128 KB
		5	256 KB
		6	512 KB
		7	1024 KB

Figure 4. 104-WLCSP 3.8 × 5.0 × 0.65 mm



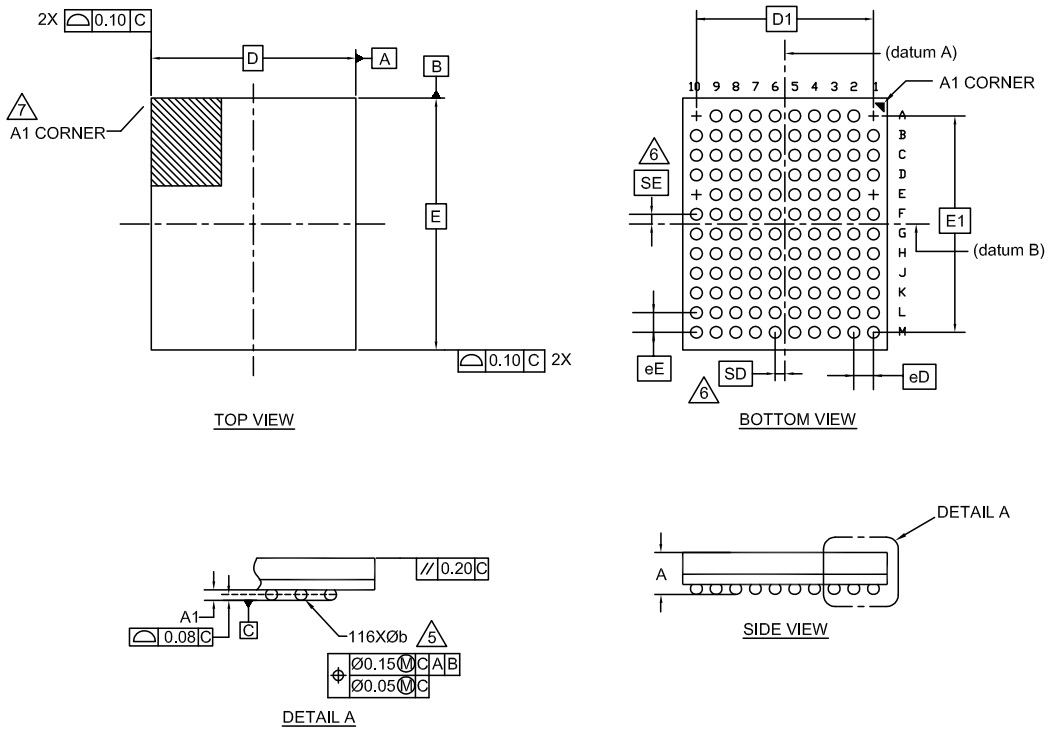
SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	0.560	0.605	0.650
A1	0.165	0.185	0.205
A2	0.395	0.420	0.445
D	3.791	3.841	3.891
E	4.95	5.00	5.05
D1	2.80 BSC		
E1	4.55 BSC		
MD	9		
ME	14		
N	104		
Ø b	0.205	0.235	0.265
eD	0.335	0.350	0.365
eE	0.335	0.350	0.365
SD	0.35 BSC		
SE	0.175 BSC		

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. SOLDER BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.
3. "e" REPRESENTS THE SOLDER BALL GRID PITCH.
4. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
   N IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
5. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
6. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" OR "SE" = 0.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
7. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK METALIZED MARK, INDENTATION OR OTHER MEANS.
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED SOLDER BALLS.
9. JEDEC SPECIFICATION NO. REF. : N/A.

002-16508 *D

Figure 5. 116-BGA 5.2 × 6.4 × 0.70 mm



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	-	-	0.70
A1	0.16	0.21	0.26
D	5.20 BSC		
E	6.40 BSC		
D1	4.50 BSC		
E1	5.50 BSC		
MD	10		
ME	12		
N	116		
Ø b	0.25	0.30	0.35
eD	0.50 BSC		
eE	0.50 BSC		
SD	0.25 BSC		
SE	0.25 BSC		

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. SOLDER BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.
3. "e" REPRESENTS THE SOLDER BALL GRID PITCH.
4. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
   N IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
5. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
6. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW "SD" OR "SE" = 0.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
7. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK METALIZED MARK, INDENTATION OR OTHER MEANS.
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED SOLDER BALLS.
9. JEDEC SPECIFICATION NO. REF: N/A

002-16574 *B