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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Not For New Designs
Core Processor	CIP-51 8051
Core Size	8-Bit
Speed	50MHz
Connectivity	I ² C, SMBus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	20
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2.25К х 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 12x10/12b SAR; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	32-WFQFN Exposed Pad
Supplier Device Package	32-QFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm8bb31f16a-b-4qfn24

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

1. Feature List

The EFM8BB3 device family are fully integrated, mixed-signal system-on-a-chip MCUs. Highlighted features are listed below.

- Core:
 - Pipelined CIP-51 Core
 - · Fully compatible with standard 8051 instruction set
 - 70% of instructions execute in 1-2 clock cycles
 - 50 MHz maximum operating frequency
- Memory:
 - Up to 64 kB flash memory (63 kB user-accessible), in-system re-programmable from firmware in 512-byte sectors
 - Up to 4352 bytes RAM (including 256 bytes standard 8051 RAM and 4096 bytes on-chip XRAM)
- · Power:
 - Internal LDO regulator for CPU core voltage
 - · Power-on reset circuit and brownout detectors
- I/O: Up to 29 total multifunction I/O pins:
 - Up to 25 pins 5 V tolerant under bias
 - Selectable state retention through reset events
 - · Flexible peripheral crossbar for peripheral routing
 - 5 mA source, 12.5 mA sink allows direct drive of LEDs
- · Clock Sources:
 - Internal 49 MHz oscillator with accuracy of ±2%
 - Internal 24.5 MHz oscillator with ±2% accuracy
 - · Internal 80 kHz low-frequency oscillator
 - External CMOS clock option
 - External crystal/RC Oscillator (up to 25 MHz)

- Analog:
 - 12/10-Bit Analog-to-Digital Converter (ADC)
 - Internal temperature sensor
 - 4 x 12-Bit Digital-to-Analog Converters (DAC)
 - 2 x Low-current analog comparators with adjustable reference
- · Communications and Digital Peripherals:
 - 2 x UART, up to 3 Mbaud
 - SPI™ Master / Slave, up to 12 Mbps
 - SMBus™/I2C™ Master / Slave, up to 400 kbps
 - I²C High-Speed Slave, up to 3.4 Mbps
 - 16-bit CRC unit, supporting automatic CRC of flash at 256byte boundaries
 - 4 Configurable Logic Units
- · Timers/Counters and PWM:
 - 6-channel programmable counter array (PCA) supporting PWM, capture/compare, and frequency output modes
 - 6 x 16-bit general-purpose timers
 - Independent watchdog timer, clocked from the low frequency oscillator
- On-Chip, Non-Intrusive Debugging
 - · Full memory and register inspection
 - · Four hardware breakpoints, single-stepping
- · Pre-programmed UART bootloader
- Temperature range -40 to 85 °C or -40 to 125 °C

With on-chip power-on reset, voltage supply monitor, watchdog timer, and clock oscillator, the EFM8BB3 devices are truly standalone system-on-a-chip solutions. The flash memory is reprogrammable in-circuit, providing nonvolatile data storage and allowing field upgrades of the firmware. The on-chip debugging interface (C2) allows non-intrusive (uses no on-chip resources), full speed, in-circuit debugging using the production MCU installed in the final application. This debug logic supports inspection and modification of memory and registers, setting breakpoints, single stepping, and run and halt commands. All analog and digital peripherals are fully functional while debugging. Device operation is specified from 2.2 V up to a 3.6 V supply. Devices are AEC-Q100 qualified and available in 4x4 mm 32-pin QFN, 3x3 mm 24-pin QFN, 32-pin QFP, or 24-pin QSOP packages. All package options are lead-free and RoHS compliant.

Universal Asynchronous Receiver/Transmitter (UART1)

UART1 is an asynchronous, full duplex serial port offering a variety of data formatting options. A dedicated baud rate generator with a 16-bit timer and selectable prescaler is included, which can generate a wide range of baud rates. A received data FIFO allows UART1 to receive multiple bytes before data is lost and an overflow occurs.

UART1 provides the following features:

- · Asynchronous transmissions and receptions
- Dedicated baud rate generator supports baud rates up to SYSCLK/2 (transmit) or SYSCLK/8 (receive)
- 5, 6, 7, 8, or 9 bit data
- Automatic start and stop generation
- Automatic parity generation and checking
- · Single-byte buffer on transmit and receive
- Auto-baud detection
- · LIN break and sync field detection
- CTS / RTS hardware flow control

Serial Peripheral Interface (SPI0)

The serial peripheral interface (SPI) module provides access to a flexible, full-duplex synchronous serial bus. The SPI can operate as a master or slave device in both 3-wire or 4-wire modes, and supports multiple masters and slaves on a single SPI bus. The slave-select (NSS) signal can be configured as an input to select the SPI in slave mode, or to disable master mode operation in a multi-master environment, avoiding contention on the SPI bus when more than one master attempts simultaneous data transfers. NSS can also be configured as a firmware-controlled chip-select output in master mode, or disable to reduce the number of pins required. Additional general purpose port I/O pins can be used to select multiple slave devices in master mode.

- Supports 3- or 4-wire master or slave modes
- · Supports external clock frequencies up to 12 Mbps in master or slave mode
- · Support for all clock phase and polarity modes
- 8-bit programmable clock rate (master)
- Programmable receive timeout (slave)
- · Two byte FIFO on transmit and receive
- · Can operate in suspend or snooze modes and wake the CPU on reception of a byte
- · Support for multiple masters on the same data lines

System Management Bus / I2C (SMB0)

The SMBus I/O interface is a two-wire, bi-directional serial bus. The SMBus is compliant with the System Management Bus Specification, version 1.1, and compatible with the I²C serial bus.

The SMBus module includes the following features:

- · Standard (up to 100 kbps) and Fast (400 kbps) transfer speeds
- · Support for master, slave, and multi-master modes
- Hardware synchronization and arbitration for multi-master mode
- · Clock low extending (clock stretching) to interface with faster masters
- · Hardware support for 7-bit slave and general call address recognition
- Firmware support for 10-bit slave address decoding
- · Ability to inhibit all slave states
- Programmable data setup/hold times
- · Transmit and receive FIFOs (one byte) to help increase throughput in faster applications

I2C Slave (I2CSLAVE0)

The I2C Slave interface is a 2-wire, bidirectional serial bus that is compatible with the I2C Bus Specification 3.0. It is capable of transferring in high-speed mode (HS-mode) at speeds of up to 3.4 Mbps. Firmware can write to the I2C interface, and the I2C interface can autonomously control the serial transfer of data. The interface also supports clock stretching for cases where the core may be temporarily prohibited from transmitting a byte or processing a received byte during an I2C transaction. This module operates only as an I2C slave device.

The I2C module includes the following features:

- Standard (up to 100 kbps), Fast (400 kbps), Fast Plus (1 Mbps), and High-speed (3.4 Mbps) transfer speeds
- · Support for slave mode only
- · Clock low extending (clock stretching) to interface with faster masters
- · Hardware support for 7-bit slave address recognition
- Transmit and receive FIFOs (two byte) to help increase throughput in faster applications
- · Hardware support for multiple slave addresses with the option to save the matching address in the receive FIFO

16-bit CRC (CRC0)

The cyclic redundancy check (CRC) module performs a CRC using a 16-bit polynomial. CRC0 accepts a stream of 8-bit data and posts the 16-bit result to an internal register. In addition to using the CRC block for data manipulation, hardware can automatically CRC the flash contents of the device.

The CRC module is designed to provide hardware calculations for flash memory verification and communications protocols. The CRC module supports the standard CCITT-16 16-bit polynomial (0x1021), and includes the following features:

- Support for CCITT-16 polynomial
- Byte-level bit reversal
- · Automatic CRC of flash contents on one or more 256-byte blocks
- · Initial seed selection of 0x0000 or 0xFFFF

Configurable Logic Units (CLU0, CLU1, CLU2, and CLU3)

The Configurable Logic block consists of multiple Configurable Logic Units (CLUs). CLUs are flexible logic functions which may be used for a variety of digital functions, such as replacing system glue logic, aiding in the generation of special waveforms, or synchronizing system event triggers.

- · Four configurable logic units (CLUs), with direct-pin and internal logic connections
- Each unit supports 256 different combinatorial logic functions (AND, OR, XOR, muxing, etc.) and includes a clocked flip-flop for synchronous operations
- · Units may be operated synchronously or asynchronously
- · May be cascaded together to perform more complicated logic functions
- · Can operate in conjunction with serial peripherals such as UART and SPI or timing peripherals such as timers and PCA channels
- · Can be used to synchronize and trigger multiple on-chip resources (ADC, DAC, Timers, etc.)
- · Asynchronous output may be used to wake from low-power states

3.10 Bootloader

All devices come pre-programmed with a UART0 bootloader. This bootloader resides in the code security page, which is the last page of code flash; it can be erased if it is not needed.

The byte before the Lock Byte is the Bootloader Signature Byte. Setting this byte to a value of 0xA5 indicates the presence of the bootloader in the system. Any other value in this location indicates that the bootloader is not present in flash.

When a bootloader is present, the device will jump to the bootloader vector after any reset, allowing the bootloader to run. The bootloader then determines if the device should stay in bootload mode or jump to the reset vector located at 0x0000. When the bootloader is not present, the device will jump to the reset vector of 0x0000 after any reset.

More information about the bootloader protocol and usage can be found in *AN945: EFM8 Factory Bootloader User Guide*. Application notes can be found on the Silicon Labs website (www.silabs.com/8bit-appnotes) or within Simplicity Studio by using the [Application Notes] tile.



Figure 3.2. Flash Memory Map with Bootloader - 62.5 KB Devices

Bootloader	Pins for Bootload Communication
UART	TX – P0.4
	RX – P0.5

Device Package	Pin for Bootload Mode Entry
QFN32	P3.7 / C2D
QFP32	P3.7 / C2D
QFN24	P3.0 / C2D
QSOP24	P3.0 / C2D

Table 3.3. Summary of Pins for Bootload Mode Entry

4.1.4 Flash Memory

Parameter	Symbol	Test Condition	Min	Тур	Max	Units
Write Time ^{1,2}	t _{WRITE}	One Byte,	19	20	21	μs
		F _{SYSCLK} = 24.5 MHz				
Erase Time ^{1,2}	t _{ERASE}	One Page,	5.2	5.35	5.5	ms
		F _{SYSCLK} = 24.5 MHz				
V _{DD} Voltage During Programming ³ V _{PROG}			2.2	_	3.6	V
Endurance (Write/Erase Cycles) N _{WE}			20k	100k	—	Cycles
CRC Calculation Time	t _{CRC}	One 256-Byte Block	_	5.5	_	μs
		SYSCLK = 49 MHz				

Table 4.4. Flash Memory

Note:

1. Does not include sequencing time before and after the write/erase operation, which may be multiple SYSCLK cycles.

2. The internal High-Frequency Oscillator 0 has a programmable output frequency, which is factory programmed to 24.5 MHz. If user firmware adjusts the oscillator speed, it must be between 22 and 25 MHz during any flash write or erase operation. It is recommended to write the HFO0CAL register back to its reset value when writing or erasing flash.

3. Flash can be safely programmed at any voltage above the supply monitor threshold (V_{VDDM}).

4. Data Retention Information is published in the Quarterly Quality and Reliability Report.

4.1.5 Power Management Timing

Table 4.5. Power Management Timing

Parameter	Symbol	Test Condition	Min	Тур	Мах	Units
Idle Mode Wake-up Time	t _{IDLEWK}		2		3	SYSCLKs
Suspend Mode Wake-up Time	t _{SUS-}	SYSCLK = HFOSC0	_	170	_	ns
	PENDWK	CLKDIV = 0x00				
Snooze Mode Wake-up Time	t _{SLEEPWK}	SYSCLK = HFOSC0	—	12	—	μs
		CLKDIV = 0x00				

4.3 Absolute Maximum Ratings

Stresses above those listed in Table 4.19 Absolute Maximum Ratings on page 32 may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. For more information on the available quality and reliability data, see the Quality and Reliability Monitor Report at http://www.silabs.com/support/quality/pages/default.aspx.

Table 4.19. Absolute Maximum Ratings

Parameter	Symbol	Test Condition	Min	Max	Unit
Ambient Temperature Under Bias	T _{BIAS}		-55	125	°C
Storage Temperature	T _{STG}		-65	150	°C
Voltage on VDD	V _{DD}		GND-0.3	4.2	V
Voltage on VIO ²	V _{IO}		GND-0.3	V _{DD} +0.3	V
Voltage on I/O pins or RSTb, excluding	V _{IN}	V _{IO} > 3.3 V	GND-0.3	5.8	V
P3.0-P3.3 (QFN32 and QSOP24) of P3.0-P3.3 (QFN32 and QFP32)		V _{IO} < 3.3 V	GND-0.3	V _{IO} +2.5	V
Voltage on P2.0-P2.3 (QFN24 and QSOP24) or P3.0-P3.3 (QFN32 and QFP32)	V _{IN}		GND-0.3	V _{DD} +0.3	V
Total Current Sunk into Supply Pin	I _{VDD}		—	200	mA
Total Current Sourced out of Ground Pin	I _{GND}		200	_	mA
Current Sourced or Sunk by any I/O Pin or RSTb	I _{IO}		-100	100	mA
Operating Junction Temperature	TJ	T _A = -40 °C to 85 °C	-40	105	°C
		T _A = -40 °C to 125 °C (I-grade parts only)	-40	130	°C

Note:

1. Exposure to maximum rating conditions for extended periods may affect device reliability.

2. In certain package configurations, the VIO and VDD supplies are bonded to the same pin.

5.2 Debug

The diagram below shows a typical connection diagram for the debug connections pins. The pin sharing resistors are only required if the functionality on the C2D (a GPIO pin) and the C2CK (RSTb) is routed to external circuitry. For example, if the RSTb pin is connected to an external switch with debouncing filter or if the GPIO sharing with the C2D pin is connected to an external circuit, the pin sharing resistors and connections to the debug adapter must be placed on the hardware. Otherwise, these components and connections can be omitted.

For more information on debug connections, see the example schematics and information available in AN127: "Pin Sharing Techniques for the C2 Interface." Application notes can be found on the Silicon Labs website (http://www.silabs.com/8bit-appnotes) or in Simplicity Studio.



Figure 5.2. Debug Connection Diagram

5.3 Other Connections

Other components or connections may be required to meet the system-level requirements. Application Note AN203: "8-bit MCU Printed Circuit Board Design Notes" contains detailed information on these connections. Application Notes can be accessed on the Silicon Labs website (www.silabs.com/8bit-appnotes).



Figure 6.2. EFM8BB3x-QFP32 Pinout

Table 6.2.	Pin Definitions	for EFM8BB3x-QFP32
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Pin	Pin Name	Description	Crossbar Capability	Additional Digital	Analog Functions
Number				Functions	
1	P0.0	Multifunction I/O	Yes	P0MAT.0	VREF
				INT0.0	
				INT1.0	
				CLU0A.8	
				CLU2A.8	
				CLU3B.8	
2	GND	Ground			
3	VIO	I/O Supply Power Input			
4	VDD	Supply Power Input			
5	RSTb /	Active-low Reset /			
	С2СК	C2 Debug Clock			

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
30	P0.3	Multifunction I/O	Yes	P0MAT.3	XTAL2
				EXTCLK	
				INT0.3	
				INT1.3	
				CLU0B.9	
				CLU2B.9	
				CLU3A.9	
31	P0.2	Multifunction I/O	Yes	P0MAT.2	XTAL1
				INT0.2	ADC0.1
				INT1.2	CMP0P.1
				CLU0OUT	CMP0N.1
				CLU0A.9	
				CLU2B.8	
				CLU3A.8	
32	P0.1	Multifunction I/O	Yes	P0MAT.1	ADC0.0
				INT0.1	CMP0P.0
				INT1.1	CMP0N.0
				CLU0B.8	AGND
				CLU2A.9	
				CLU3B.9	

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
2	P0.0	Multifunction I/O	Yes	P0MAT.0	VREF
				INT0.0	
				INT1.0	
				CLU0A.8	
				CLU2A.8	
				CLU3B.8	
3	GND	Ground			
4	VDD / VIO	Supply Power Input			
5	RSTb /	Active-low Reset /			
	C2CK	C2 Debug Clock			
6	P3.0 /	Multifunction I/O /			
	C2D	C2 Debug Data			
7	P2.3	Multifunction I/O	Yes	P2MAT.3	DAC3
				CLU1B.15	
				CLU2B.15	
				CLU3A.15	
8	P2.2	Multifunction I/O	Yes	P2MAT.2	DAC2
				CLU1A.15	
				CLU2B.14	
				CLU3A.14	
9	P2.1	Multifunction I/O	Yes	P2MAT.1	DAC1
				CLU1B.14	
				CLU2A.15	
				CLU3B.15	
10	P2.0	Multifunction I/O	Yes	P2MAT.0	DAC0
				CLU1A.14	
				CLU2A.14	
				CLU3B.14	
11	P1.6	Multifunction I/O	Yes	P1MAT.6	ADC0.11
				CLU3OUT	CMP1P.5
				CLU0A.15	CMP1N.5
				CLU1B.12	
				CLU2A.12	

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
12	P1.5	Multifunction I/O	Yes	P1MAT.5	ADC0.10
				CLU2OUT	CMP1P.4
				CLU0B.14	CMP1N.4
				CLU1A.13	
				CLU2B.13	
13	P1.4	Multifunction I/O	Yes	P1MAT.4	ADC0.9
				I2C0_SCL	CMP1P.3
				CLU0A.14	CMP1N.3
				CLU1A.12	
				CLU2B.12	
14	P1.3	Multifunction I/O	Yes	P1MAT.3	CMP1P.2
				I2C0_SDA	CMP1N.2
				CLU0B.13	
				CLU1B.11	
				CLU2B.11	
				CLU3A.13	
15	GND	Ground			
16	P1.2	Multifunction I/O	Yes	P1MAT.2	ADC0.8
				CLU0A.13	
				CLU1A.11	
				CLU2B.10	
				CLU3A.12	
17	P1.1	Multifunction I/O	Yes	P1MAT.1	ADC0.7
				CLU0B.12	
				CLU1B.10	
				CLU2A.11	
				CLU3B.13	
18	P1.0	Multifunction I/O	Yes	P1MAT.0	ADC0.6
				CLU0A.12	
				CLU1A.10	
				CLU2A.10	
				CLU3B.12	



Figure 6.4. EFM8BB3x-QSOP24 Pinout

TADIE 0.4. FIII DEIIIIIUUIIS IUI EFINIODD3X-Q30F2	Table 6.4.	Pin Definitions	for EFM8BB3x	-QSOP24
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Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
1	P0.3	Multifunction I/O	Yes	P0MAT.3	XTAL2
				EXTCLK	
				INT0.3	
				INT1.3	
				CLU0B.9	
				CLU2B.9	
				CLU3A.9	

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
11	P2.1	Multifunction I/O	Yes	P2MAT.1	DAC1
				CLU1B.14	
				CLU2A.15	
				CLU3B.15	
12	P2.0	Multifunction I/O	Yes	P2MAT.0	DAC0
				CLU1A.14	
				CLU2A.14	
				CLU3B.14	
13	P1.7	Multifunction I/O	Yes	P1MAT.7	ADC0.12
				CLU0B.15	CMP1P.6
				CLU1B.13	CMP1N.6
				CLU2A.13	
14	P1.6	Multifunction I/O	Yes	P1MAT.6	ADC0.11
				CLU3OUT	CMP1P.5
				CLU0A.15	CMP1N.5
				CLU1B.12	
				CLU2A.12	
15	P1.5	Multifunction I/O	Yes	P1MAT.5	ADC0.10
				CLU2OUT	CMP1P.4
				CLU0B.14	CMP1N.4
				CLU1A.13	
				CLU2B.13	
16	P1.4	Multifunction I/O	Yes	P1MAT.4	ADC0.9
				I2C0_SCL	CMP1P.3
				CLU0A.14	CMP1N.3
				CLU1A.12	
				CLU2B.12	
17	P1.3	Multifunction I/O	Yes	P1MAT.3	CMP1P.2
				I2C0_SDA	CMP1N.2
				CLU0B.13	
				CLU1B.11	
				CLU2B.11	
				CLU3A.13	

Dimension	Min	Мах			
Note:					
1. All dimensions shown are in millimeters	(mm) unless otherwise noted.				
2. Dimensioning and Tolerancing is per the	2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.				
3. This Land Pattern Design is based on the IPC-7351 guidelines.					
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabri- cation Allowance of 0.05mm.					
5. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.					
6. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.					
7. The stencil thickness should be 0.125 mm (5 mils).					
8. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.					
9. A 2 x 2 array of 1.10 mm square openings on a 1.30 mm pitch should be used for the center pad.					

- 10. A No-Clean, Type-3 solder paste is recommended.
- 11. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

7.3 QFN32 Package Marking



Figure 7.3. QFN32 Package Marking

The package marking consists of:

- PPPPPPP The part number designation.
- TTTTTT A trace or manufacturing code.
- YY The last 2 digits of the assembly year.
- WW The 2-digit workweek when the device was assembled.
- # The device revision (A, B, etc.).

Dimension	Min	Тур	Мах
ааа	0.20		
bbb	0.20		
ссс	0.10		
ddd	0.20		
theta	0°	3.5°	7°
Note:			

1. All dimensions shown are in millimeters (mm) unless otherwise noted.

2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.

3. This drawing conforms to JEDEC outline MS-026.

4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

8.2 QFP32 PCB Land Pattern



Figure 8.2. QFP32 PCB Land Pattern Drawing

Table 8.2.	QFP32 PCB	Land Pattern	Dimensions
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Dimension	Min	Мах	
C1	8.40	8.50	
C2	8.40	8.50	
E	0.80 BSC		
X1	0.55		
Y1	1.5		

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.

2. This Land Pattern Design is based on the IPC-7351 guidelines.

3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.

5. The stencil thickness should be 0.125 mm (5 mils).

6. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.

7. A No-Clean, Type-3 solder paste is recommended.

8. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

10. QSOP24 Package Specifications

10.1 QSOP24 Package Dimensions



Figure 10.1. QSOP24 Package Drawing

Table 10.1. QSOP24 Package Dimensions

Dimension	Min	Тур	Мах
A	_	—	1.75
A1	0.10	—	0.25
b	0.20	—	0.30
с	0.10	—	0.25
D	8.65 BSC		
E	6.00 BSC		
E1	3.90 BSC		
е	0.635 BSC		
L	0.40 — 1.27		
theta	0°	—	8°

Min	Тур	Мах
	0.20	
0.18		
	0.10	
	0.10	
	Min	Min Typ 0.20 0.18 0.10 0.10

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.

2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.

3. This drawing conforms to JEDEC outline MO-137, variation AE.

4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

10.2 QSOP24 PCB Land Pattern



Figure 10.2. QSOP24 PCB Land Pattern Drawing

Table 10.2. QSOP24 PCB Land Pattern Dimension

Dimension	Min	Мах	
С	5.20	5.30	
E	0.635 BSC		
x	0.30	0.40	
Y	1.50	1.60	

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.

2. This land pattern design is based on the IPC-7351 guidelines.

3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.

5. The stencil thickness should be 0.125 mm (5 mils).

6. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.

7. A No-Clean, Type-3 solder paste is recommended.

8. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.