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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Discontinued at Digi-Key
Core Processor	CIP-51 8051
Core Size	8-Bit
Speed	50MHz
Connectivity	I <sup>2</sup> C, SMBus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	28
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2.25K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 20x10/12b SAR; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-QFP
Supplier Device Package	32-QFP (7x7)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/silicon-labs/efm8bb31f16g-b-qfp32r">https://www.e-xfl.com/product-detail/silicon-labs/efm8bb31f16g-b-qfp32r</a>

## 1. Feature List

The EFM8BB3 device family are fully integrated, mixed-signal system-on-a-chip MCUs. Highlighted features are listed below.

- Core:
  - Pipelined CIP-51 Core
  - Fully compatible with standard 8051 instruction set
  - 70% of instructions execute in 1-2 clock cycles
  - 50 MHz maximum operating frequency
- Memory:
  - Up to 64 kB flash memory (63 kB user-accessible), in-system re-programmable from firmware in 512-byte sectors
  - Up to 4352 bytes RAM (including 256 bytes standard 8051 RAM and 4096 bytes on-chip XRAM)
- Power:
  - Internal LDO regulator for CPU core voltage
  - Power-on reset circuit and brownout detectors
- I/O: Up to 29 total multifunction I/O pins:
  - Up to 25 pins 5 V tolerant under bias
  - Selectable state retention through reset events
  - Flexible peripheral crossbar for peripheral routing
  - 5 mA source, 12.5 mA sink allows direct drive of LEDs
- Clock Sources:
  - Internal 49 MHz oscillator with accuracy of  $\pm 2\%$
  - Internal 24.5 MHz oscillator with  $\pm 2\%$  accuracy
  - Internal 80 kHz low-frequency oscillator
  - External CMOS clock option
  - External crystal/RC Oscillator (up to 25 MHz)
- Analog:
  - 12/10-Bit Analog-to-Digital Converter (ADC)
  - Internal temperature sensor
  - 4 x 12-Bit Digital-to-Analog Converters (DAC)
  - 2 x Low-current analog comparators with adjustable reference
- Communications and Digital Peripherals:
  - 2 x UART, up to 3 Mbaud
  - SPI™ Master / Slave, up to 12 Mbps
  - SMBus™/I2C™ Master / Slave, up to 400 kbps
  - I2C High-Speed Slave, up to 3.4 Mbps
  - 16-bit CRC unit, supporting automatic CRC of flash at 256-byte boundaries
  - 4 Configurable Logic Units
- Timers/Counters and PWM:
  - 6-channel programmable counter array (PCA) supporting PWM, capture/compare, and frequency output modes
  - 6 x 16-bit general-purpose timers
  - Independent watchdog timer, clocked from the low frequency oscillator
- On-Chip, Non-Intrusive Debugging
  - Full memory and register inspection
  - Four hardware breakpoints, single-stepping
- Pre-programmed UART bootloader
- Temperature range -40 to 85 °C or -40 to 125 °C

With on-chip power-on reset, voltage supply monitor, watchdog timer, and clock oscillator, the EFM8BB3 devices are truly standalone system-on-a-chip solutions. The flash memory is reprogrammable in-circuit, providing nonvolatile data storage and allowing field upgrades of the firmware. The on-chip debugging interface (C2) allows non-intrusive (uses no on-chip resources), full speed, in-circuit debugging using the production MCU installed in the final application. This debug logic supports inspection and modification of memory and registers, setting breakpoints, single stepping, and run and halt commands. All analog and digital peripherals are fully functional while debugging. Device operation is specified from 2.2 V up to a 3.6 V supply. Devices are AEC-Q100 qualified and available in 4x4 mm 32-pin QFN, 3x3 mm 24-pin QFN, 32-pin QFP, or 24-pin QSOP packages. All package options are lead-free and RoHS compliant.

## 3. System Overview

### 3.1 Introduction

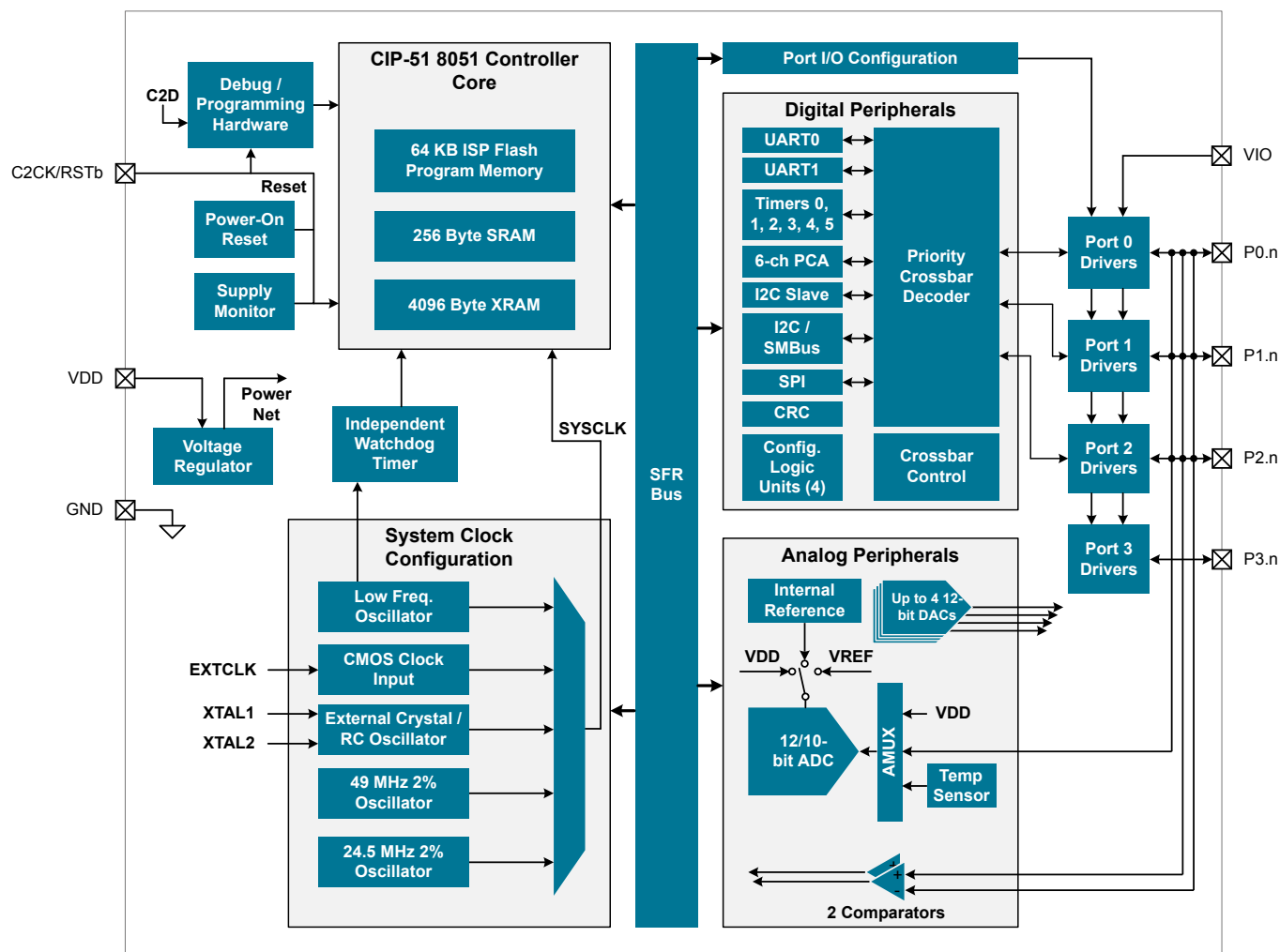


Figure 3.1. Detailed EFM8BB3 Block Diagram

### 3.4 Clocking

The CPU core and peripheral subsystem may be clocked by both internal and external oscillator resources. By default, the system clock comes up running from the 24.5 MHz oscillator divided by 8.

The clock control system offers the following features:

- Provides clock to core and peripherals.
- 24.5 MHz internal oscillator (HFOSC0), accurate to  $\pm 2\%$  over supply and temperature corners.
- 49 MHz internal oscillator (HFOSC1), accurate to  $\pm 2\%$  over supply and temperature corners.
- 80 kHz low-frequency oscillator (LFOSC0).
- External RC, CMOS, and high-frequency crystal clock options (EXTCLK).
- Clock divider with eight settings for flexible clock scaling:
  - Divide the selected clock source by 1, 2, 4, 8, 16, 32, 64, or 128.
  - HFOSC0 and HFOSC1 include 1.5x pre-scalers for further flexibility.

### 3.5 Counters/Timers and PWM

#### Programmable Counter Array (PCA0)

The programmable counter array (PCA) provides multiple channels of enhanced timer and PWM functionality while requiring less CPU intervention than standard counter/timers. The PCA consists of a dedicated 16-bit counter/timer and one 16-bit capture/compare module for each channel. The counter/timer is driven by a programmable timebase that has flexible external and internal clocking options. Each capture/compare module may be configured to operate independently in one of five modes: Edge-Triggered Capture, Software Timer, High-Speed Output, Frequency Output, or Pulse-Width Modulated (PWM) Output. Each capture/compare module has its own associated I/O line (CEXn) which is routed through the crossbar to port I/O when enabled.

- 16-bit time base
- Programmable clock divisor and clock source selection
- Up to six independently-configurable channels
- 8, 9, 10, 11 and 16-bit PWM modes (center or edge-aligned operation)
- Output polarity control
- Frequency output mode
- Capture on rising, falling or any edge
- Compare function for arbitrary waveform generation
- Software timer (internal compare) mode
- Can accept hardware “kill” signal from comparator 0 or comparator 1

### 3.10 Bootloader

All devices come pre-programmed with a UART0 bootloader. This bootloader resides in the code security page, which is the last page of code flash; it can be erased if it is not needed.

The byte before the Lock Byte is the Bootloader Signature Byte. Setting this byte to a value of 0xA5 indicates the presence of the bootloader in the system. Any other value in this location indicates that the bootloader is not present in flash.

When a bootloader is present, the device will jump to the bootloader vector after any reset, allowing the bootloader to run. The bootloader then determines if the device should stay in bootload mode or jump to the reset vector located at 0x0000. When the bootloader is not present, the device will jump to the reset vector of 0x0000 after any reset.

More information about the bootloader protocol and usage can be found in *AN945: EFM8 Factory Bootloader User Guide*. Application notes can be found on the Silicon Labs website ([www.silabs.com/8bit-appnotes](http://www.silabs.com/8bit-appnotes)) or within Simplicity Studio by using the [Application Notes] tile.

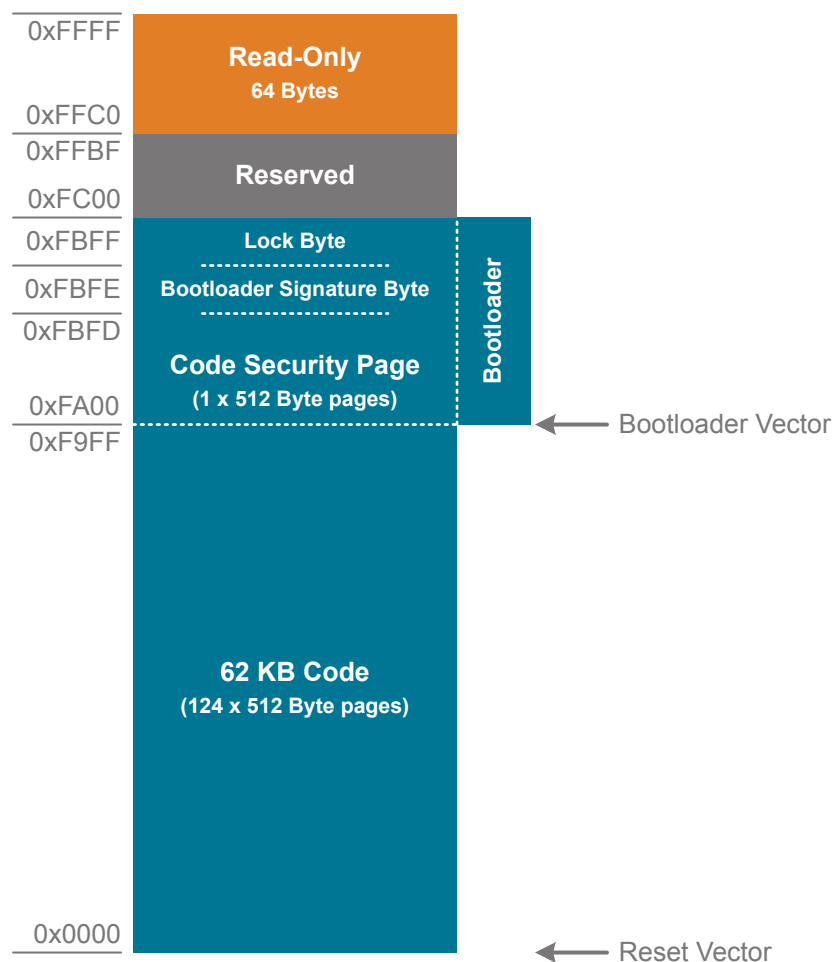


Figure 3.2. Flash Memory Map with Bootloader — 62.5 KB Devices

Table 3.2. Summary of Pins for Bootloader Communication

Bootloader	Pins for Bootload Communication
UART	TX – P0.4
	RX – P0.5

#### 4.1.6 Internal Oscillators

**Table 4.6. Internal Oscillators**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>High Frequency Oscillator 0 (24.5 MHz)</b>						
Oscillator Frequency	$f_{\text{HFOSC0}}$	Full Temperature and Supply Range	24	24.5	25	MHz
Power Supply Sensitivity	$\text{PSS}_{\text{HFOSC0}}$	$T_A = 25^\circ\text{C}$	—	0.5	—	%/V
Temperature Sensitivity	$\text{TS}_{\text{HFOSC0}}$	$V_{\text{DD}} = 3.0\text{ V}$	—	40	—	ppm/°C
<b>High Frequency Oscillator 1 (49 MHz)</b>						
Oscillator Frequency	$f_{\text{HFOSC1}}$	Full Temperature and Supply Range	48.02	49	49.98	MHz
Power Supply Sensitivity	$\text{PSS}_{\text{HFOSC1}}$	$T_A = 25^\circ\text{C}$	—	300	—	ppm/V
Temperature Sensitivity	$\text{TS}_{\text{HFOSC1}}$	$V_{\text{DD}} = 3.0\text{ V}$	—	103	—	ppm/°C
<b>Low Frequency Oscillator (80 kHz)</b>						
Oscillator Frequency	$f_{\text{LFOSC}}$	Full Temperature and Supply Range	75	80	85	kHz
Power Supply Sensitivity	$\text{PSS}_{\text{LFOSC}}$	$T_A = 25^\circ\text{C}$	—	0.05	—	%/V
Temperature Sensitivity	$\text{TS}_{\text{LFOSC}}$	$V_{\text{DD}} = 3.0\text{ V}$	—	65	—	ppm/°C

#### 4.1.7 External Clock Input

**Table 4.7. External Clock Input**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
External Input CMOS Clock Frequency (at EXTCLK pin)	$f_{\text{CMOS}}$		0	—	50	MHz
External Input CMOS Clock High Time	$t_{\text{CMOSH}}$		9	—	—	ns
External Input CMOS Clock Low Time	$t_{\text{CMOSL}}$		9	—	—	ns

#### 4.1.11 Temperature Sensor

**Table 4.11. Temperature Sensor**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Offset	$V_{OFF}$	$T_A = 0\text{ }^{\circ}\text{C}$	—	751	—	mV
Offset Error <sup>1</sup>	$E_{OFF}$	$T_A = 0\text{ }^{\circ}\text{C}$	—	19	—	mV
Slope	M		—	2.82	—	mV/ $^{\circ}\text{C}$
Slope Error <sup>1</sup>	$E_M$		—	29	—	$\mu\text{V}/^{\circ}\text{C}$
Linearity	LIN	$T = -40\text{ }^{\circ}\text{C}$ to $85\text{ }^{\circ}\text{C}$	—	$\pm 0.4$	—	$^{\circ}\text{C}$
		$T = -40\text{ }^{\circ}\text{C}$ to $125\text{ }^{\circ}\text{C}$ (I-grade parts only)	—	-0.6 to 1.2	—	$^{\circ}\text{C}$
Turn-on Time	$t_{ON}$		—	3.5	—	$\mu\text{s}$
<b>Note:</b> 1. Represents one standard deviation from the mean.						

#### 4.1.16 SMBus

**Table 4.16. SMBus Peripheral Timing Performance (Master Mode)**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>Standard Mode (100 kHz Class)</b>						
I2C Operating Frequency	$f_{I2C}$		0	—	$70^2$	kHz
SMBus Operating Frequency	$f_{SMB}$		$40^1$	—	$70^2$	kHz
Bus Free Time Between STOP and START Conditions	$t_{BUF}$		9.4	—	—	$\mu s$
Hold Time After (Repeated) START Condition	$t_{HD:STA}$		4.7	—	—	$\mu s$
Repeated START Condition Setup Time	$t_{SU:STA}$		9.4	—	—	$\mu s$
STOP Condition Setup Time	$t_{SU:STO}$		9.4	—	—	$\mu s$
Data Hold Time	$t_{HD:DAT}$		0	—	—	$\mu s$
Data Setup Time	$t_{SU:DAT}$		4.7	—	—	$\mu s$
Detect Clock Low Timeout	$t_{TIMEOUT}$		25	—	—	ms
Clock Low Period	$t_{LOW}$		4.7	—	—	$\mu s$
Clock High Period	$t_{HIGH}$		9.4	—	$50^3$	$\mu s$
<b>Fast Mode (400 kHz Class)</b>						
I2C Operating Frequency	$f_{I2C}$		0	—	$256^2$	kHz
SMBus Operating Frequency	$f_{SMB}$		$40^1$	—	$256^2$	kHz
Bus Free Time Between STOP and START Conditions	$t_{BUF}$		2.6	—	—	$\mu s$
Hold Time After (Repeated) START Condition	$t_{HD:STA}$		1.3	—	—	$\mu s$
Repeated START Condition Setup Time	$t_{SU:STA}$		2.6	—	—	$\mu s$
STOP Condition Setup Time	$t_{SU:STO}$		2.6	—	—	$\mu s$
Data Hold Time	$t_{HD:DAT}$		0	—	—	$\mu s$
Data Setup Time	$t_{SU:DAT}$		1.3	—	—	$\mu s$
Detect Clock Low Timeout	$t_{TIMEOUT}$		25	—	—	ms
Clock Low Period	$t_{LOW}$		1.3	—	—	$\mu s$
Clock High Period	$t_{HIGH}$		2.6	—	$50^3$	$\mu s$

**Note:**

1. The minimum SMBus frequency is limited by the maximum Clock High Period requirement of the SMBus specification.
2. The maximum I2C and SMBus frequencies are limited by the minimum Clock Low Period requirements of their respective specifications.
3. SMBus has a maximum requirement of 50  $\mu s$  for Clock High Period. Operating frequencies lower than 40 kHz will be longer than 50  $\mu s$ . I2C can support periods longer than 50  $\mu s$ .



Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
15	P2.2	Multifunction I/O	Yes	P2MAT.2 CLU2OUT CLU1A.15 CLU2B.14 CLU3A.14	ADC0.15 CMP1P.4 CMP1N.4
16	P2.1	Multifunction I/O	Yes	P2MAT.1 I2C0_SCL CLU1B.14 CLU2A.15 CLU3B.15	ADC0.14 CMP1P.3 CMP1N.3
17	P2.0	Multifunction I/O	Yes	P2MAT.0 I2C0_SDA CLU1A.14 CLU2A.14 CLU3B.14	CMP1P.2 CMP1N.2
18	P1.7	Multifunction I/O	Yes	P1MAT.7 CLU0B.15 CLU1B.13 CLU2A.13	ADC0.13 CMP0P.9 CMP0N.9
19	P1.6	Multifunction I/O	Yes	P1MAT.6 CLU0A.15 CLU1B.12 CLU2A.12	ADC0.12
20	P1.5	Multifunction I/O	Yes	P1MAT.5 CLU0B.14 CLU1A.13 CLU2B.13	ADC0.11
21	P1.4	Multifunction I/O	Yes	P1MAT.4 CLU0A.14 CLU1A.12 CLU2B.12	ADC0.10
22	P1.3	Multifunction I/O	Yes	P1MAT.3 CLU0B.13 CLU1B.11 CLU2B.11 CLU3A.13	ADC0.9

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
23	P1.2	Multifunction I/O	Yes	P1MAT.2 CLU0A.13 CLU1A.11 CLU2B.10 CLU3A.12	ADC0.8 CMP0P.8 CMP0N.8
24	P1.1	Multifunction I/O	Yes	P1MAT.1 CLU0B.12 CLU1B.10 CLU2A.11 CLU3B.13	ADC0.7 CMP0P.7 CMP0N.7
25	P1.0	Multifunction I/O	Yes	P1MAT.0 CLU1OUT CLU0A.12 CLU1A.10 CLU2A.10 CLU3B.12	ADC0.6 CMP0P.6 CMP0N.6 CMP1P.1 CMP1N.1
26	P0.7	Multifunction I/O	Yes	P0MAT.7 INT0.7 INT1.7 CLU0B.11 CLU1B.9 CLU3A.11	ADC0.5 CMP0P.5 CMP0N.5 CMP1P.0 CMP1N.0
27	P0.6	Multifunction I/O	Yes	P0MAT.6 CNVSTR INT0.6 INT1.6 CLU0A.11 CLU1B.8 CLU3A.10	ADC0.4 CMP0P.4 CMP0N.4
28	P0.5	Multifunction I/O	Yes	P0MAT.5 INT0.5 INT1.5 UART0_RX CLU0B.10 CLU1A.9 CLU3B.11	ADC0.3 CMP0P.3 CMP0N.3

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
29	P0.4	Multifunction I/O	Yes	P0MAT.4 INT0.4 INT1.4 UART0_TX CLU0A.10 CLU1A.8 CLU3B.10	ADC0.2 CMP0P.2 CMP0N.2
30	P0.3	Multifunction I/O	Yes	P0MAT.3 EXTCLK INT0.3 INT1.3 CLU0B.9 CLU2B.9 CLU3A.9	XTAL2
31	P0.2	Multifunction I/O	Yes	P0MAT.2 INT0.2 INT1.2 CLU0OUT CLU0A.9 CLU2B.8 CLU3A.8	XTAL1 ADC0.1 CMP0P.1 CMP0N.1
32	P0.1	Multifunction I/O	Yes	P0MAT.1 INT0.1 INT1.1 CLU0B.8 CLU2A.9 CLU3B.9	ADC0.0 CMP0P.0 CMP0N.0 AGND
Center	GND	Ground			

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
6	P3.7 / C2D	Multifunction I/O / C2 Debug Data			
7	P3.3	Multifunction I/O			DAC3
8	P3.2	Multifunction I/O			DAC2
9	P3.1	Multifunction I/O			DAC1
10	P3.0	Multifunction I/O			DAC0
11	P2.6	Multifunction I/O			ADC0.19 CMP1P.8 CMP1N.8
12	P2.5	Multifunction I/O		CLU3OUT	ADC0.18 CMP1P.7 CMP1N.7
13	P2.4	Multifunction I/O			ADC0.17 CMP1P.6 CMP1N.6
14	P2.3	Multifunction I/O	Yes	P2MAT.3 CLU1B.15 CLU2B.15 CLU3A.15	ADC0.16 CMP1P.5 CMP1N.5
15	P2.2	Multifunction I/O	Yes	P2MAT.2 CLU2OUT CLU1A.15 CLU2B.14 CLU3A.14	ADC0.15 CMP1P.4 CMP1N.4
16	P2.1	Multifunction I/O	Yes	P2MAT.1 I2C0_SCL CLU1B.14 CLU2A.15 CLU3B.15	ADC0.14 CMP1P.3 CMP1N.3
17	P2.0	Multifunction I/O	Yes	P2MAT.0 I2C0_SDA CLU1A.14 CLU2A.14 CLU3B.14	CMP1P.2 CMP1N.2

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
18	P1.7	Multifunction I/O	Yes	P1MAT.7 CLU0B.15 CLU1B.13 CLU2A.13	ADC0.13 CMP0P.9 CMP0N.9
19	P1.6	Multifunction I/O	Yes	P1MAT.6 CLU0A.15 CLU1B.12 CLU2A.12	ADC0.12
20	P1.5	Multifunction I/O	Yes	P1MAT.5 CLU0B.14 CLU1A.13 CLU2B.13	ADC0.11
21	P1.4	Multifunction I/O	Yes	P1MAT.4 CLU0A.14 CLU1A.12 CLU2B.12	ADC0.10
22	P1.3	Multifunction I/O	Yes	P1MAT.3 CLU0B.13 CLU1B.11 CLU2B.11 CLU3A.13	ADC0.9
23	P1.2	Multifunction I/O	Yes	P1MAT.2 CLU0A.13 CLU1A.11 CLU2B.10 CLU3A.12	ADC0.8 CMP0P.8 CMP0N.8
24	P1.1	Multifunction I/O	Yes	P1MAT.1 CLU0B.12 CLU1B.10 CLU2A.11 CLU3B.13	ADC0.7 CMP0P.7 CMP0N.7

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
2	P0.0	Multifunction I/O	Yes	P0MAT.0 INT0.0 INT1.0 CLU0A.8 CLU2A.8 CLU3B.8	VREF
3	GND	Ground			
4	VDD / VIO	Supply Power Input			
5	RSTb / C2CK	Active-low Reset / C2 Debug Clock			
6	P3.0 / C2D	Multifunction I/O / C2 Debug Data			
7	P2.3	Multifunction I/O	Yes	P2MAT.3 CLU1B.15 CLU2B.15 CLU3A.15	DAC3
8	P2.2	Multifunction I/O	Yes	P2MAT.2 CLU1A.15 CLU2B.14 CLU3A.14	DAC2
9	P2.1	Multifunction I/O	Yes	P2MAT.1 CLU1B.14 CLU2A.15 CLU3B.15	DAC1
10	P2.0	Multifunction I/O	Yes	P2MAT.0 CLU1A.14 CLU2A.14 CLU3B.14	DAC0
11	P1.6	Multifunction I/O	Yes	P1MAT.6 CLU3OUT CLU0A.15 CLU1B.12 CLU2A.12	ADC0.11 CMP1P.5 CMP1N.5

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
19	P0.7	Multifunction I/O	Yes	P0MAT.7 INT0.7 INT1.7 CLU1OUT CLU0B.11 CLU1B.9 CLU3A.11	ADC0.5 CMP0P.5 CMP0N.5 CMP1P.1 CMP1N.1
20	P0.6	Multifunction I/O	Yes	P0MAT.6 CNVSTR INT0.6 INT1.6 CLU0A.11 CLU1B.8 CLU3A.10	ADC0.4 CMP0P.4 CMP0N.4 CMP1P.0 CMP1N.0
21	P0.5	Multifunction I/O	Yes	P0MAT.5 INT0.5 INT1.5 UART0_RX CLU0B.10 CLU1A.9 CLU3B.11	ADC0.3 CMP0P.3 CMP0N.3
22	P0.4	Multifunction I/O	Yes	P0MAT.4 INT0.4 INT1.4 UART0_TX CLU0A.10 CLU1A.8 CLU3B.10	ADC0.2 CMP0P.2 CMP0N.2
23	P0.3	Multifunction I/O	Yes	P0MAT.3 EXTCLK INT0.3 INT1.3 CLU0B.9 CLU2B.9 CLU3A.9	XTAL2

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
24	P0.2	Multifunction I/O	Yes	P0MAT.2 INT0.2 INT1.2 CLU0OUT CLU0A.9 CLU2B.8 CLU3A.8	XTAL1 ADC0.1 CMP0P.1 CMP0N.1
Center	GND	Ground			



Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
18	P1.2	Multifunction I/O	Yes	P1MAT.2 CLU0A.13 CLU1A.11 CLU2B.10 CLU3A.12	ADC0.8
19	P1.1	Multifunction I/O	Yes	P1MAT.1 CLU0B.12 CLU1B.10 CLU2A.11 CLU3B.13	ADC0.7
20	P1.0	Multifunction I/O	Yes	P1MAT.0 CLU0A.12 CLU1A.10 CLU2A.10 CLU3B.12	ADC0.6
21	P0.7	Multifunction I/O	Yes	P0MAT.7 INT0.7 INT1.7 CLU1OUT CLU0B.11 CLU1B.9 CLU3A.11	ADC0.5 CMP0P.5 CMP0N.5 CMP1P.1 CMP1N.1
22	P0.6	Multifunction I/O	Yes	P0MAT.6 CNVSTR INT0.6 INT1.6 CLU0A.11 CLU1B.8 CLU3A.10	ADC0.4 CMP0P.4 CMP0N.4 CMP1P.0 CMP1N.0
23	P0.5	Multifunction I/O	Yes	P0MAT.5 INT0.5 INT1.5 UART0_RX CLU0B.10 CLU1A.9 CLU3B.11	ADC0.3 CMP0P.3 CMP0N.3

Dimension	Min	Typ	Max
<b>Note:</b> <ol style="list-style-type: none"> <li>All dimensions shown are in millimeters (mm) unless otherwise noted.</li> <li>Dimensioning and Tolerancing per ANSI Y14.5M-1994.</li> <li>This drawing conforms to JEDEC Solid State Outline MO-220.</li> <li>Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.</li> </ol>			

Dimension	Min	Max
<b>Note:</b> <ol style="list-style-type: none"> <li>1. All dimensions shown are in millimeters (mm) unless otherwise noted.</li> <li>2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.</li> <li>3. This Land Pattern Design is based on the IPC-SM-782 guidelines.</li> <li>4. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.</li> <li>5. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.</li> <li>6. The stencil thickness should be 0.125 mm (5 mils).</li> <li>7. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.</li> <li>8. A 2 x 1 array of 0.7 mm x 1.6 mm openings on a 0.9 mm pitch should be used for the center pad.</li> <li>9. A No-Clean, Type-3 solder paste is recommended.</li> <li>10. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.</li> </ol>		

### 9.3 QFN24 Package Marking

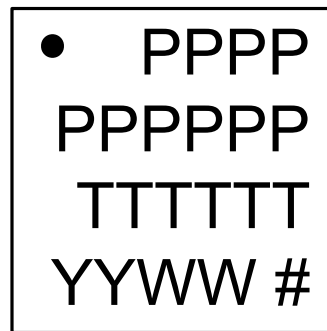


Figure 9.3. QFN24 Package Marking

The package marking consists of:

- P P P P P P P P – The part number designation.
- T T T T T T – A trace or manufacturing code.
- Y Y – The last 2 digits of the assembly year.
- W W – The 2-digit workweek when the device was assembled.
- # – The device revision (A, B, etc.).

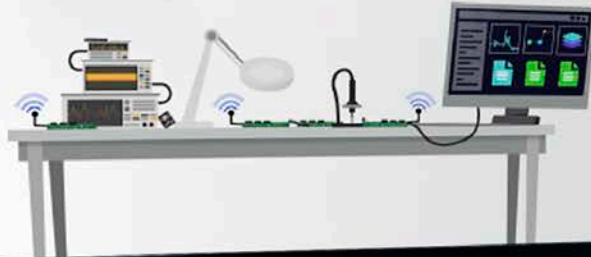
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