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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Not For New Designs
Core Processor	CIP-51 8051
Core Size	8-Bit
Speed	50MHz
Connectivity	I <sup>2</sup> C, SMBus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	20
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2.25K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 12x10/12b SAR; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	24-WFQFN Exposed Pad
Supplier Device Package	24-QFN (4x4)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/silicon-labs/efm8bb31f16i-b-4qfn24r">https://www.e-xfl.com/product-detail/silicon-labs/efm8bb31f16i-b-4qfn24r</a>

## 1. Feature List

The EFM8BB3 device family are fully integrated, mixed-signal system-on-a-chip MCUs. Highlighted features are listed below.

- Core:
  - Pipelined CIP-51 Core
  - Fully compatible with standard 8051 instruction set
  - 70% of instructions execute in 1-2 clock cycles
  - 50 MHz maximum operating frequency
- Memory:
  - Up to 64 kB flash memory (63 kB user-accessible), in-system re-programmable from firmware in 512-byte sectors
  - Up to 4352 bytes RAM (including 256 bytes standard 8051 RAM and 4096 bytes on-chip XRAM)
- Power:
  - Internal LDO regulator for CPU core voltage
  - Power-on reset circuit and brownout detectors
- I/O: Up to 29 total multifunction I/O pins:
  - Up to 25 pins 5 V tolerant under bias
  - Selectable state retention through reset events
  - Flexible peripheral crossbar for peripheral routing
  - 5 mA source, 12.5 mA sink allows direct drive of LEDs
- Clock Sources:
  - Internal 49 MHz oscillator with accuracy of  $\pm 2\%$
  - Internal 24.5 MHz oscillator with  $\pm 2\%$  accuracy
  - Internal 80 kHz low-frequency oscillator
  - External CMOS clock option
  - External crystal/RC Oscillator (up to 25 MHz)
- Analog:
  - 12/10-Bit Analog-to-Digital Converter (ADC)
  - Internal temperature sensor
  - 4 x 12-Bit Digital-to-Analog Converters (DAC)
  - 2 x Low-current analog comparators with adjustable reference
- Communications and Digital Peripherals:
  - 2 x UART, up to 3 Mbaud
  - SPI™ Master / Slave, up to 12 Mbps
  - SMBus™/I2C™ Master / Slave, up to 400 kbps
  - I2C High-Speed Slave, up to 3.4 Mbps
  - 16-bit CRC unit, supporting automatic CRC of flash at 256-byte boundaries
  - 4 Configurable Logic Units
- Timers/Counters and PWM:
  - 6-channel programmable counter array (PCA) supporting PWM, capture/compare, and frequency output modes
  - 6 x 16-bit general-purpose timers
  - Independent watchdog timer, clocked from the low frequency oscillator
- On-Chip, Non-Intrusive Debugging
  - Full memory and register inspection
  - Four hardware breakpoints, single-stepping
- Pre-programmed UART bootloader
- Temperature range -40 to 85 °C or -40 to 125 °C

With on-chip power-on reset, voltage supply monitor, watchdog timer, and clock oscillator, the EFM8BB3 devices are truly standalone system-on-a-chip solutions. The flash memory is reprogrammable in-circuit, providing nonvolatile data storage and allowing field upgrades of the firmware. The on-chip debugging interface (C2) allows non-intrusive (uses no on-chip resources), full speed, in-circuit debugging using the production MCU installed in the final application. This debug logic supports inspection and modification of memory and registers, setting breakpoints, single stepping, and run and halt commands. All analog and digital peripherals are fully functional while debugging. Device operation is specified from 2.2 V up to a 3.6 V supply. Devices are AEC-Q100 qualified and available in 4x4 mm 32-pin QFN, 3x3 mm 24-pin QFN, 32-pin QFP, or 24-pin QSOP packages. All package options are lead-free and RoHS compliant.

### 3.2 Power

All internal circuitry draws power from the VDD supply pin. External I/O pins are powered from the VIO supply voltage (or VDD on devices without a separate VIO connection), while most of the internal circuitry is supplied by an on-chip LDO regulator. Control over the device power can be achieved by enabling/disabling individual peripherals as needed. Each analog peripheral can be disabled when not in use and placed in low power mode. Digital peripherals, such as timers and serial buses, have their clocks gated off and draw little power when they are not in use.

**Table 3.1. Power Modes**

Power Mode	Details	Mode Entry	Wake-Up Sources
Normal	Core and all peripherals clocked and fully operational		
Idle	<ul style="list-style-type: none"> <li>Core halted</li> <li>All peripherals clocked and fully operational</li> <li>Code resumes execution on wake event</li> </ul>	Set IDLE bit in PCON0	Any interrupt
Suspend	<ul style="list-style-type: none"> <li>Core and peripheral clocks halted</li> <li>HFOSC0 and HFOSC1 oscillators stopped</li> <li>Regulator in normal bias mode for fast wake</li> <li>Timer 3 and 4 may clock from LFOSC0</li> <li>Code resumes execution on wake event</li> </ul>	<ol style="list-style-type: none"> <li>Switch SYSCLK to HFOSC0</li> <li>Set SUSPEND bit in PCON1</li> </ol>	<ul style="list-style-type: none"> <li>Timer 4 Event</li> <li>SPI0 Activity</li> <li>I2C0 Slave Activity</li> <li>Port Match Event</li> <li>Comparator 0 Falling Edge</li> <li>CLUn Interrupt-Enabled Event</li> </ul>
Stop	<ul style="list-style-type: none"> <li>All internal power nets shut down</li> <li>Pins retain state</li> <li>Exit on any reset source</li> </ul>	<ol style="list-style-type: none"> <li>Clear STOPCF bit in REG0CN</li> <li>Set STOP bit in PCON0</li> </ol>	Any reset source
Snooze	<ul style="list-style-type: none"> <li>Core and peripheral clocks halted</li> <li>HFOSC0 and HFOSC1 oscillators stopped</li> <li>Regulator in low bias current mode for energy savings</li> <li>Timer 3 and 4 may clock from LFOSC0</li> <li>Code resumes execution on wake event</li> </ul>	<ol style="list-style-type: none"> <li>Switch SYSCLK to HFOSC0</li> <li>Set SNOOZE bit in PCON1</li> </ol>	<ul style="list-style-type: none"> <li>Timer 4 Event</li> <li>SPI0 Activity</li> <li>I2C0 Slave Activity</li> <li>Port Match Event</li> <li>Comparator 0 Falling Edge</li> <li>CLUn Interrupt-Enabled Event</li> </ul>
Shutdown	<ul style="list-style-type: none"> <li>All internal power nets shut down</li> <li>Pins retain state</li> <li>Exit on pin or power-on reset</li> </ul>	<ol style="list-style-type: none"> <li>Set STOPCF bit in REG0CN</li> <li>Set STOP bit in PCON0</li> </ol>	<ul style="list-style-type: none"> <li>RSTb pin reset</li> <li>Power-on reset</li> </ul>

### 3.3 I/O

Digital and analog resources are externally available on the device's multi-purpose I/O pins. Port pins P0.0-P2.3 can be defined as general-purpose I/O (GPIO), assigned to one of the internal digital resources through the crossbar or dedicated channels, or assigned to an analog function. Port pins P2.4 to P3.7 can be used as GPIO. Additionally, the C2 Interface Data signal (C2D) is shared with P3.0 or P3.7, depending on the package option.

The port control block offers the following features:

- Up to 29 multi-functions I/O pins, supporting digital and analog functions.
- Flexible priority crossbar decoder for digital peripheral assignment.
- Two drive strength settings for each port.
- State retention feature allows pins to retain configuration through most reset sources.
- Two direct-pin interrupt sources with dedicated interrupt vectors (INT0 and INT1).
- Up to 24 direct-pin interrupt sources with shared interrupt vector (Port Match).

### 3.4 Clocking

The CPU core and peripheral subsystem may be clocked by both internal and external oscillator resources. By default, the system clock comes up running from the 24.5 MHz oscillator divided by 8.

The clock control system offers the following features:

- Provides clock to core and peripherals.
- 24.5 MHz internal oscillator (HFOSC0), accurate to  $\pm 2\%$  over supply and temperature corners.
- 49 MHz internal oscillator (HFOSC1), accurate to  $\pm 2\%$  over supply and temperature corners.
- 80 kHz low-frequency oscillator (LFOSC0).
- External RC, CMOS, and high-frequency crystal clock options (EXTCLK).
- Clock divider with eight settings for flexible clock scaling:
  - Divide the selected clock source by 1, 2, 4, 8, 16, 32, 64, or 128.
  - HFOSC0 and HFOSC1 include 1.5x pre-scalers for further flexibility.

### 3.5 Counters/Timers and PWM

#### Programmable Counter Array (PCA0)

The programmable counter array (PCA) provides multiple channels of enhanced timer and PWM functionality while requiring less CPU intervention than standard counter/timers. The PCA consists of a dedicated 16-bit counter/timer and one 16-bit capture/compare module for each channel. The counter/timer is driven by a programmable timebase that has flexible external and internal clocking options. Each capture/compare module may be configured to operate independently in one of five modes: Edge-Triggered Capture, Software Timer, High-Speed Output, Frequency Output, or Pulse-Width Modulated (PWM) Output. Each capture/compare module has its own associated I/O line (CEXn) which is routed through the crossbar to port I/O when enabled.

- 16-bit time base
- Programmable clock divisor and clock source selection
- Up to six independently-configurable channels
- 8, 9, 10, 11 and 16-bit PWM modes (center or edge-aligned operation)
- Output polarity control
- Frequency output mode
- Capture on rising, falling or any edge
- Compare function for arbitrary waveform generation
- Software timer (internal compare) mode
- Can accept hardware “kill” signal from comparator 0 or comparator 1

## Timers (Timer 0, Timer 1, Timer 2, Timer 3, Timer 4, and Timer 5)

Several counter/timers are included in the device: two are 16-bit counter/timers compatible with those found in the standard 8051, and the rest are 16-bit auto-reload timers for timing peripherals or for general purpose use. These timers can be used to measure time intervals, count external events and generate periodic interrupt requests. Timer 0 and Timer 1 are nearly identical and have four primary modes of operation. The other timers offer both 16-bit and split 8-bit timer functionality with auto-reload and capture capabilities.

Timer 0 and Timer 1 include the following features:

- Standard 8051 timers, supporting backwards-compatibility with firmware and hardware.
- Clock sources include SYSCLK, SYSCLK divided by 12, 4, or 48, the External Clock divided by 8, or an external pin.
- 8-bit auto-reload counter/timer mode
- 13-bit counter/timer mode
- 16-bit counter/timer mode
- Dual 8-bit counter/timer mode (Timer 0)

Timer 2, Timer 3, Timer 4, and Timer 5 are 16-bit timers including the following features:

- Clock sources for all timers include SYSCLK, SYSCLK divided by 12, or the External Clock divided by 8
- LFOSC0 divided by 8 may be used to clock Timer 3 and Timer 4 in active or suspend/snooze power modes
- Timer 4 is a low-power wake source, and can be chained together with Timer 3
- 16-bit auto-reload timer mode
- Dual 8-bit auto-reload timer mode
- External pin capture
- LFOSC0 capture
- Comparator 0 capture
- Configurable Logic output capture

## Watchdog Timer (WDT0)

The device includes a programmable watchdog timer (WDT) running off the low-frequency oscillator. A WDT overflow forces the MCU into the reset state. To prevent the reset, the WDT must be restarted by application software before overflow. If the system experiences a software or hardware malfunction preventing the software from restarting the WDT, the WDT overflows and causes a reset. Following a reset, the WDT is automatically enabled and running with the default maximum time interval. If needed, the WDT can be disabled by system software or locked on to prevent accidental disabling. Once locked, the WDT cannot be disabled until the next system reset. The state of the RST pin is unaffected by this reset.

The Watchdog Timer has the following features:

- Programmable timeout interval
- Runs from the low-frequency oscillator
- Lock-out feature to prevent any modification until a system reset

## 3.6 Communications and Other Digital Peripherals

### Universal Asynchronous Receiver/Transmitter (UART0)

UART0 is an asynchronous, full duplex serial port offering modes 1 and 3 of the standard 8051 UART. Enhanced baud rate support allows a wide range of clock sources to generate standard baud rates. Received data buffering allows UART0 to start reception of a second incoming data byte before software has finished reading the previous data byte.

The UART module provides the following features:

- Asynchronous transmissions and receptions.
- Baud rates up to  $\text{SYSCLK}/2$  (transmit) or  $\text{SYSCLK}/8$  (receive).
- 8- or 9-bit data.
- Automatic start and stop generation.
- Single-byte FIFO on transmit and receive.

## Universal Asynchronous Receiver/Transmitter (UART1)

UART1 is an asynchronous, full duplex serial port offering a variety of data formatting options. A dedicated baud rate generator with a 16-bit timer and selectable prescaler is included, which can generate a wide range of baud rates. A received data FIFO allows UART1 to receive multiple bytes before data is lost and an overflow occurs.

UART1 provides the following features:

- Asynchronous transmissions and receptions
- Dedicated baud rate generator supports baud rates up to  $\text{SYSCLK}/2$  (transmit) or  $\text{SYSCLK}/8$  (receive)
- 5, 6, 7, 8, or 9 bit data
- Automatic start and stop generation
- Automatic parity generation and checking
- Single-byte buffer on transmit and receive
- Auto-baud detection
- LIN break and sync field detection
- CTS / RTS hardware flow control

## Serial Peripheral Interface (SPI0)

The serial peripheral interface (SPI) module provides access to a flexible, full-duplex synchronous serial bus. The SPI can operate as a master or slave device in both 3-wire or 4-wire modes, and supports multiple masters and slaves on a single SPI bus. The slave-select (NSS) signal can be configured as an input to select the SPI in slave mode, or to disable master mode operation in a multi-master environment, avoiding contention on the SPI bus when more than one master attempts simultaneous data transfers. NSS can also be configured as a firmware-controlled chip-select output in master mode, or disabled to reduce the number of pins required. Additional general purpose port I/O pins can be used to select multiple slave devices in master mode.

- Supports 3- or 4-wire master or slave modes
- Supports external clock frequencies up to 12 Mbps in master or slave mode
- Support for all clock phase and polarity modes
- 8-bit programmable clock rate (master)
- Programmable receive timeout (slave)
- Two byte FIFO on transmit and receive
- Can operate in suspend or snooze modes and wake the CPU on reception of a byte
- Support for multiple masters on the same data lines

## System Management Bus / I2C (SMB0)

The SMBus I/O interface is a two-wire, bi-directional serial bus. The SMBus is compliant with the System Management Bus Specification, version 1.1, and compatible with the I<sup>2</sup>C serial bus.

The SMBus module includes the following features:

- Standard (up to 100 kbps) and Fast (400 kbps) transfer speeds
- Support for master, slave, and multi-master modes
- Hardware synchronization and arbitration for multi-master mode
- Clock low extending (clock stretching) to interface with faster masters
- Hardware support for 7-bit slave and general call address recognition
- Firmware support for 10-bit slave address decoding
- Ability to inhibit all slave states
- Programmable data setup/hold times
- Transmit and receive FIFOs (one byte) to help increase throughput in faster applications

## I2C Slave (I2CSLAVE0)

The I2C Slave interface is a 2-wire, bidirectional serial bus that is compatible with the I2C Bus Specification 3.0. It is capable of transferring in high-speed mode (HS-mode) at speeds of up to 3.4 Mbps. Firmware can write to the I2C interface, and the I2C interface can autonomously control the serial transfer of data. The interface also supports clock stretching for cases where the core may be temporarily prohibited from transmitting a byte or processing a received byte during an I2C transaction. This module operates only as an I2C slave device.

The I2C module includes the following features:

- Standard (up to 100 kbps), Fast (400 kbps), Fast Plus (1 Mbps), and High-speed (3.4 Mbps) transfer speeds
- Support for slave mode only
- Clock low extending (clock stretching) to interface with faster masters
- Hardware support for 7-bit slave address recognition
- Transmit and receive FIFOs (two byte) to help increase throughput in faster applications
- Hardware support for multiple slave addresses with the option to save the matching address in the receive FIFO

## 16-bit CRC (CRC0)

The cyclic redundancy check (CRC) module performs a CRC using a 16-bit polynomial. CRC0 accepts a stream of 8-bit data and posts the 16-bit result to an internal register. In addition to using the CRC block for data manipulation, hardware can automatically CRC the flash contents of the device.

The CRC module is designed to provide hardware calculations for flash memory verification and communications protocols. The CRC module supports the standard CCITT-16 16-bit polynomial (0x1021), and includes the following features:

- Support for CCITT-16 polynomial
- Byte-level bit reversal
- Automatic CRC of flash contents on one or more 256-byte blocks
- Initial seed selection of 0x0000 or 0xFFFF

## Configurable Logic Units (CLU0, CLU1, CLU2, and CLU3)

The Configurable Logic block consists of multiple Configurable Logic Units (CLUs). CLUs are flexible logic functions which may be used for a variety of digital functions, such as replacing system glue logic, aiding in the generation of special waveforms, or synchronizing system event triggers.

- Four configurable logic units (CLUs), with direct-pin and internal logic connections
- Each unit supports 256 different combinatorial logic functions (AND, OR, XOR, muxing, etc.) and includes a clocked flip-flop for synchronous operations
- Units may be operated synchronously or asynchronously
- May be cascaded together to perform more complicated logic functions
- Can operate in conjunction with serial peripherals such as UART and SPI or timing peripherals such as timers and PCA channels
- Can be used to synchronize and trigger multiple on-chip resources (ADC, DAC, Timers, etc.)
- Asynchronous output may be used to wake from low-power states

## 3.7 Analog

### 12/10-Bit Analog-to-Digital Converter (ADC0)

The ADC is a successive-approximation-register (SAR) ADC with 12- and 10-bit modes, integrated track-and hold and a programmable window detector. The ADC is fully configurable under software control via several registers. The ADC may be configured to measure different signals using the analog multiplexer. The voltage reference for the ADC is selectable between internal and external reference sources.

- Up to 20 external inputs
- Single-ended 12-bit and 10-bit modes
- Supports an output update rate of up to 350 ksps in 12-bit mode
- Channel sequencer logic with direct-to-XDATA output transfers
- Operation in a low power mode at lower conversion speeds
- Asynchronous hardware conversion trigger, selectable between software, external I/O and internal timer and configurable logic sources
- Output data window comparator allows automatic range checking
- Support for output data accumulation
- Conversion complete and window compare interrupts supported
- Flexible output data formatting
- Includes a fully-internal fast-settling 1.65 V reference and an on-chip precision 2.4 / 1.2 V reference, with support for using the supply as the reference, an external reference and signal ground
- Integrated temperature sensor

### 12-Bit Digital-to-Analog Converters (DAC0, DAC1, DAC2, DAC3)

The DAC modules are 12-bit Digital-to-Analog Converters with the capability to synchronize multiple outputs together. The DACs are fully configurable under software control. The voltage reference for the DACs is selectable between internal and external reference sources.

- Voltage output with 12-bit performance
- Supports an update rate of 200 ksps
- Hardware conversion trigger, selectable between software, external I/O and internal timer and configurable logic sources
- Outputs may be configured to persist through reset and maintain output state to avoid system disruption
- Multiple DAC outputs can be synchronized together
- DAC pairs (DAC0 and 1 or DAC2 and 3) support complementary output waveform generation
- Outputs may be switched between two levels according to state of configurable logic / PWM input trigger
- Flexible input data formatting
- Supports references from internal supply, on-chip precision reference, or external VREF pin



## 4.1.4 Flash Memory

Table 4.4. Flash Memory

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Write Time <sup>1,2</sup>	$t_{\text{WRITE}}$	One Byte, $F_{\text{SYSCLK}} = 24.5 \text{ MHz}$	19	20	21	$\mu\text{s}$
Erase Time <sup>1,2</sup>	$t_{\text{ERASE}}$	One Page, $F_{\text{SYSCLK}} = 24.5 \text{ MHz}$	5.2	5.35	5.5	ms
$V_{\text{DD}}$ Voltage During Programming <sup>3</sup>	$V_{\text{PROG}}$		2.2	—	3.6	V
Endurance (Write/Erase Cycles)	$N_{\text{WE}}$		20k	100k	—	Cycles
CRC Calculation Time	$t_{\text{CRC}}$	One 256-Byte Block $\text{SYSCLK} = 49 \text{ MHz}$	—	5.5	—	$\mu\text{s}$

**Note:**

1. Does not include sequencing time before and after the write/erase operation, which may be multiple SYSCLK cycles.
2. The internal High-Frequency Oscillator 0 has a programmable output frequency, which is factory programmed to 24.5 MHz. If user firmware adjusts the oscillator speed, it must be between 22 and 25 MHz during any flash write or erase operation. It is recommended to write the HFO0CAL register back to its reset value when writing or erasing flash.
3. Flash can be safely programmed at any voltage above the supply monitor threshold ( $V_{\text{VDDM}}$ ).
4. Data Retention Information is published in the Quarterly Quality and Reliability Report.

## 4.1.5 Power Management Timing

Table 4.5. Power Management Timing

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Idle Mode Wake-up Time	$t_{\text{IDLEWK}}$		2	—	3	SYSCLKs
Suspend Mode Wake-up Time	$t_{\text{SUS-}}t_{\text{PENDWK}}$	$\text{SYSCLK} = \text{HFOSC0}$ $\text{CLKDIV} = 0x00$	—	170	—	ns
Snooze Mode Wake-up Time	$t_{\text{SLEEPWK}}$	$\text{SYSCLK} = \text{HFOSC0}$ $\text{CLKDIV} = 0x00$	—	12	—	$\mu\text{s}$

## 4.1.9 ADC

Table 4.9. ADC

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Resolution	N <sub>bits</sub>	12 Bit Mode	12			Bits
		10 Bit Mode	10			Bits
Throughput Rate (High Speed Mode)	f <sub>S</sub>	10 Bit Mode	—	—	1.125	Msp/s
Throughput Rate (Low Power Mode)	f <sub>S</sub>	12 Bit Mode	—	—	340	ksps
		10 Bit Mode	—	—	360	ksps
Tracking Time	t <sub>TRK</sub>	High Speed Mode	230	—	—	ns
		Low Power Mode	450	—	—	ns
Power-On Time	t <sub>PWR</sub>		1.2	—	—	μs
SAR Clock Frequency	f <sub>SAR</sub>	High Speed Mode	—	—	18	MHz
		Low Power Mode	—	—	12.25	MHz
Conversion Time <sup>1</sup>	t <sub>CNV</sub>	12-Bit Conversion, SAR Clock = 6.125 MHz, System Clock = 49 MHz	2.0			μs
		10-Bit Conversion, SAR Clock = 16.33 MHz, System Clock = 49 MHz	0.658			μs
Sample/Hold Capacitor	C <sub>SAR</sub>	Gain = 1	—	5.2	—	pF
		Gain = 0.75	—	3.9	—	pF
		Gain = 0.5	—	2.6	—	pF
		Gain = 0.25	—	1.3	—	pF
Input Pin Capacitance	C <sub>IN</sub>		—	20	—	pF
Input Mux Impedance	R <sub>MUX</sub>		—	550	—	Ω
Voltage Reference Range	V <sub>REF</sub>		1	—	V <sub>IO</sub>	V
Input Voltage Range <sup>2</sup>	V <sub>IN</sub>		0	—	V <sub>REF</sub> / Gain	V
Power Supply Rejection Ratio	PSRR <sub>ADC</sub>	At 1 kHz	—	66	—	dB
		At 1 MHz	—	43	—	dB
DC Performance						

### 4.1.13 Comparators

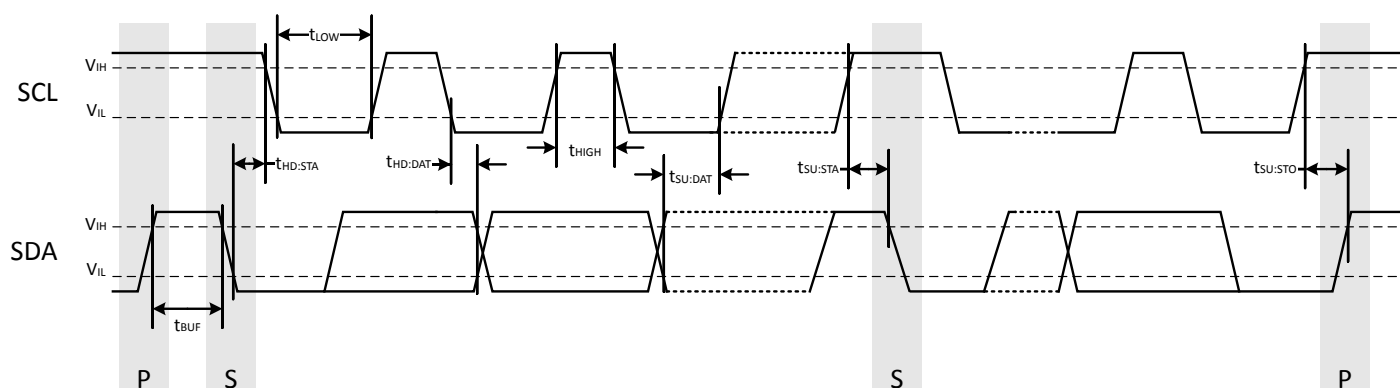
Table 4.13. Comparators

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Response Time, CPMD = 00 (Highest Speed)	$t_{RESP0}$	+100 mV Differential	—	100	—	ns
		-100 mV Differential	—	150	—	ns
Response Time, CPMD = 11 (Low- est Power)	$t_{RESP3}$	+100 mV Differential	—	1.5	—	μs
		-100 mV Differential	—	3.5	—	μs
Positive Hysteresis Mode 0 (CPMD = 00)	$HYS_{CP+}$	CPHYP = 00	—	0.4	—	mV
		CPHYP = 01	—	8	—	mV
		CPHYP = 10	—	16	—	mV
		CPHYP = 11	—	32	—	mV
Negative Hysteresis Mode 0 (CPMD = 00)	$HYS_{CP-}$	CPHYN = 00	—	-0.4	—	mV
		CPHYN = 01	—	-8	—	mV
		CPHYN = 10	—	-16	—	mV
		CPHYN = 11	—	-32	—	mV
Positive Hysteresis Mode 1 (CPMD = 01)	$HYS_{CP+}$	CPHYP = 00	—	0.5	—	mV
		CPHYP = 01	—	6	—	mV
		CPHYP = 10	—	12	—	mV
		CPHYP = 11	—	24	—	mV
Negative Hysteresis Mode 1 (CPMD = 01)	$HYS_{CP-}$	CPHYN = 00	—	-0.5	—	mV
		CPHYN = 01	—	-6	—	mV
		CPHYN = 10	—	-12	—	mV
		CPHYN = 11	—	-24	—	mV
Positive Hysteresis Mode 2 (CPMD = 10)	$HYS_{CP+}$	CPHYP = 00	—	0.7	—	mV
		CPHYP = 01	—	4.5	—	mV
		CPHYP = 10	—	9	—	mV
		CPHYP = 11	—	18	—	mV
Negative Hysteresis Mode 2 (CPMD = 10)	$HYS_{CP-}$	CPHYN = 00	—	-0.6	—	mV
		CPHYN = 01	—	-4.5	—	mV
		CPHYN = 10	—	-9	—	mV
		CPHYN = 11	—	-18	—	mV
Positive Hysteresis Mode 3 (CPMD = 11)	$HYS_{CP+}$	CPHYP = 00	—	1.5	—	mV
		CPHYP = 01	—	4	—	mV
		CPHYP = 10	—	8	—	mV
		CPHYP = 11	—	16	—	mV

**Table 4.17. SMBus Peripheral Timing Formulas (Master Mode)**

Parameter	Symbol	Clocks
SMBus Operating Frequency	$f_{\text{SMB}}$	$f_{\text{CSO}} / 3$
Bus Free Time Between STOP and START Conditions	$t_{\text{BUF}}$	$2 / f_{\text{CSO}}$
Hold Time After (Repeated) START Condition	$t_{\text{HD:STA}}$	$1 / f_{\text{CSO}}$
Repeated START Condition Setup Time	$t_{\text{SU:STA}}$	$2 / f_{\text{CSO}}$
STOP Condition Setup Time	$t_{\text{SU:STO}}$	$2 / f_{\text{CSO}}$
Clock Low Period	$t_{\text{LOW}}$	$1 / f_{\text{CSO}}$
Clock High Period	$t_{\text{HIGH}}$	$2 / f_{\text{CSO}}$

**Note:**  
1.  $f_{\text{CSO}}$  is the SMBus peripheral clock source overflow frequency.



**Figure 4.1. SMBus Peripheral Timing Diagram (Master Mode)**

## 4.2 Thermal Conditions

**Table 4.18. Thermal Conditions**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Thermal Resistance	$\theta_{\text{JA}}$	QFN24 Packages	—	30	—	°C/W
		QFN32 Packages	—	26	—	°C/W
		QFP32 Packages	—	80	—	°C/W
		QSOP24 Packages	—	65	—	°C/W

**Note:**  
1. Thermal resistance assumes a multi-layer PCB with any exposed pad soldered to a PCB pad.

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
15	P2.2	Multifunction I/O	Yes	P2MAT.2 CLU2OUT CLU1A.15 CLU2B.14 CLU3A.14	ADC0.15 CMP1P.4 CMP1N.4
16	P2.1	Multifunction I/O	Yes	P2MAT.1 I2C0_SCL CLU1B.14 CLU2A.15 CLU3B.15	ADC0.14 CMP1P.3 CMP1N.3
17	P2.0	Multifunction I/O	Yes	P2MAT.0 I2C0_SDA CLU1A.14 CLU2A.14 CLU3B.14	CMP1P.2 CMP1N.2
18	P1.7	Multifunction I/O	Yes	P1MAT.7 CLU0B.15 CLU1B.13 CLU2A.13	ADC0.13 CMP0P.9 CMP0N.9
19	P1.6	Multifunction I/O	Yes	P1MAT.6 CLU0A.15 CLU1B.12 CLU2A.12	ADC0.12
20	P1.5	Multifunction I/O	Yes	P1MAT.5 CLU0B.14 CLU1A.13 CLU2B.13	ADC0.11
21	P1.4	Multifunction I/O	Yes	P1MAT.4 CLU0A.14 CLU1A.12 CLU2B.12	ADC0.10
22	P1.3	Multifunction I/O	Yes	P1MAT.3 CLU0B.13 CLU1B.11 CLU2B.11 CLU3A.13	ADC0.9

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
29	P0.4	Multifunction I/O	Yes	P0MAT.4 INT0.4 INT1.4 UART0_TX CLU0A.10 CLU1A.8 CLU3B.10	ADC0.2 CMP0P.2 CMP0N.2
30	P0.3	Multifunction I/O	Yes	P0MAT.3 EXTCLK INT0.3 INT1.3 CLU0B.9 CLU2B.9 CLU3A.9	XTAL2
31	P0.2	Multifunction I/O	Yes	P0MAT.2 INT0.2 INT1.2 CLU0OUT CLU0A.9 CLU2B.8 CLU3A.8	XTAL1 ADC0.1 CMP0P.1 CMP0N.1
32	P0.1	Multifunction I/O	Yes	P0MAT.1 INT0.1 INT1.1 CLU0B.8 CLU2A.9 CLU3B.9	ADC0.0 CMP0P.0 CMP0N.0 AGND
Center	GND	Ground			

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
6	P3.7 / C2D	Multifunction I/O / C2 Debug Data			
7	P3.3	Multifunction I/O			DAC3
8	P3.2	Multifunction I/O			DAC2
9	P3.1	Multifunction I/O			DAC1
10	P3.0	Multifunction I/O			DAC0
11	P2.6	Multifunction I/O			ADC0.19 CMP1P.8 CMP1N.8
12	P2.5	Multifunction I/O		CLU3OUT	ADC0.18 CMP1P.7 CMP1N.7
13	P2.4	Multifunction I/O			ADC0.17 CMP1P.6 CMP1N.6
14	P2.3	Multifunction I/O	Yes	P2MAT.3 CLU1B.15 CLU2B.15 CLU3A.15	ADC0.16 CMP1P.5 CMP1N.5
15	P2.2	Multifunction I/O	Yes	P2MAT.2 CLU2OUT CLU1A.15 CLU2B.14 CLU3A.14	ADC0.15 CMP1P.4 CMP1N.4
16	P2.1	Multifunction I/O	Yes	P2MAT.1 I2C0_SCL CLU1B.14 CLU2A.15 CLU3B.15	ADC0.14 CMP1P.3 CMP1N.3
17	P2.0	Multifunction I/O	Yes	P2MAT.0 I2C0_SDA CLU1A.14 CLU2A.14 CLU3B.14	CMP1P.2 CMP1N.2

### 6.3 EFM8BB3x-QFN24 Pin Definitions

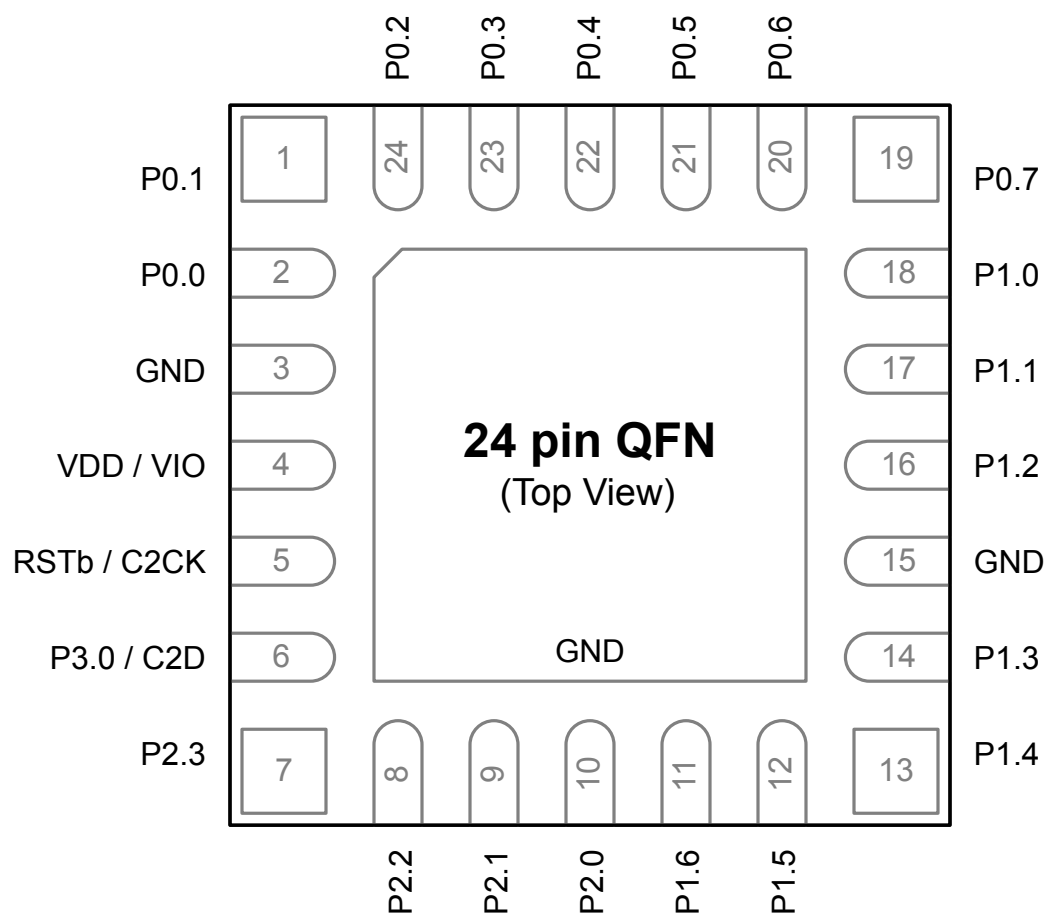


Figure 6.3. EFM8BB3x-QFN24 Pinout

Table 6.3. Pin Definitions for EFM8BB3x-QFN24

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
1	P0.1	Multifunction I/O	Yes	P0MAT.1 INT0.1 INT1.1 CLU0B.8 CLU2A.9 CLU3B.9	ADC0.0 CMP0P.0 CMP0N.0 AGND



Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
2	P0.2	Multifunction I/O	Yes	P0MAT.2 INT0.2 INT1.2 CLU0OUT CLU0A.9 CLU2B.8 CLU3A.8	XTAL1 ADC0.1 CMP0P.1 CMP0N.1
3	P0.1	Multifunction I/O	Yes	P0MAT.1 INT0.1 INT1.1 CLU0B.8 CLU2A.9 CLU3B.9	ADC0.0 CMP0P.0 CMP0N.0 AGND
4	P0.0	Multifunction I/O	Yes	P0MAT.0 INT0.0 INT1.0 CLU0A.8 CLU2A.8 CLU3B.8	VREF
5	GND	Ground			
6	VDD / VIO	Supply Power Input			
7	RSTb / C2CK	Active-low Reset / C2 Debug Clock			
8	P3.0 / C2D	Multifunction I/O / C2 Debug Data			
9	P2.3	Multifunction I/O	Yes	P2MAT.3 CLU1B.15 CLU2B.15 CLU3A.15	DAC3
10	P2.2	Multifunction I/O	Yes	P2MAT.2 CLU1A.15 CLU2B.14 CLU3A.14	DAC2

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
24	P0.4	Multifunction I/O	Yes	P0MAT.4 INT0.4 INT1.4 UART0_TX CLU0A.10 CLU1A.8 CLU3B.10	ADC0.2 CMP0P.2 CMP0N.2

## 7. QFN32 Package Specifications

### 7.1 QFN32 Package Dimensions

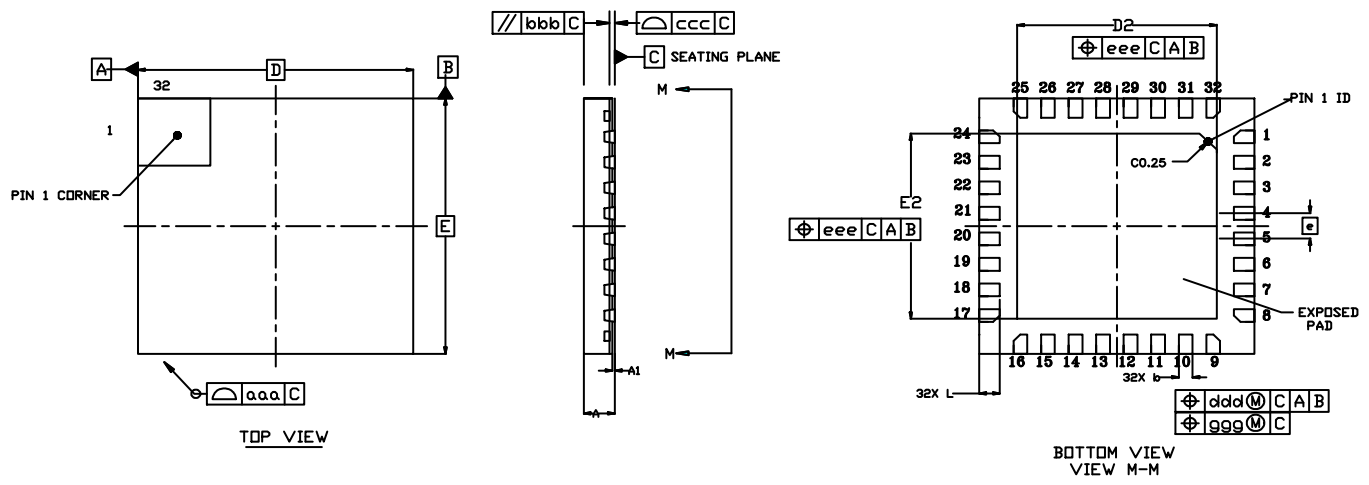


Figure 7.1. QFN32 Package Drawing

Table 7.1. QFN32 Package Dimensions

Dimension	Min	Typ	Max
A	0.45	0.50	0.55
A1	0.00	0.035	0.05
b	0.15	0.20	0.25
D	4.00 BSC.		
D2	2.80	2.90	3.00
e	0.40 BSC.		
E	4.00 BSC.		
E2	2.80	2.90	3.00
L	0.20	0.30	0.40
aaa	—	—	0.10
bbb	—	—	0.10
ccc	—	—	0.08
ddd	—	—	0.10
eee	—	—	0.10
ggg	—	—	0.05

## 7.2 QFN32 PCB Land Pattern

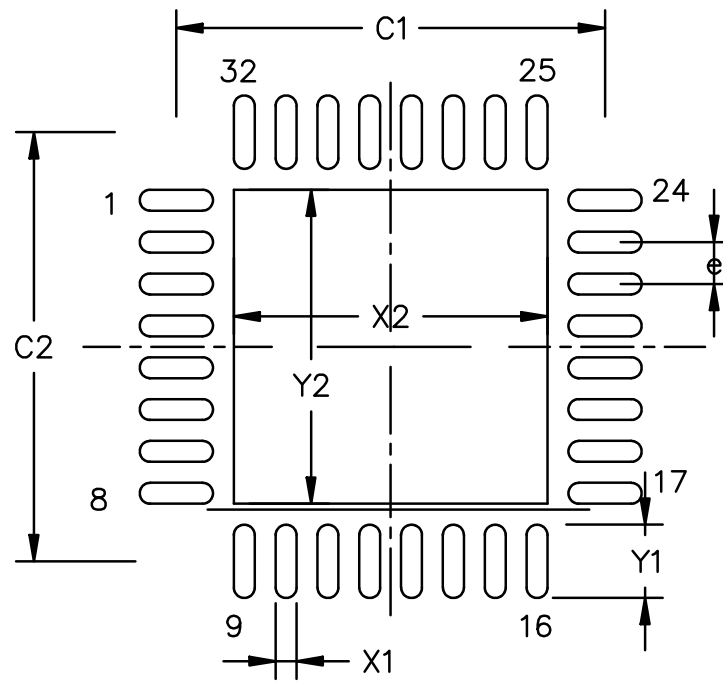


Figure 7.2. QFN32 PCB Land Pattern Drawing

Table 7.2. QFN32 PCB Land Pattern Dimensions

Dimension	Min	Max
C1	—	4.10
C2	—	4.10
X1	—	0.2
X2	—	3.0
Y1	—	0.7
Y2	—	3.0
e	—	0.4

## 9.2 QFN24 PCB Land Pattern

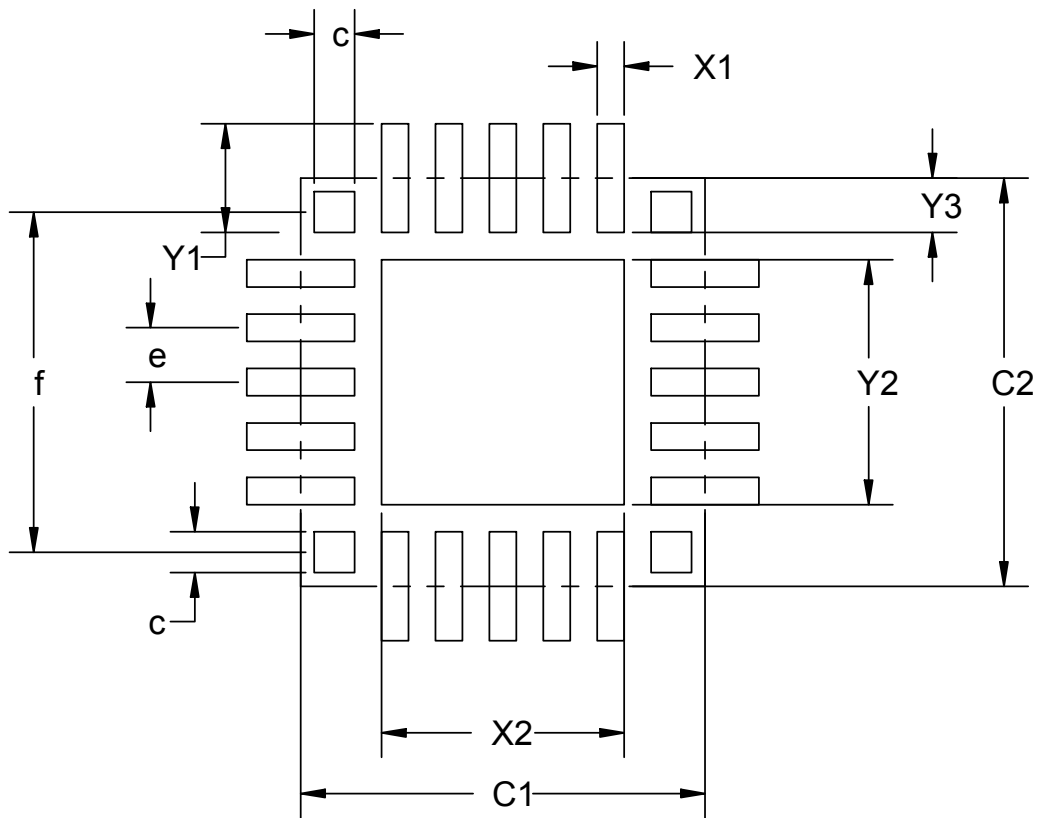


Figure 9.2. QFN24 PCB Land Pattern Drawing

Table 9.2. QFN24 PCB Land Pattern Dimensions

Dimension	Min	Max
C1		3.00
C2		3.00
e		0.4 REF
X1		0.20
X2		1.80
Y1		0.80
Y2		1.80
Y3		0.4
f		2.50 REF
c	0.25	0.35