

Welcome to [E-XFL.COM](https://www.e-xfl.com)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Not For New Designs
Core Processor	CIP-51 8051
Core Size	8-Bit
Speed	50MHz
Connectivity	I ² C, SMBus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	20
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2.25K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 12x10/12b SAR; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	24-VFQFN Exposed Pad
Supplier Device Package	24-QFN (3x3)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm8bb31f16i-b-qfn24

1. Feature List

The EFM8BB3 device family are fully integrated, mixed-signal system-on-a-chip MCUs. Highlighted features are listed below.

- Core:
 - Pipelined CIP-51 Core
 - Fully compatible with standard 8051 instruction set
 - 70% of instructions execute in 1-2 clock cycles
 - 50 MHz maximum operating frequency
- Memory:
 - Up to 64 kB flash memory (63 kB user-accessible), in-system re-programmable from firmware in 512-byte sectors
 - Up to 4352 bytes RAM (including 256 bytes standard 8051 RAM and 4096 bytes on-chip XRAM)
- Power:
 - Internal LDO regulator for CPU core voltage
 - Power-on reset circuit and brownout detectors
- I/O: Up to 29 total multifunction I/O pins:
 - Up to 25 pins 5 V tolerant under bias
 - Selectable state retention through reset events
 - Flexible peripheral crossbar for peripheral routing
 - 5 mA source, 12.5 mA sink allows direct drive of LEDs
- Clock Sources:
 - Internal 49 MHz oscillator with accuracy of $\pm 2\%$
 - Internal 24.5 MHz oscillator with $\pm 2\%$ accuracy
 - Internal 80 kHz low-frequency oscillator
 - External CMOS clock option
 - External crystal/RC Oscillator (up to 25 MHz)
- Analog:
 - 12/10-Bit Analog-to-Digital Converter (ADC)
 - Internal temperature sensor
 - 4 x 12-Bit Digital-to-Analog Converters (DAC)
 - 2 x Low-current analog comparators with adjustable reference
- Communications and Digital Peripherals:
 - 2 x UART, up to 3 Mbaud
 - SPI™ Master / Slave, up to 12 Mbps
 - SMBus™/I2C™ Master / Slave, up to 400 kbps
 - I2C High-Speed Slave, up to 3.4 Mbps
 - 16-bit CRC unit, supporting automatic CRC of flash at 256-byte boundaries
 - 4 Configurable Logic Units
- Timers/Counters and PWM:
 - 6-channel programmable counter array (PCA) supporting PWM, capture/compare, and frequency output modes
 - 6 x 16-bit general-purpose timers
 - Independent watchdog timer, clocked from the low frequency oscillator
- On-Chip, Non-Intrusive Debugging
 - Full memory and register inspection
 - Four hardware breakpoints, single-stepping
- Pre-programmed UART bootloader
- Temperature range -40 to 85 °C or -40 to 125 °C

With on-chip power-on reset, voltage supply monitor, watchdog timer, and clock oscillator, the EFM8BB3 devices are truly standalone system-on-a-chip solutions. The flash memory is reprogrammable in-circuit, providing nonvolatile data storage and allowing field upgrades of the firmware. The on-chip debugging interface (C2) allows non-intrusive (uses no on-chip resources), full speed, in-circuit debugging using the production MCU installed in the final application. This debug logic supports inspection and modification of memory and registers, setting breakpoints, single stepping, and run and halt commands. All analog and digital peripherals are fully functional while debugging. Device operation is specified from 2.2 V up to a 3.6 V supply. Devices are AEC-Q100 qualified and available in 4x4 mm 32-pin QFN, 3x3 mm 24-pin QFN, 32-pin QFP, or 24-pin QSOP packages. All package options are lead-free and RoHS compliant.

3.4 Clocking

The CPU core and peripheral subsystem may be clocked by both internal and external oscillator resources. By default, the system clock comes up running from the 24.5 MHz oscillator divided by 8.

The clock control system offers the following features:

- Provides clock to core and peripherals.
- 24.5 MHz internal oscillator (HFOSC0), accurate to $\pm 2\%$ over supply and temperature corners.
- 49 MHz internal oscillator (HFOSC1), accurate to $\pm 2\%$ over supply and temperature corners.
- 80 kHz low-frequency oscillator (LFOSC0).
- External RC, CMOS, and high-frequency crystal clock options (EXTCLK).
- Clock divider with eight settings for flexible clock scaling:
 - Divide the selected clock source by 1, 2, 4, 8, 16, 32, 64, or 128.
 - HFOSC0 and HFOSC1 include 1.5x pre-scalers for further flexibility.

3.5 Counters/Timers and PWM

Programmable Counter Array (PCA0)

The programmable counter array (PCA) provides multiple channels of enhanced timer and PWM functionality while requiring less CPU intervention than standard counter/timers. The PCA consists of a dedicated 16-bit counter/timer and one 16-bit capture/compare module for each channel. The counter/timer is driven by a programmable timebase that has flexible external and internal clocking options. Each capture/compare module may be configured to operate independently in one of five modes: Edge-Triggered Capture, Software Timer, High-Speed Output, Frequency Output, or Pulse-Width Modulated (PWM) Output. Each capture/compare module has its own associated I/O line (CEXn) which is routed through the crossbar to port I/O when enabled.

- 16-bit time base
- Programmable clock divisor and clock source selection
- Up to six independently-configurable channels
- 8, 9, 10, 11 and 16-bit PWM modes (center or edge-aligned operation)
- Output polarity control
- Frequency output mode
- Capture on rising, falling or any edge
- Compare function for arbitrary waveform generation
- Software timer (internal compare) mode
- Can accept hardware “kill” signal from comparator 0 or comparator 1

3.7 Analog

12/10-Bit Analog-to-Digital Converter (ADC0)

The ADC is a successive-approximation-register (SAR) ADC with 12- and 10-bit modes, integrated track-and hold and a programmable window detector. The ADC is fully configurable under software control via several registers. The ADC may be configured to measure different signals using the analog multiplexer. The voltage reference for the ADC is selectable between internal and external reference sources.

- Up to 20 external inputs
- Single-ended 12-bit and 10-bit modes
- Supports an output update rate of up to 350 ksps in 12-bit mode
- Channel sequencer logic with direct-to-XDATA output transfers
- Operation in a low power mode at lower conversion speeds
- Asynchronous hardware conversion trigger, selectable between software, external I/O and internal timer and configurable logic sources
- Output data window comparator allows automatic range checking
- Support for output data accumulation
- Conversion complete and window compare interrupts supported
- Flexible output data formatting
- Includes a fully-internal fast-settling 1.65 V reference and an on-chip precision 2.4 / 1.2 V reference, with support for using the supply as the reference, an external reference and signal ground
- Integrated temperature sensor

12-Bit Digital-to-Analog Converters (DAC0, DAC1, DAC2, DAC3)

The DAC modules are 12-bit Digital-to-Analog Converters with the capability to synchronize multiple outputs together. The DACs are fully configurable under software control. The voltage reference for the DACs is selectable between internal and external reference sources.

- Voltage output with 12-bit performance
- Supports an update rate of 200 ksps
- Hardware conversion trigger, selectable between software, external I/O and internal timer and configurable logic sources
- Outputs may be configured to persist through reset and maintain output state to avoid system disruption
- Multiple DAC outputs can be synchronized together
- DAC pairs (DAC0 and 1 or DAC2 and 3) support complementary output waveform generation
- Outputs may be switched between two levels according to state of configurable logic / PWM input trigger
- Flexible input data formatting
- Supports references from internal supply, on-chip precision reference, or external VREF pin

3.10 Bootloader

All devices come pre-programmed with a UART0 bootloader. This bootloader resides in the code security page, which is the last page of code flash; it can be erased if it is not needed.

The byte before the Lock Byte is the Bootloader Signature Byte. Setting this byte to a value of 0xA5 indicates the presence of the bootloader in the system. Any other value in this location indicates that the bootloader is not present in flash.

When a bootloader is present, the device will jump to the bootloader vector after any reset, allowing the bootloader to run. The bootloader then determines if the device should stay in bootload mode or jump to the reset vector located at 0x0000. When the bootloader is not present, the device will jump to the reset vector of 0x0000 after any reset.

More information about the bootloader protocol and usage can be found in *AN945: EFM8 Factory Bootloader User Guide*. Application notes can be found on the Silicon Labs website (www.silabs.com/8bit-appnotes) or within Simplicity Studio by using the [Application Notes] tile.

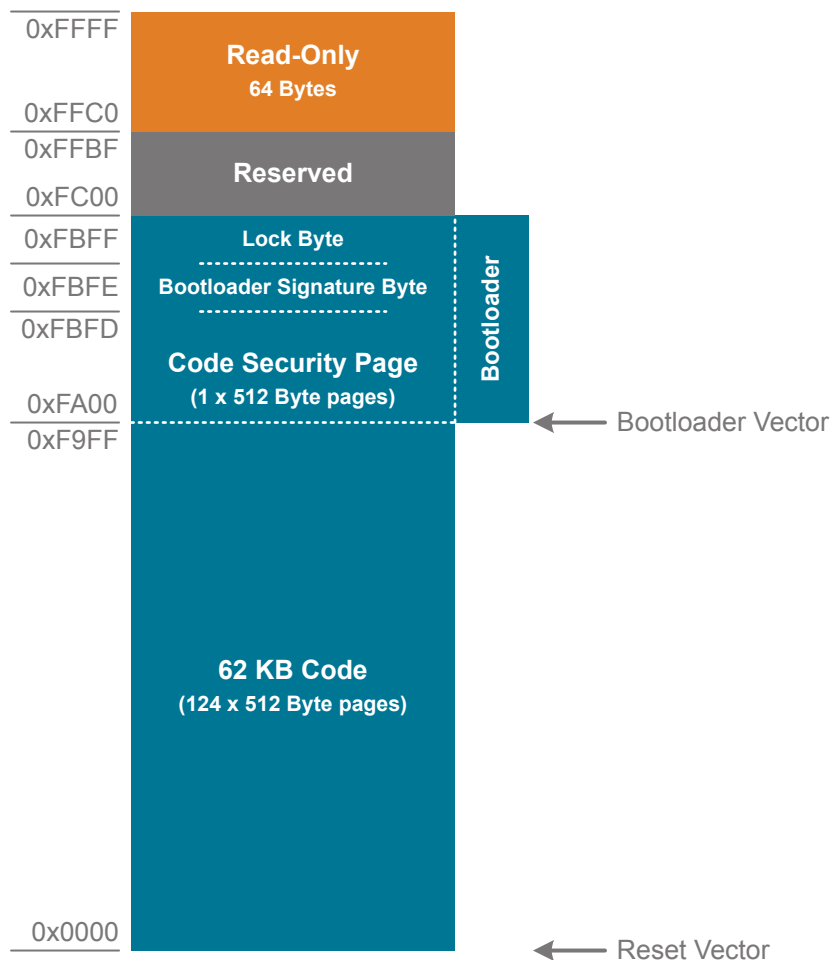


Figure 3.2. Flash Memory Map with Bootloader — 62.5 KB Devices

Table 3.2. Summary of Pins for Bootloader Communication

Bootloader	Pins for Bootload Communication
UART	TX – P0.4
	RX – P0.5

Table 3.3. Summary of Pins for Bootload Mode Entry

Device Package	Pin for Bootload Mode Entry
QFN32	P3.7 / C2D
QFP32	P3.7 / C2D
QFN24	P3.0 / C2D
QSOP24	P3.0 / C2D

4.1.8 Crystal Oscillator

Table 4.8. Crystal Oscillator

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Crystal Frequency	f_{XTAL}		0.02	—	25	MHz
Crystal Drive Current	I_{XTAL}	XFCN = 0	—	0.5	—	μA
		XFCN = 1	—	1.5	—	μA
		XFCN = 2	—	4.8	—	μA
		XFCN = 3	—	14	—	μA
		XFCN = 4	—	40	—	μA
		XFCN = 5	—	120	—	μA
		XFCN = 6	—	550	—	μA
		XFCN = 7	—	2.6	—	mA

4.1.9 ADC

Table 4.9. ADC

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Resolution	N _{bits}	12 Bit Mode	12			Bits
		10 Bit Mode	10			Bits
Throughput Rate (High Speed Mode)	f _S	10 Bit Mode	—	—	1.125	Msp/s
Throughput Rate (Low Power Mode)	f _S	12 Bit Mode	—	—	340	ksps
		10 Bit Mode	—	—	360	ksps
Tracking Time	t _{TRK}	High Speed Mode	230	—	—	ns
		Low Power Mode	450	—	—	ns
Power-On Time	t _{PWR}		1.2	—	—	μs
SAR Clock Frequency	f _{SAR}	High Speed Mode	—	—	18	MHz
		Low Power Mode	—	—	12.25	MHz
Conversion Time ¹	t _{CNV}	12-Bit Conversion, SAR Clock = 6.125 MHz, System Clock = 49 MHz	2.0			μs
		10-Bit Conversion, SAR Clock = 16.33 MHz, System Clock = 49 MHz	0.658			μs
Sample/Hold Capacitor	C _{SAR}	Gain = 1	—	5.2	—	pF
		Gain = 0.75	—	3.9	—	pF
		Gain = 0.5	—	2.6	—	pF
		Gain = 0.25	—	1.3	—	pF
Input Pin Capacitance	C _{IN}		—	20	—	pF
Input Mux Impedance	R _{MUX}		—	550	—	Ω
Voltage Reference Range	V _{REF}		1	—	V _{IO}	V
Input Voltage Range ²	V _{IN}		0	—	V _{REF} / Gain	V
Power Supply Rejection Ratio	PSRR _{ADC}	At 1 kHz	—	66	—	dB
		At 1 MHz	—	43	—	dB
DC Performance						

4.1.12 DACs

Table 4.12. DACs

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Resolution	N _{bits}		12			Bits
Throughput Rate	f _S		—	—	200	ksps
Integral Nonlinearity	INL	DAC0 and DAC2 T _A = -40 °C to 125 °C (I-grade parts only)	-11.5	-1.77 / 1.56	11.5	LSB
		DAC0 and DAC3 T _A = -40 °C to 125 °C (I-grade parts only)	-13.5	-2.73 / 1.11	13.5	LSB
Differential Nonlinearity	DNL		-1	—	1	LSB
Output Noise	V _{REF} = 2.4 V f _S = 0.1 Hz to 300 kHz		—	110	—	μV _{RMS}
Slew Rate	SLEW		—	±1	—	V/μs
Output Settling Time to 1% Full-scale	t _{SETTLE}	V _{OUT} change between 25% and 75% Full Scale	—	2.6	5	μs
Power-on Time	t _{PWR}		—	—	10	μs
Voltage Reference Range	V _{REF}		1.15	—	V _{DD}	V
Power Supply Rejection Ratio	PSRR	DC, V _{OUT} = 50% Full Scale	—	78	—	dB
Total Harmonic Distortion	THD	V _{OUT} = 10 kHz sine wave, 10% to 90%	54	—	—	dB
Offset Error	E _{OFF}	V _{REF} = 2.4 V	-8	0	8	LSB
Full-Scale Error	E _{FS}	V _{REF} = 2.4 V	-13	±5	13	LSB
External Load Impedance	R _{LOAD}		2	—	—	kΩ
External Load Capacitance ¹	C _{LOAD}		—	—	100	pF

Note:

1. No minimum external load capacitance is required. However, under low loading conditions, it is possible for the DAC output to glitch during start-up. If smooth start-up is required, the minimum loading capacitance at the pin should be a minimum of 10 pF.

5.2 Debug

The diagram below shows a typical connection diagram for the debug connections pins. The pin sharing resistors are only required if the functionality on the C2D (a GPIO pin) and the C2CK (RSTb) is routed to external circuitry. For example, if the RSTb pin is connected to an external switch with debouncing filter or if the GPIO sharing with the C2D pin is connected to an external circuit, the pin sharing resistors and connections to the debug adapter must be placed on the hardware. Otherwise, these components and connections can be omitted.

For more information on debug connections, see the example schematics and information available in AN127: "Pin Sharing Techniques for the C2 Interface." Application notes can be found on the Silicon Labs website (<http://www.silabs.com/8bit-appnotes>) or in Simplicity Studio.

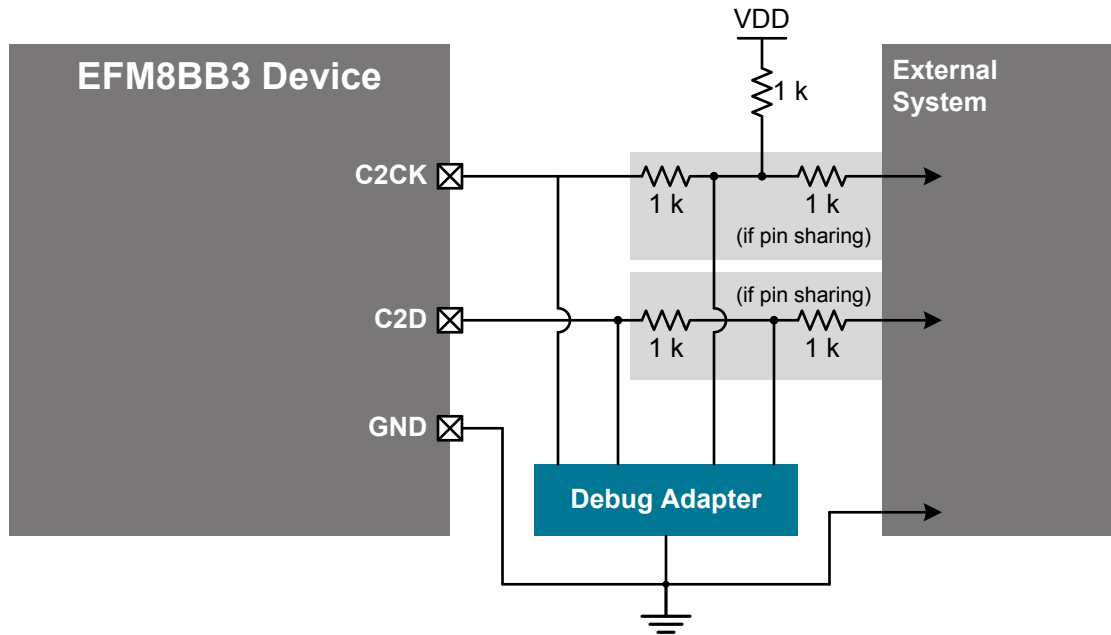


Figure 5.2. Debug Connection Diagram

5.3 Other Connections

Other components or connections may be required to meet the system-level requirements. Application Note AN203: "8-bit MCU Printed Circuit Board Design Notes" contains detailed information on these connections. Application Notes can be accessed on the Silicon Labs website (www.silabs.com/8bit-appnotes).

6. Pin Definitions

6.1 EFM8BB3x-QFN32 Pin Definitions

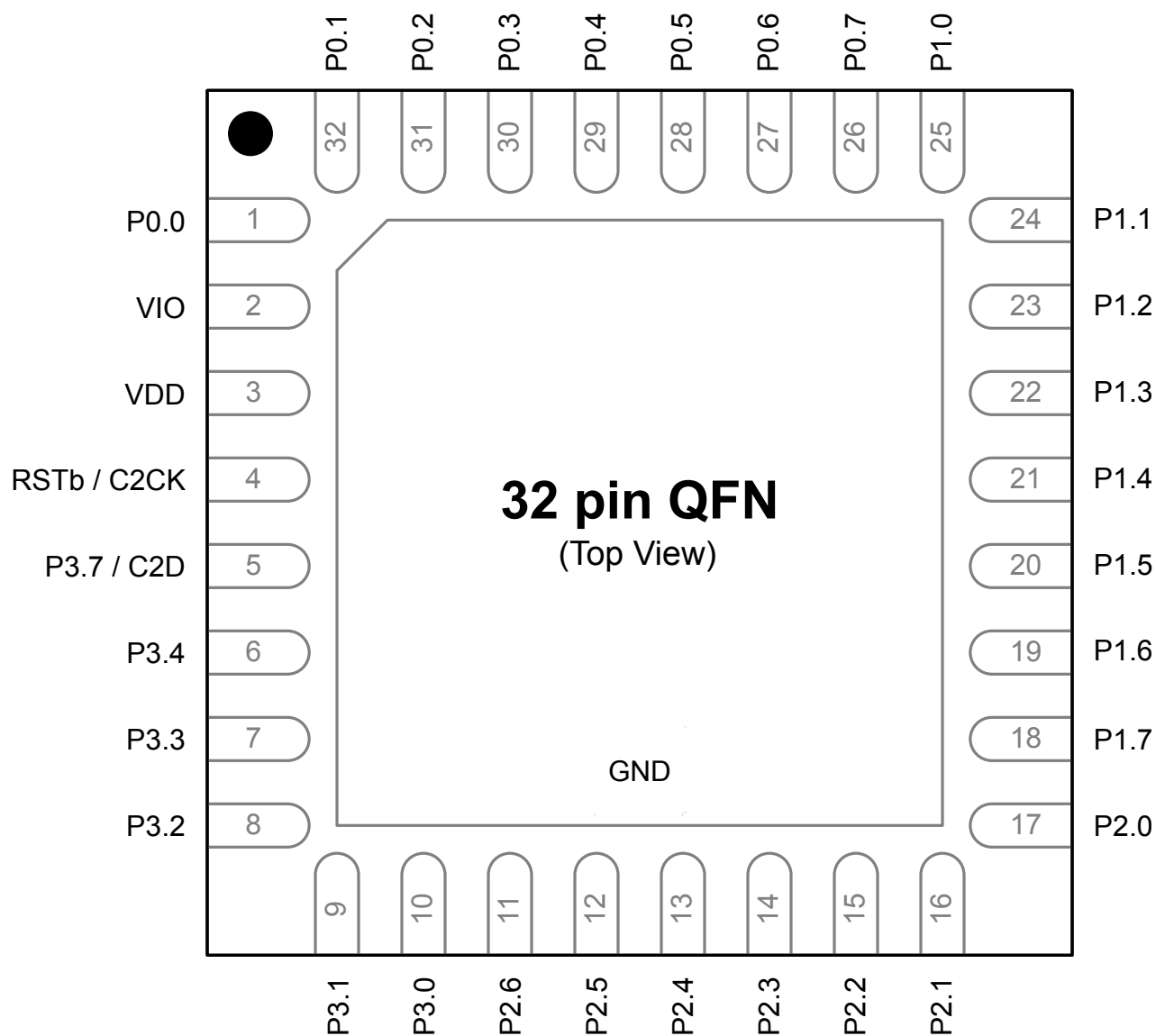


Figure 6.1. EFM8BB3x-QFN32 Pinout

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
18	P1.7	Multifunction I/O	Yes	P1MAT.7 CLU0B.15 CLU1B.13 CLU2A.13	ADC0.13 CMP0P.9 CMP0N.9
19	P1.6	Multifunction I/O	Yes	P1MAT.6 CLU0A.15 CLU1B.12 CLU2A.12	ADC0.12
20	P1.5	Multifunction I/O	Yes	P1MAT.5 CLU0B.14 CLU1A.13 CLU2B.13	ADC0.11
21	P1.4	Multifunction I/O	Yes	P1MAT.4 CLU0A.14 CLU1A.12 CLU2B.12	ADC0.10
22	P1.3	Multifunction I/O	Yes	P1MAT.3 CLU0B.13 CLU1B.11 CLU2B.11 CLU3A.13	ADC0.9
23	P1.2	Multifunction I/O	Yes	P1MAT.2 CLU0A.13 CLU1A.11 CLU2B.10 CLU3A.12	ADC0.8 CMP0P.8 CMP0N.8
24	P1.1	Multifunction I/O	Yes	P1MAT.1 CLU0B.12 CLU1B.10 CLU2A.11 CLU3B.13	ADC0.7 CMP0P.7 CMP0N.7

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
25	P1.0	Multifunction I/O	Yes	P1MAT.0 CLU1OUT CLU0A.12 CLU1A.10 CLU2A.10 CLU3B.12	ADC0.6 CMP0P.6 CMP0N.6 CMP1P.1 CMP1N.1
26	P0.7	Multifunction I/O	Yes	P0MAT.7 INT0.7 INT1.7 CLU0B.11 CLU1B.9 CLU3A.11	ADC0.5 CMP0P.5 CMP0N.5 CMP1P.0 CMP1N.0
27	P0.6	Multifunction I/O	Yes	P0MAT.6 CNVSTR INT0.6 INT1.6 CLU0A.11 CLU1B.8 CLU3A.10	ADC0.4 CMP0P.4 CMP0N.4
28	P0.5	Multifunction I/O	Yes	P0MAT.5 INT0.5 INT1.5 UART0_RX CLU0B.10 CLU1A.9 CLU3B.11	ADC0.3 CMP0P.3 CMP0N.3
29	P0.4	Multifunction I/O	Yes	P0MAT.4 INT0.4 INT1.4 UART0_TX CLU0A.10 CLU1A.8 CLU3B.10	ADC0.2 CMP0P.2 CMP0N.2

6.3 EFM8BB3x-QFN24 Pin Definitions

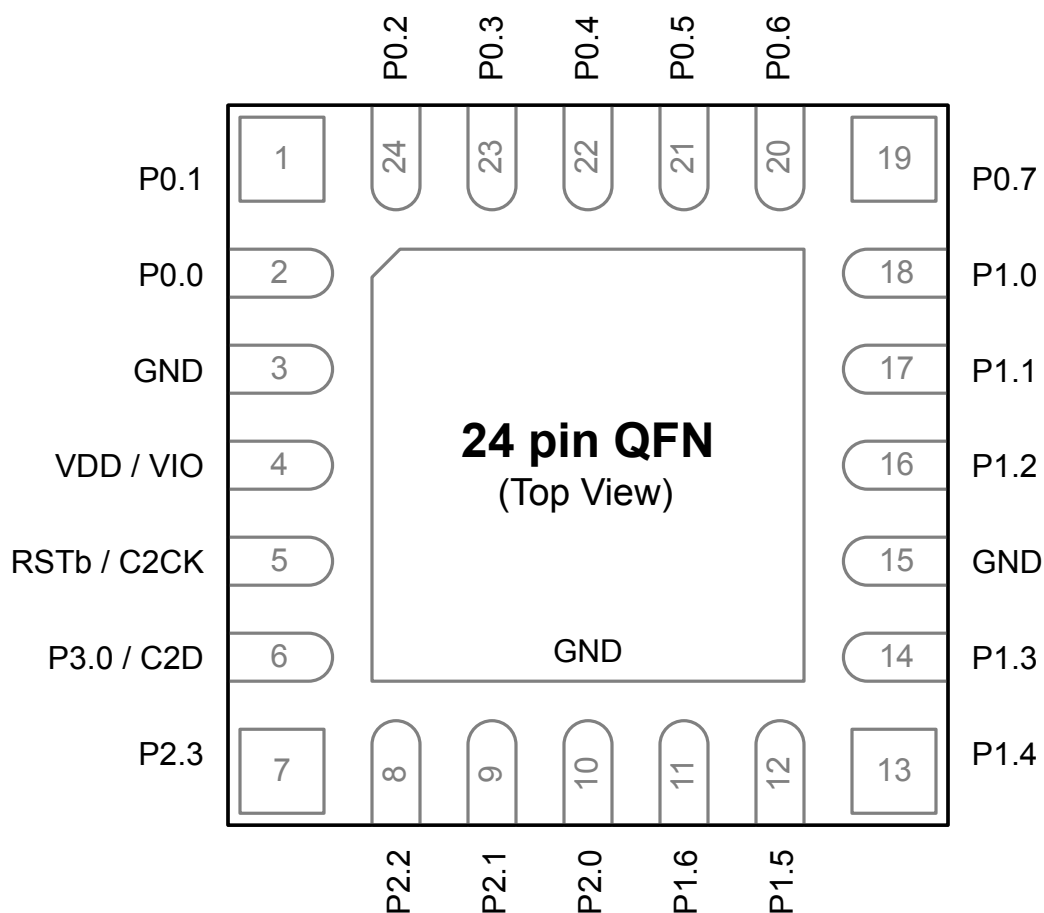


Figure 6.3. EFM8BB3x-QFN24 Pinout

Table 6.3. Pin Definitions for EFM8BB3x-QFN24

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
1	P0.1	Multifunction I/O	Yes	P0MAT.1 INT0.1 INT1.1 CLU0B.8 CLU2A.9 CLU3B.9	ADC0.0 CMP0P.0 CMP0N.0 AGND

7. QFN32 Package Specifications

7.1 QFN32 Package Dimensions

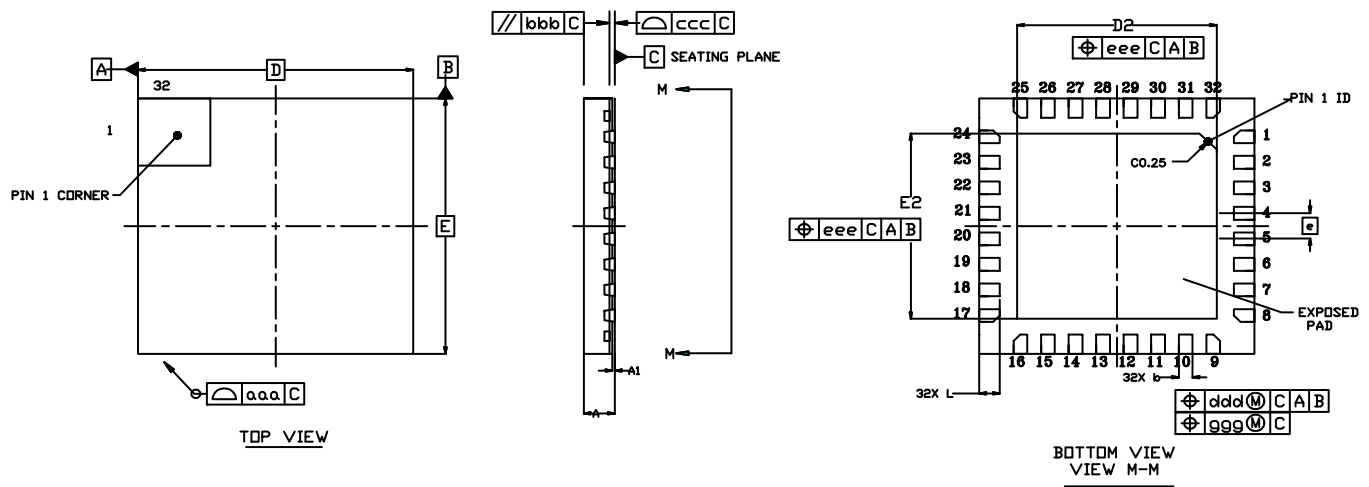


Figure 7.1. QFN32 Package Drawing

Table 7.1. QFN32 Package Dimensions

Dimension	Min	Typ	Max
A	0.45	0.50	0.55
A1	0.00	0.035	0.05
b	0.15	0.20	0.25
D	4.00 BSC.		
D2	2.80	2.90	3.00
e	0.40 BSC.		
E	4.00 BSC.		
E2	2.80	2.90	3.00
L	0.20	0.30	0.40
aaa	—	—	0.10
bbb	—	—	0.10
ccc	—	—	0.08
ddd	—	—	0.10
eee	—	—	0.10
ggg	—	—	0.05

Dimension	Min	Max
Note: <ol style="list-style-type: none"> 1. All dimensions shown are in millimeters (mm) unless otherwise noted. 2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification. 3. This Land Pattern Design is based on the IPC-7351 guidelines. 4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05mm. 5. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad. 6. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release. 7. The stencil thickness should be 0.125 mm (5 mils). 8. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads. 9. A 2 x 2 array of 1.10 mm square openings on a 1.30 mm pitch should be used for the center pad. 10. A No-Clean, Type-3 solder paste is recommended. 11. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components. 		

7.3 QFN32 Package Marking



Figure 7.3. QFN32 Package Marking

The package marking consists of:

- P P P P P P P P – The part number designation.
- T T T T T T – A trace or manufacturing code.
- Y Y – The last 2 digits of the assembly year.
- W W – The 2-digit workweek when the device was assembled.
- # – The device revision (A, B, etc.).

Dimension	Min	Typ	Max
aaa	0.20		
bbb	0.20		
ccc	0.10		
ddd	0.20		
theta	0°	3.5°	7°

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC outline MS-026.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

8.3 QFP32 Package Marking

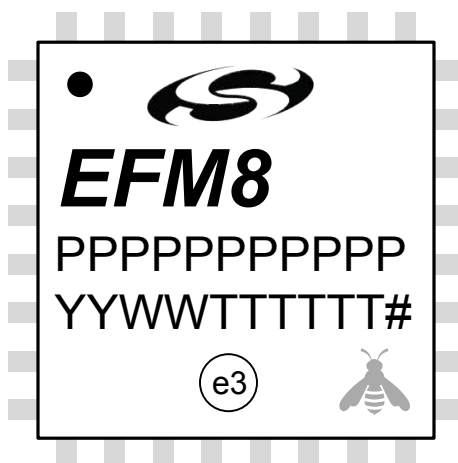


Figure 8.3. QFP32 Package Marking

The package marking consists of:

- P P P P P P P P – The part number designation.
- T T T T T T – A trace or manufacturing code.
- Y Y – The last 2 digits of the assembly year.
- W W – The 2-digit workweek when the device was assembled.
- # – The device revision (A, B, etc.).

10.3 QSOP24 Package Marking



Figure 10.3. QSOP24 Package Marking

The package marking consists of:

- P P P P P P P P – The part number designation.
- T T T T T T – A trace or manufacturing code.
- Y Y – The last 2 digits of the assembly year.
- W W – The 2-digit workweek when the device was assembled.
- # – The device revision (A, B, etc.).

11. Revision History

11.1 Revision 1.01

October 21st, 2016

Updated [Figure 2.1 EFM8BB3 Part Numbering on page 2](#) to include the I-grade description.

Updated QFN24 center pad stencil description.

11.2 Revision 1.0

September 6th, 2016

Filled in all TBD values in [4. Electrical Specifications](#).

Added a note regarding which DACs are available to [Table 2.1 Product Selection Guide on page 2](#).

Added specifications for [4.1.16 SMBus](#).

Added bootloader pinout information to [3.10 Bootloader](#).

Added CRC Calculation Time to [4.1.4 Flash Memory](#).

11.3 Revision 0.4

May 12th, 2016

Filled in TBD values for DAC Integral Nonlinearity in [Table 4.12 DACs on page 26](#).

Added I-grade devices.

Adjusted the Total Current Sunk into Supply Pin and Total Current Sourced out of Ground Pin specifications in [4.3 Absolute Maximum Ratings](#).

Added Operating Junction Temperature specification to [4.3 Absolute Maximum Ratings](#).

11.4 Revision 0.3

February 10th, 2016

Added EFM8831F16G-A-QFN24 to [Table 2.1 Product Selection Guide on page 2](#).

Updated [Figure 5.2 Debug Connection Diagram on page 34](#) to move the pull-up resistor on C2D / RSTb to after the series resistor instead of before.

Added mention of the pre-programmed bootloader in [1. Feature List](#).

Added a reference to *AN945: EFM8 Factory Bootloader User Guide* in [3.10 Bootloader](#).

Updated all part numbers to revision B.

Adjusted C1, C2, X2, Y2, and Y1 maximums for [7.2 QFN32 PCB Land Pattern](#).

Adjusted package markings for QFN32 and QSOP24 packages.

Filled in TBD minimum and maximum values for DAC Differential Nonlinearity in [Table 4.12 DACs on page 26](#).

11.5 Revision 0.2

Added information on the bootloader to [3.10 Bootloader](#).

Updated some characterization TBD values.

11.6 Revision 0.1

Initial release.

Table of Contents

1. Feature List	1
2. Ordering Information	2
3. System Overview	4
3.1 Introduction	4
3.2 Power	5
3.3 I/O	5
3.4 Clocking	6
3.5 Counters/Timers and PWM	6
3.6 Communications and Other Digital Peripherals	7
3.7 Analog	10
3.8 Reset Sources	11
3.9 Debugging	11
3.10 Bootloader	12
4. Electrical Specifications	14
4.1 Electrical Characteristics	14
4.1.1 Recommended Operating Conditions	14
4.1.2 Power Consumption	15
4.1.3 Reset and Supply Monitor	17
4.1.4 Flash Memory	18
4.1.5 Power Management Timing	18
4.1.6 Internal Oscillators	19
4.1.7 External Clock Input	19
4.1.8 Crystal Oscillator	20
4.1.9 ADC	21
4.1.10 Voltage Reference	24
4.1.11 Temperature Sensor	25
4.1.12 DACs	26
4.1.13 Comparators	27
4.1.14 Configurable Logic	28
4.1.15 Port I/O	29
4.1.16 SMBus	30
4.2 Thermal Conditions	31
4.3 Absolute Maximum Ratings	32
5. Typical Connection Diagrams	33
5.1 Power	33
5.2 Debug	34
5.3 Other Connections	34
6. Pin Definitions	35
6.1 EFM8BB3x-QFN32 Pin Definitions	35