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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Not For New Designs
Core Processor	CIP-51 8051
Core Size	8-Bit
Speed	50MHz
Connectivity	I ² C, SMBus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	29
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2.25К х 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 20x10/12b SAR; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	32-UFQFN Exposed Pad
Supplier Device Package	32-QFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm8bb31f16i-b-qfn32r

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2. Ordering Information



Figure 2.1. EFM8BB3 Part Numbering

All EFM8BB3 family members have the following features:

- · CIP-51 Core running up to 49 MHz
- Three Internal Oscillators (49 MHz, 24.5 MHz and 80 kHz)
- SMBus
- I2C Slave
- SPI
- 2 UARTs
- · 6-Channel Programmable Counter Array (PWM, Clock Generation, Capture/Compare)
- · Six 16-bit Timers
- Four Configurable Logic Units
- 12-bit Analog-to-Digital Converter with integrated multiplexer, voltage reference, temperature sensor, channel sequencer, and direct-to-XRAM data transfer
- Two Analog Comparators
- 16-bit CRC Unit
- AEC-Q100 qualified
- Pre-loaded UART bootloader

In addition to these features, each part number in the EFM8BB3 family has a set of features that vary across the product line. The product selection guide shows the features available on each family member.

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Ordering Part Number	Flash Memory (kB)	RAM (Bytes)	Digital Port I/Os (Total)	Voltage DACs	ADC0 Channels	Comparator 0 Inputs	Comparator 1 Inputs	Pb-free (RoHS Compliant)	Temperature Range	Package
EFM8BB31F64G-B-QFN32	64	4352	29	4	20	10	9	Yes	-40 to +85 °C	QFN32
EFM8BB31F64G-B-QFP32	64	4352	28	4	20	10	9	Yes	-40 to +85 °C	QFP32
EFM8BB31F64G-B-QFN24	64	4352	20	4	12	6	6	Yes	-40 to +85 °C	QFN24
				•		•		•		

Table 2.1. Product Selection Guide

Timers (Timer 0, Timer 1, Timer 2, Timer 3, Timer 4, and Timer 5)

Several counter/timers are included in the device: two are 16-bit counter/timers compatible with those found in the standard 8051, and the rest are 16-bit auto-reload timers for timing peripherals or for general purpose use. These timers can be used to measure time intervals, count external events and generate periodic interrupt requests. Timer 0 and Timer 1 are nearly identical and have four primary modes of operation. The other timers offer both 16-bit and split 8-bit timer functionality with auto-reload and capture capabilities.

Timer 0 and Timer 1 include the following features:

- Standard 8051 timers, supporting backwards-compatibility with firmware and hardware.
- Clock sources include SYSCLK, SYSCLK divided by 12, 4, or 48, the External Clock divided by 8, or an external pin.
- · 8-bit auto-reload counter/timer mode
- 13-bit counter/timer mode
- 16-bit counter/timer mode
- Dual 8-bit counter/timer mode (Timer 0)

Timer 2, Timer 3, Timer 4, and Timer 5 are 16-bit timers including the following features:

- · Clock sources for all timers include SYSCLK, SYSCLK divided by 12, or the External Clock divided by 8
- · LFOSC0 divided by 8 may be used to clock Timer 3 and Timer 4 in active or suspend/snooze power modes
- Timer 4 is a low-power wake source, and can be chained together with Timer 3
- 16-bit auto-reload timer mode
- Dual 8-bit auto-reload timer mode
- · External pin capture
- LFOSC0 capture
- Comparator 0 capture
- Configurable Logic output capture

Watchdog Timer (WDT0)

The device includes a programmable watchdog timer (WDT) running off the low-frequency oscillator. A WDT overflow forces the MCU into the reset state. To prevent the reset, the WDT must be restarted by application software before overflow. If the system experiences a software or hardware malfunction preventing the software from restarting the WDT, the WDT overflows and causes a reset. Following a reset, the WDT is automatically enabled and running with the default maximum time interval. If needed, the WDT can be disabled by system software or locked on to prevent accidental disabling. Once locked, the WDT cannot be disabled until the next system reset. The state of the RST pin is unaffected by this reset.

The Watchdog Timer has the following features:

- · Programmable timeout interval
- · Runs from the low-frequency oscillator
- · Lock-out feature to prevent any modification until a system reset

3.6 Communications and Other Digital Peripherals

Universal Asynchronous Receiver/Transmitter (UART0)

UART0 is an asynchronous, full duplex serial port offering modes 1 and 3 of the standard 8051 UART. Enhanced baud rate support allows a wide range of clock sources to generate standard baud rates. Received data buffering allows UART0 to start reception of a second incoming data byte before software has finished reading the previous data byte.

The UART module provides the following features:

- · Asynchronous transmissions and receptions.
- Baud rates up to SYSCLK/2 (transmit) or SYSCLK/8 (receive).
- 8- or 9-bit data.
- Automatic start and stop generation.
- · Single-byte FIFO on transmit and receive.

4.1.10 Voltage Reference

Table 4	4.10.	Voltage	Reference
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Parameter	Symbol	Test Condition	Min	Тур	Max	Unit			
Internal Fast Settling Reference									
Output Voltage	V _{REFFS}		1.62	1.65	1.68	V			
(Full Temperature and Supply Range)									
Temperature Coefficient	TC _{REFFS}			50	_	ppm/°C			
Turn-on Time	t _{REFFS}				1.5	μs			
Power Supply Rejection	PSRR _{REF} FS		_	400	_	ppm/V			
On-chip Precision Reference									
Valid Supply Range	V _{DD}	1.2 V Output	2.2	—	3.6	V			
		2.4 V Output	2.7	—	3.6	V			
Output Voltage	V _{REFP}	1.2 V Output, V _{DD} = 3.3 V, T = 25 °C	1.195	1.2	1.205	V			
		1.2 V Output	1.18	1.2	1.22	V			
		2.4 V Output, V _{DD} = 3.3 V, T = 25 °C	2.39	2.4	2.41	V			
		2.4 V Output	2.36	2.4	2.44	V			
Turn-on Time, settling to 0.5 LSB	t _{VREFP}	4.7 μF tantalum + 0.1 μF ceramic bypass on VREF pin	—	3	_	ms			
		0.1 μ F ceramic bypass on VREF pin	_	100	_	μs			
Load Regulation	LR _{VREFP}	VREF = 2.4 V, Load = 0 to 200 μ A to GND	_	8	_	μV/μΑ			
		VREF = 1.2 V, Load = 0 to 200 μ A to GND		5	_	μV/μΑ			
Load Capacitor	C _{VREFP}	Load = 0 to 200 µA to GND	0.1	_	_	μF			
Short-circuit current	ISC _{VREFP}		_	_	8	mA			
Power Supply Rejection	PSRR _{VRE} FP			75	_	dB			
External Reference	,	1		1					
Input Current	I _{EXTREF}	ADC Sample Rate = 800 ksps; VREF = 3.0 V	_	5	_	μA			

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
Negative Hysteresis	HYS _{CP-}	CPHYN = 00	—	-1.5	—	mV
Mode 3 (CPMD = 11)		CPHYN = 01	_	-4	—	mV
		CPHYN = 10	—	-8	—	mV
		CPHYN = 11	—	-16	_	mV
Input Range (CP+ or CP-)	V _{IN}		-0.25	_	V _{IO} +0.25	V
Input Pin Capacitance	C _{CP}		_	7.5	_	pF
Internal Reference DAC Resolution	N _{bits}			6		bits
Common-Mode Rejection Ratio	CMRR _{CP}		—	70	_	dB
Power Supply Rejection Ratio	PSRR _{CP}		_	72	_	dB
Input Offset Voltage	V _{OFF}	T _A = 25 °C	-10	0	10	mV
Input Offset Tempco	TC _{OFF}		_	3.5	_	μV/°

4.1.14 Configurable Logic

Table 4.14. Configurable Logic

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
Propagation Delay	t _{DLY}	Through single CLU	—	_	35.3	ns
		Using an external pin				
		Through single CLU	_	3	—	ns
		Using an internal connection				
Clocking Frequency	F _{CLK}	1 or 2 CLUs Cascaded	—	—	73.5	MHz
		3 or 4 CLUs Cascaded		_	36.75	MHz

Pin	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
23	P1.2	Multifunction I/O	Yes	P1MAT.2	ADC0.8
				CLU0A.13	CMP0P.8
				CLU1A.11	CMP0N.8
				CLU2B.10	
				CLU3A.12	
24	P1.1	Multifunction I/O	Yes	P1MAT.1	ADC0.7
				CLU0B.12	CMP0P.7
				CLU1B.10	CMP0N.7
				CLU2A.11	
				CLU3B.13	
25	P1.0	Multifunction I/O	Yes	P1MAT.0	ADC0.6
				CLU1OUT	CMP0P.6
				CLU0A.12	CMP0N.6
				CLU1A.10	CMP1P.1
				CLU2A.10	CMP1N.1
				CLU3B.12	
26	P0.7	Multifunction I/O	Yes	P0MAT.7	ADC0.5
				INT0.7	CMP0P.5
				INT1.7	CMP0N.5
				CLU0B.11	CMP1P.0
				CLU1B.9	CMP1N.0
				CLU3A.11	
27	P0.6	Multifunction I/O	Yes	P0MAT.6	ADC0.4
				CNVSTR	CMP0P.4
				INT0.6	CMP0N.4
				INT1.6	
				CLU0A.11	
				CLU1B.8	
				CLU3A.10	
28	P0.5	Multifunction I/O	Yes	P0MAT.5	ADC0.3
				INT0.5	CMP0P.3
				INT1.5	CMP0N.3
				UART0_RX	
				CLU0B.10	
				CLU1A.9	
				CLU3B.11	

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
18	P1.7	Multifunction I/O	Yes	P1MAT.7	ADC0.13
				CLU0B.15	CMP0P.9
				CLU1B.13	CMP0N.9
				CLU2A.13	
19	P1.6	Multifunction I/O	Yes	P1MAT.6	ADC0.12
				CLU0A.15	
				CLU1B.12	
				CLU2A.12	
20	P1.5	Multifunction I/O	Yes	P1MAT.5	ADC0.11
				CLU0B.14	
				CLU1A.13	
				CLU2B.13	
21	P1.4	Multifunction I/O	Yes	P1MAT.4	ADC0.10
				CLU0A.14	
				CLU1A.12	
				CLU2B.12	
22	P1.3	Multifunction I/O	Yes	P1MAT.3	ADC0.9
				CLU0B.13	
				CLU1B.11	
				CLU2B.11	
				CLU3A.13	
23	P1.2	Multifunction I/O	Yes	P1MAT.2	ADC0.8
				CLU0A.13	CMP0P.8
				CLU1A.11	CMP0N.8
				CLU2B.10	
				CLU3A.12	
24	P1.1	Multifunction I/O	Yes	P1MAT.1	ADC0.7
				CLU0B.12	CMP0P.7
				CLU1B.10	CMP0N.7
				CLU2A.11	
				CLU3B.13	

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
25	P1.0	Multifunction I/O	Yes	P1MAT.0	ADC0.6
				CLU1OUT	CMP0P.6
				CLU0A.12	CMP0N.6
				CLU1A.10	CMP1P.1
				CLU2A.10	CMP1N.1
				CLU3B.12	
26	P0.7	Multifunction I/O	Yes	P0MAT.7	ADC0.5
				INT0.7	CMP0P.5
				INT1.7	CMP0N.5
				CLU0B.11	CMP1P.0
				CLU1B.9	CMP1N.0
				CLU3A.11	
27	P0.6	Multifunction I/O	Yes	P0MAT.6	ADC0.4
				CNVSTR	CMP0P.4
				INT0.6	CMP0N.4
				INT1.6	
				CLU0A.11	
				CLU1B.8	
				CLU3A.10	
28	P0.5	Multifunction I/O	Yes	P0MAT.5	ADC0.3
				INT0.5	CMP0P.3
				INT1.5	CMP0N.3
				UART0_RX	
				CLU0B.10	
				CLU1A.9	
				CLU3B.11	
29	P0.4	Multifunction I/O	Yes	P0MAT.4	ADC0.2
				INT0.4	CMP0P.2
				INT1.4	CMP0N.2
				UART0_TX	
				CLU0A.10	
				CLU1A.8	
				CLU3B.10	

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
2	P0.0	Multifunction I/O	Yes	P0MAT.0	VREF
				INT0.0	
				INT1.0	
				CLU0A.8	
				CLU2A.8	
				CLU3B.8	
3	GND	Ground			
4	VDD / VIO	Supply Power Input			
5	RSTb /	Active-low Reset /			
	C2CK	C2 Debug Clock			
6	P3.0 /	Multifunction I/O /			
	C2D	C2 Debug Data			
7	P2.3	Multifunction I/O	Yes	P2MAT.3	DAC3
				CLU1B.15	
				CLU2B.15	
				CLU3A.15	
8	P2.2	Multifunction I/O	Yes	P2MAT.2	DAC2
				CLU1A.15	
				CLU2B.14	
				CLU3A.14	
9	P2.1	Multifunction I/O	Yes	P2MAT.1	DAC1
				CLU1B.14	
				CLU2A.15	
				CLU3B.15	
10	P2.0	Multifunction I/O	Yes	P2MAT.0	DAC0
				CLU1A.14	
				CLU2A.14	
				CLU3B.14	
11	P1.6	Multifunction I/O	Yes	P1MAT.6	ADC0.11
				CLU3OUT	CMP1P.5
				CLU0A.15	CMP1N.5
				CLU1B.12	
				CLU2A.12	

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
19	P0.7	Multifunction I/O	Yes	P0MAT.7	ADC0.5
				INT0.7	CMP0P.5
				INT1.7	CMP0N.5
				CLU1OUT	CMP1P.1
				CLU0B.11	CMP1N.1
				CLU1B.9	
				CLU3A.11	
20	P0.6	Multifunction I/O	Yes	P0MAT.6	ADC0.4
				CNVSTR	CMP0P.4
				INT0.6	CMP0N.4
				INT1.6	CMP1P.0
				CLU0A.11	CMP1N.0
				CLU1B.8	
				CLU3A.10	
21	P0.5	Multifunction I/O	Yes	P0MAT.5	ADC0.3
				INT0.5	CMP0P.3
				INT1.5	CMP0N.3
				UART0_RX	
				CLU0B.10	
				CLU1A.9	
				CLU3B.11	
22	P0.4	Multifunction I/O	Yes	P0MAT.4	ADC0.2
				INT0.4	CMP0P.2
				INT1.4	CMP0N.2
				UART0_TX	
				CLU0A.10	
				CLU1A.8	
				CLU3B.10	
23	P0.3	Multifunction I/O	Yes	P0MAT.3	XTAL2
				EXTCLK	
				INT0.3	
				INT1.3	
				CLU0B.9	
				CLU2B.9	
				CLU3A.9	

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
18	P1.2	Multifunction I/O	Yes	P1MAT.2	ADC0.8
				CLU0A.13	
				CLU1A.11	
				CLU2B.10	
				CLU3A.12	
19	P1.1	Multifunction I/O	Yes	P1MAT.1	ADC0.7
				CLU0B.12	
				CLU1B.10	
				CLU2A.11	
				CLU3B.13	
20	P1.0	Multifunction I/O	Yes	P1MAT.0	ADC0.6
				CLU0A.12	
				CLU1A.10	
				CLU2A.10	
				CLU3B.12	
21	P0.7	Multifunction I/O	Yes	P0MAT.7	ADC0.5
				INT0.7	CMP0P.5
				INT1.7	CMP0N.5
				CLU1OUT	CMP1P.1
				CLU0B.11	CMP1N.1
				CLU1B.9	
				CLU3A.11	
22	P0.6	Multifunction I/O	Yes	P0MAT.6	ADC0.4
				CNVSTR	CMP0P.4
				INT0.6	CMP0N.4
				INT1.6	CMP1P.0
				CLU0A.11	CMP1N.0
				CLU1B.8	
				CLU3A.10	
23	P0.5	Multifunction I/O	Yes	P0MAT.5	ADC0.3
				INT0.5	CMP0P.3
				INT1.5	CMP0N.3
				UART0_RX	
				CLU0B.10	
				CLU1A.9	
				CLU3B.11	

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
24	P0.4	Multifunction I/O	Yes	P0MAT.4	ADC0.2
				INT0.4	CMP0P.2
				INT1.4	CMP0N.2
				UART0_TX	
				CLU0A.10	
				CLU1A.8	
				CLU3B.10	

7. QFN32 Package Specifications

7.1 QFN32 Package Dimensions



Figure 7.1. QFN32 Package Drawing

Dimension	Min	Тур	Мах
A	0.45	0.50	0.55
A1	0.00	0.035	0.05
b	0.15	0.20	0.25
D		4.00 BSC.	
D2	2.80	2.90	3.00
е	0.40 BSC.		
E	4.00 BSC.		
E2	2.80	2.90	3.00
L	0.20	0.30	0.40
ааа		_	0.10
bbb	_	—	0.10
ССС		—	0.08
ddd	_	_	0.10
eee	—	—	0.10
999			0.05

Table 7.1. QFN32 Package Dimensions

Dimension	Min	Тур	Мах	
Note:				
1. All dimensions shown are in millimeters (mm) unless otherwise noted.				
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.				
3. This drawing conforms to JEDEC Solid State Outline MO-220.				
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.				

Dimension	Min	Мах			
Note:					
1. All dimensions shown are in millimeters	(mm) unless otherwise noted.				
2. Dimensioning and Tolerancing is per the	ANSI Y14.5M-1994 specification.				
3. This Land Pattern Design is based on th	3. This Land Pattern Design is based on the IPC-7351 guidelines.				
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabri- cation Allowance of 0.05mm.					
5. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 μm minimum, all the way around the pad.					
6. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release					
7. The stencil thickness should be 0.125 mm (5 mils).					
8. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.					
9. A 2 x 2 array of 1.10 mm square opening	gs on a 1.30 mm pitch should be used for the	center pad.			

- 10. A No-Clean, Type-3 solder paste is recommended.
- 11. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

7.3 QFN32 Package Marking



Figure 7.3. QFN32 Package Marking

The package marking consists of:

- PPPPPPP The part number designation.
- TTTTTT A trace or manufacturing code.
- YY The last 2 digits of the assembly year.
- WW The 2-digit workweek when the device was assembled.
- # The device revision (A, B, etc.).

8.2 QFP32 PCB Land Pattern



Figure 8.2. QFP32 PCB Land Pattern Drawing

Table 8.2.	QFP32 PCB	Land Pattern	Dimensions
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Dimension	Min	Мах
C1	8.40	8.50
C2	8.40	8.50
E	0.80 BSC	
X1	0.55	
Y1	1.5	

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.

2. This Land Pattern Design is based on the IPC-7351 guidelines.

3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.

5. The stencil thickness should be 0.125 mm (5 mils).

6. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.

7. A No-Clean, Type-3 solder paste is recommended.

8. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.



Figure 8.3. QFP32 Package Marking

The package marking consists of:

- PPPPPPP The part number designation.
- TTTTTT A trace or manufacturing code.
- YY The last 2 digits of the assembly year.
- WW The 2-digit workweek when the device was assembled.
- # The device revision (A, B, etc.).

9.2 QFN24 PCB Land Pattern



Figure 9.2. QFN24 PCB Land Pattern Drawing

Table 9.2. QFN24 PCB Land Pattern Dimensions

Dimension	Min	Мах	
C1	3.00		
C2	3.00		
e	0.4 REF		
X1	0.20		
X2	1.80		
Y1	0.80		
Y2	1.80		
Y3	0.4		
f	2.50 REF		
с	0.25	0.35	

10. QSOP24 Package Specifications

10.1 QSOP24 Package Dimensions



Figure 10.1. QSOP24 Package Drawing

Table 10.1. QSOP24 Package Dimensions

Dimension	Min	Тур	Мах
A	—	—	1.75
A1	0.10	—	0.25
b	0.20	—	0.30
с	0.10	—	0.25
D	8.65 BSC		
E	6.00 BSC		
E1	3.90 BSC		
е	0.635 BSC		
L	0.40 — 1.27		
theta	0°	—	8°

Min	Тур	Мах
	0.20	
	0.18	
	0.10	
	0.10	
	Min	Min Typ 0.20 0.18 0.10 0.10

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.

2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.

3. This drawing conforms to JEDEC outline MO-137, variation AE.

4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

10.2 QSOP24 PCB Land Pattern



Figure 10.2. QSOP24 PCB Land Pattern Drawing

Table 10.2. QSOP24 PCB Land Pattern Dimension

Dimension	Min	Мах	
С	5.20	5.30	
E	0.635 BSC		
x	0.30	0.40	
Y	1.50	1.60	

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.

2. This land pattern design is based on the IPC-7351 guidelines.

3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.

5. The stencil thickness should be 0.125 mm (5 mils).

6. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.

7. A No-Clean, Type-3 solder paste is recommended.

8. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.