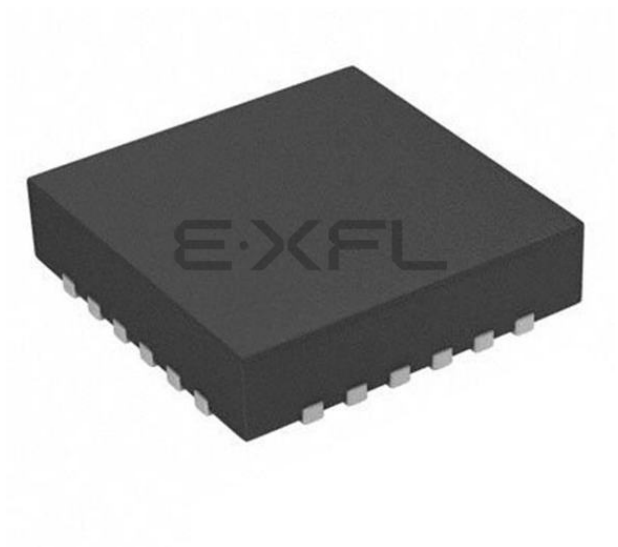

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	CIP-51 8051
Core Size	8-Bit
Speed	50MHz
Connectivity	I²C, SMBus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	20
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2.25K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 12x10/12b SAR; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	24-WFQFN Exposed Pad
Supplier Device Package	24-QFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm8bb31f32a-b-4qfn24

2. Ordering Information

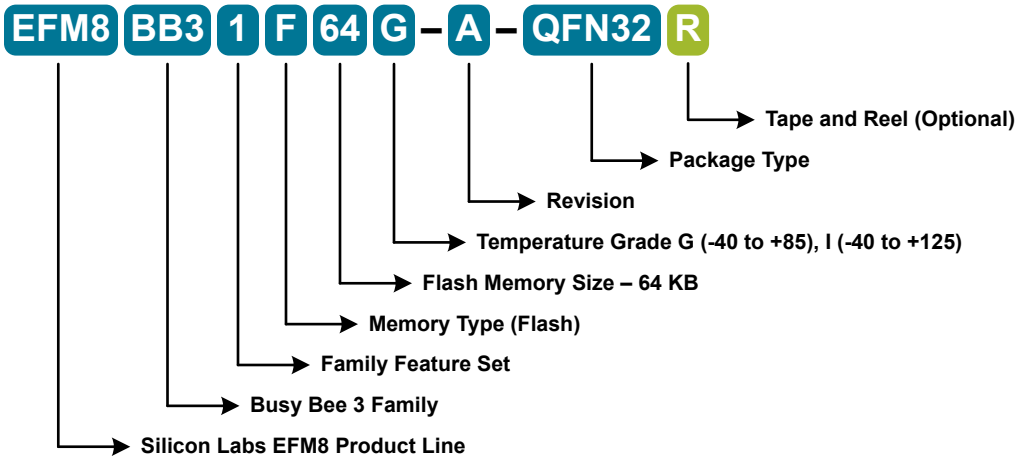

Figure 2.1. EFM8BB3 Part Numbering

All EFM8BB3 family members have the following features:

- CIP-51 Core running up to 49 MHz
- Three Internal Oscillators (49 MHz, 24.5 MHz and 80 kHz)
- SMBus
- I2C Slave
- SPI
- 2 UARTs
- 6-Channel Programmable Counter Array (PWM, Clock Generation, Capture/Compare)
- Six 16-bit Timers
- Four Configurable Logic Units
- 12-bit Analog-to-Digital Converter with integrated multiplexer, voltage reference, temperature sensor, channel sequencer, and direct-to-XRAM data transfer
- Two Analog Comparators
- 16-bit CRC Unit
- AEC-Q100 qualified
- Pre-loaded UART bootloader

In addition to these features, each part number in the EFM8BB3 family has a set of features that vary across the product line. The product selection guide shows the features available on each family member.

Table 2.1. Product Selection Guide

Ordering Part Number	Flash Memory (kB)	RAM (Bytes)	Digital Port I/Os (Total)	Voltage DACs	ADC0 Channels	Comparator 0 Inputs	Comparator 1 Inputs	Pb-free (RoHS Compliant)	Temperature Range	Package
EFM8BB31F64G-B-QFN32	64	4352	29	4	20	10	9	Yes	-40 to +85 °C	QFN32
EFM8BB31F64G-B-QFP32	64	4352	28	4	20	10	9	Yes	-40 to +85 °C	QFP32
EFM8BB31F64G-B-QFN24	64	4352	20	4	12	6	6	Yes	-40 to +85 °C	QFN24

3.7 Analog

12/10-Bit Analog-to-Digital Converter (ADC0)

The ADC is a successive-approximation-register (SAR) ADC with 12- and 10-bit modes, integrated track-and hold and a programmable window detector. The ADC is fully configurable under software control via several registers. The ADC may be configured to measure different signals using the analog multiplexer. The voltage reference for the ADC is selectable between internal and external reference sources.

- Up to 20 external inputs
- Single-ended 12-bit and 10-bit modes
- Supports an output update rate of up to 350 ksps in 12-bit mode
- Channel sequencer logic with direct-to-XDATA output transfers
- Operation in a low power mode at lower conversion speeds
- Asynchronous hardware conversion trigger, selectable between software, external I/O and internal timer and configurable logic sources
- Output data window comparator allows automatic range checking
- Support for output data accumulation
- Conversion complete and window compare interrupts supported
- Flexible output data formatting
- Includes a fully-internal fast-settling 1.65 V reference and an on-chip precision 2.4 / 1.2 V reference, with support for using the supply as the reference, an external reference and signal ground
- Integrated temperature sensor

12-Bit Digital-to-Analog Converters (DAC0, DAC1, DAC2, DAC3)

The DAC modules are 12-bit Digital-to-Analog Converters with the capability to synchronize multiple outputs together. The DACs are fully configurable under software control. The voltage reference for the DACs is selectable between internal and external reference sources.

- Voltage output with 12-bit performance
- Supports an update rate of 200 ksps
- Hardware conversion trigger, selectable between software, external I/O and internal timer and configurable logic sources
- Outputs may be configured to persist through reset and maintain output state to avoid system disruption
- Multiple DAC outputs can be synchronized together
- DAC pairs (DAC0 and 1 or DAC2 and 3) support complementary output waveform generation
- Outputs may be switched between two levels according to state of configurable logic / PWM input trigger
- Flexible input data formatting
- Supports references from internal supply, on-chip precision reference, or external VREF pin

3.10 Bootloader

All devices come pre-programmed with a UART0 bootloader. This bootloader resides in the code security page, which is the last page of code flash; it can be erased if it is not needed.

The byte before the Lock Byte is the Bootloader Signature Byte. Setting this byte to a value of 0xA5 indicates the presence of the bootloader in the system. Any other value in this location indicates that the bootloader is not present in flash.

When a bootloader is present, the device will jump to the bootloader vector after any reset, allowing the bootloader to run. The bootloader then determines if the device should stay in bootload mode or jump to the reset vector located at 0x0000. When the bootloader is not present, the device will jump to the reset vector of 0x0000 after any reset.

More information about the bootloader protocol and usage can be found in *AN945: EFM8 Factory Bootloader User Guide*. Application notes can be found on the Silicon Labs website (www.silabs.com/8bit-appnotes) or within Simplicity Studio by using the [**Application Notes**] tile.

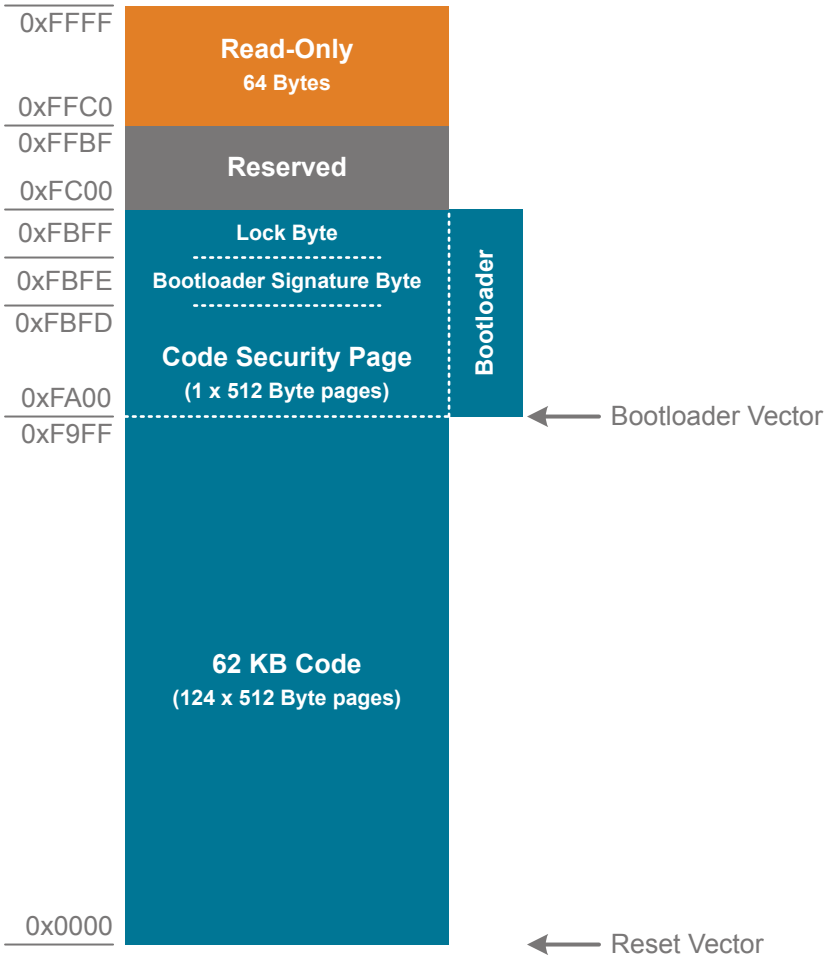

Figure 3.2. Flash Memory Map with Bootloader — 62.5 KB Devices

Table 3.2. Summary of Pins for Bootloader Communication

Bootloader	Pins for Bootload Communication
UART	TX – P0.4
	RX – P0.5

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Stop Mode—Core halted and all clocks stopped,Internal LDO On, Supply monitor off.	I_{DD}		—	120	740	µA
Shutdown Mode—Core halted and all clocks stopped,Internal LDO Off, Supply monitor off.	I_{DD}		—	0.2	4.5	µA
Analog Peripheral Supply Currents (-40 °C to +125 °C)						
High-Frequency Oscillator 0	I_{HFOSC0}	Operating at 24.5 MHz, T_A = 25 °C	—	120	135	µA
High-Frequency Oscillator 1	I_{HFOSC1}	Operating at 49 MHz, T_A = 25 °C	—	770	1200	µA
Low-Frequency Oscillator	I_{LFOSC}	Operating at 80 kHz, T_A = 25 °C	—	3.7	6	µA
ADC0[4]	I_{ADC}	High Speed Mode 1 Msps, 10-bit conversions Normal bias settings V_{DD} = 3.0 V	—	1210	1600	µA
		Low Power Mode 350 ksps, 12-bit conversions Low power bias settings V_{DD} = 3.0 V	—	415	560	µA
Internal ADC0 Reference[5]	I_{VREFFS}	High Speed Mode	—	700	790	µA
		Low Power Mode	—	170	210	µA
On-chip Precision Reference	I_{VREFP}		—	75	—	µA
Temperature Sensor	I_{TSENSE}		—	68	120	µA
Digital-to-Analog Converters (DAC0, DAC1, DAC2, DAC3)[6]	I_{DAC}		—	125	—	µA
Comparators (CMP0, CMP1)	I_{CMP}	CPMD = 11	—	0.5	—	µA
		CPMD = 10	—	3	—	µA
		CPMD = 01	—	10	—	µA
		CPMD = 00	—	25	—	µA
Comparator Reference	I_{CPREF}		—	24	—	µA
Voltage Supply Monitor (VMON0)	I_{VMON}		—	15	20	µA

4.1.9 ADC

Table 4.9. ADC

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Resolution	N_{bits}	12 Bit Mode		12		Bits
		10 Bit Mode		10		Bits
Throughput Rate (High Speed Mode)	f_S	10 Bit Mode	—	—	1.125	Msps
Throughput Rate (Low Power Mode)	f_S	12 Bit Mode	—	—	340	ksps
		10 Bit Mode	—	—	360	ksps
Tracking Time	t_{TRK}	High Speed Mode	230	—	—	ns
		Low Power Mode	450	—	—	ns
Power-On Time	t_{PWR}		1.2	—	—	µs
SAR Clock Frequency	f_{SAR}	High Speed Mode	—	—	18	MHz
		Low Power Mode	—	—	12.25	MHz
Conversion Time[1]	t_{CNV}	12-Bit Conversion, SAR Clock = 6.125 MHz, System Clock = 49 MHz		2.0		µs
		10-Bit Conversion, SAR Clock = 16.33 MHz, System Clock = 49 MHz		0.658		µs
Sample/Hold Capacitor	C_{SAR}	Gain = 1	—	5.2	—	pF
		Gain = 0.75	—	3.9	—	pF
		Gain = 0.5	—	2.6	—	pF
		Gain = 0.25	—	1.3	—	pF
Input Pin Capacitance	C_{IN}		—	20	—	pF
Input Mux Impedance	R_{MUX}		—	550	—	Ω
Voltage Reference Range	V_{REF}		1	—	V_{IO}	V
Input Voltage Range[2]	V_{IN}		0	—	V_{REF} / Gain	V
Power Supply Rejection Ratio	$PSRR_{ADC}$	At 1 kHz	—	66	—	dB
		At 1 MHz	—	43	—	dB
DC Performance						

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Integral Nonlinearity	INL	12 Bit Mode	-1.9	-0.35 / +1	1.9	LSB
		10 Bit Mode T_A = -40 °C to 85 °C	-0.6	±0.2	0.6	LSB
		10 Bit Mode T_A = -40 °C to 125 °C (I-grade parts only)	-0.7	±0.2	0.7	LSB
Differential Nonlinearity (Guaranteed Monotonic)	DNL	12 Bit Mode T_A = -40 °C to 85 °C	-0.9	±0.3	0.9	LSB
		12 Bit Mode T_A = -40 °C to 125 °C (I-grade parts only)	-1.02	±0.3	1.02	LSB
		10 Bit Mode	-0.5	±0.2	0.5	LSB
Offset Error[3]	E_{OFF}	12 Bit Mode T_A = -40 °C to 85 °C	-2	0	2	LSB
		12 Bit Mode T_A = -40 °C to 125 °C (I-grade parts only)	-3	0	3	LSB
		10 Bit Mode T_A = -40 °C to 85 °C	-1	0	1	LSB
		10 Bit Mode T_A = -40 °C to 125 °C (I-grade parts only)	-1	0	1.3	LSB
Offset Temperature Coefficient	TC_{OFF}		—	0.011	—	LSB/°C
Slope Error	E_M	12 Bit Mode T_A = -40 °C to 85 °C	-2.5	—	2.5	LSB
		12 Bit Mode T_A = -40 °C to 125 °C (I-grade parts only)	-2.6	—	2.6	LSB
		10 Bit Mode	-1.1	—	1.1	LSB
Dynamic Performance 10 kHz Sine Wave Input 1 dB below full scale, Max throughput, using AGND pin						
Signal-to-Noise	SNR	12 Bit Mode	64	68	—	dB
		10 Bit Mode	59	61	—	dB
Signal-to-Noise Plus Distortion	SNDR	12 Bit Mode	64	68	—	dB
		10 Bit Mode	59	61	—	dB
Total Harmonic Distortion (Up to 5th Harmonic)	THD	12 Bit Mode	—	-72	—	dB
		10 Bit Mode	—	-69	—	dB
Spurious-Free Dynamic Range	SFDR	12 Bit Mode	—	74	—	dB
		10 Bit Mode	—	71	—	dB

4.1.10 Voltage Reference

Table 4.10. Voltage Reference

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Internal Fast Settling Reference						
Output Voltage (Full Temperature and Supply Range)	V_{REFFS}		1.62	1.65	1.68	V
Temperature Coefficient	TC_{REFFS}		—	50	—	ppm/°C
Turn-on Time	t_{REFFS}		—	—	1.5	µs
Power Supply Rejection	$PSRR_{REFFS}$		—	400	—	ppm/V
On-chip Precision Reference						
Valid Supply Range	V_{DD}	1.2 V Output	2.2	—	3.6	V
		2.4 V Output	2.7	—	3.6	V
Output Voltage	V_{REFP}	1.2 V Output, V_{DD} = 3.3 V, T = 25 °C	1.195	1.2	1.205	V
		1.2 V Output	1.18	1.2	1.22	V
		2.4 V Output, V_{DD} = 3.3 V, T = 25 °C	2.39	2.4	2.41	V
		2.4 V Output	2.36	2.4	2.44	V
Turn-on Time, settling to 0.5 LSB	t_{VREFP}	4.7 µF tantalum + 0.1 µF ceramic bypass on VREF pin	—	3	—	ms
		0.1 µF ceramic bypass on VREF pin	—	100	—	µs
Load Regulation	LR_{VREFP}	VREF = 2.4 V, Load = 0 to 200 µA to GND	—	8	—	µV/µA
		VREF = 1.2 V, Load = 0 to 200 µA to GND	—	5	—	µV/µA
Load Capacitor	C_{VREFP}	Load = 0 to 200 µA to GND	0.1	—	—	µF
Short-circuit current	ISC_{VREFP}		—	—	8	mA
Power Supply Rejection	$PSRR_{VREFP}$		—	75	—	dB
External Reference						
Input Current	I_{EXTREF}	ADC Sample Rate = 800 ksps; VREF = 3.0 V	—	5	—	µA

4.1.11 Temperature Sensor

Table 4.11. Temperature Sensor

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Offset	V_{OFF}	T_A = 0 °C	—	751	—	mV
Offset Error[1]	E_{OFF}	T_A = 0 °C	—	19	—	mV
Slope	M		—	2.82	—	mV/°C
Slope Error[1]	E_M		—	29	—	µV/°C
Linearity	LIN	T = -40 °C to 85 °C	—	±0.4	—	°C
		T = -40 °C to 125 °C (I-grade parts only)	—	-0.6 to 1.2	—	°C
Turn-on Time	t_{ON}		—	3.5	—	µs

Note:
1. Represents one standard deviation from the mean.

4.1.12 DACs

Table 4.12. DACs

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Resolution	N_{bits}			12		Bits
Throughput Rate	f_S		—	—	200	ksps
Integral Nonlinearity	INL	DAC0 and DAC2 T_A = -40 °C to 125 °C (I-grade parts only)	-11.5	-1.77 / 1.56	11.5	LSB
		DAC0 and DAC3 T_A = -40 °C to 125 °C (I-grade parts only)	-13.5	-2.73 / 1.11	13.5	LSB
Differential Nonlinearity	DNL		-1	—	1	LSB
Output Noise	VREF = 2.4 V f_S = 0.1 Hz to 300 kHz		—	110	—	μV_{RMS}
Slew Rate	SLEW		—	±1	—	V/µs
Output Settling Time to 1% Full-scale	t_{SETTLE}	V_{OUT} change between 25% and 75% Full Scale	—	2.6	5	µs
Power-on Time	t_{PWR}		—	—	10	µs
Voltage Reference Range	V_{REF}		1.15	—	V_{DD}	V
Power Supply Rejection Ratio	PSRR	DC, V_{OUT} = 50% Full Scale	—	78	—	dB
Total Harmonic Distortion	THD	V_{OUT} = 10 kHz sine wave, 10% to 90%	54	—	—	dB
Offset Error	E_{OFF}	VREF = 2.4 V	-8	0	8	LSB
Full-Scale Error	E_{FS}	VREF = 2.4 V	-13	±5	13	LSB
External Load Impedance	R_{LOAD}		2	—	—	kΩ
External Load Capacitance[1]	C_{LOAD}		—	—	100	pF

Note:

1. No minimum external load capacitance is required. However, under low loading conditions, it is possible for the DAC output to glitch during start-up. If smooth start-up is required, the minimum loading capacitance at the pin should be a minimum of 10 pF.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Negative Hysteresis Mode 3 (CPMD = 11)	HYS_{CP-}	CPHYN = 00	—	-1.5	—	mV
		CPHYN = 01	—	-4	—	mV
		CPHYN = 10	—	-8	—	mV
		CPHYN = 11	—	-16	—	mV
Input Range (CP+ or CP-)	V_{IN}		-0.25	—	V_{IO}+0.25	V
Input Pin Capacitance	C_{CP}		—	7.5	—	pF
Internal Reference DAC Resolution	N_{bits}			6		bits
Common-Mode Rejection Ratio	$CMRR_{CP}$		—	70	—	dB
Power Supply Rejection Ratio	$PSRR_{CP}$		—	72	—	dB
Input Offset Voltage	V_{OFF}	T_A = 25 °C	-10	0	10	mV
Input Offset Tempco	TC_{OFF}		—	3.5	—	µV/°

4.1.14 Configurable Logic

Table 4.14. Configurable Logic

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Propagation Delay	t_{DLY}	Through single CLU Using an external pin	—	—	35.3	ns
		Through single CLU Using an internal connection	—	3	—	ns
Clocking Frequency	F_{CLK}	1 or 2 CLUs Cascaded	—	—	73.5	MHz
		3 or 4 CLUs Cascaded	—	—	36.75	MHz

4.1.15 Port I/O

Table 4.15. Port I/O

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output High Voltage (High Drive)	V_{OH}	I_{OH} = -7 mA, V_{IO} ≥ 3.0 V	V_{IO} - 0.7	—	—	V
		I_{OH} = -3.3 mA, 2.2 V ≤ V_{IO} < 3.0 V I_{OH} = -1.8 mA, 1.71 V ≤ V_{IO} < 2.2 V	V_{IO} x 0.8	—	—	V
Output Low Voltage (High Drive)	V_{OL}	I_{OL} = 13.5 mA, V_{IO} ≥ 3.0 V	—	—	0.6	V
		I_{OL} = 7 mA, 2.2 V ≤ V_{IO} < 3.0 V I_{OL} = 3.6 mA, 1.71 V ≤ V_{IO} < 2.2 V	—	—	V_{IO} x 0.2	V
Output High Voltage (Low Drive)	V_{OH}	I_{OH} = -4.75 mA, V_{IO} ≥ 3.0 V	V_{IO} - 0.7	—	—	V
		I_{OH} = -2.25 mA, 2.2 V ≤ V_{IO} < 3.0 V I_{OH} = -1.2 mA, 1.71 V ≤ V_{IO} < 2.2 V	V_{IO} x 0.8	—	—	V
Output Low Voltage (Low Drive)	V_{OL}	I_{OL} = 6.5 mA, V_{IO} ≥ 3.0 V	—	—	0.6	V
		I_{OL} = 3.5 mA, 2.2 V ≤ V_{IO} < 3.0 V I_{OL} = 1.8 mA, 1.71 V ≤ V_{IO} < 2.2 V	—	—	V_{IO} x 0.2	V
Input High Voltage	V_{IH}		0.7 x V_{IO}	—	—	V
Input Low Voltage	V_{IL}		—	—	0.3 x V_{IO}	V
Pin Capacitance	C_{IO}		—	7	—	pF
Weak Pull-Up Current (V_{IN} = 0 V)	I_{PU}	V_{DD} = 3.6	-30	-20	-10	µA
Input Leakage (Pullups off or Analog)	I_{LK}	GND < V_{IN} < V_{IO}	-1.1	—	4	µA
Input Leakage Current with V_{IN} above V_{IO}	I_{LK}	V_{IO} < V_{IN} < V_{IO}+2.5 V Any pin except P3.0, P3.1, P3.2, or P3.3	0	5	150	µA

5. Typical Connection Diagrams

5.1 Power

Figure 5.1 Power Connection Diagram on page 33 shows a typical connection diagram for the power pins of the device.

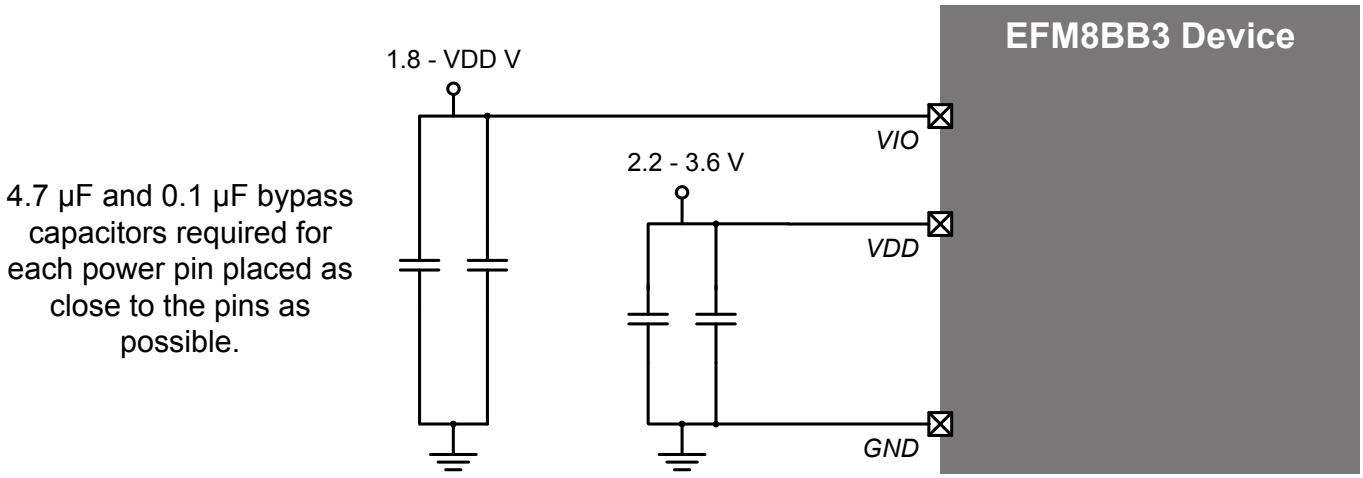

Figure 5.1. Power Connection Diagram

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
29	P0.4	Multifunction I/O	Yes	P0MAT.4 INT0.4 INT1.4 UART0_TX CLU0A.10 CLU1A.8 CLU3B.10	ADC0.2 CMP0P.2 CMP0N.2
30	P0.3	Multifunction I/O	Yes	P0MAT.3 EXTCLK INT0.3 INT1.3 CLU0B.9 CLU2B.9 CLU3A.9	XTAL2
31	P0.2	Multifunction I/O	Yes	P0MAT.2 INT0.2 INT1.2 CLU0OUT CLU0A.9 CLU2B.8 CLU3A.8	XTAL1 ADC0.1 CMP0P.1 CMP0N.1
32	P0.1	Multifunction I/O	Yes	P0MAT.1 INT0.1 INT1.1 CLU0B.8 CLU2A.9 CLU3B.9	ADC0.0 CMP0P.0 CMP0N.0 AGND
Center	GND	Ground			

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
30	P0.3	Multifunction I/O	Yes	P0MAT.3 EXTCLK INT0.3 INT1.3 CLU0B.9 CLU2B.9 CLU3A.9	XTAL2
31	P0.2	Multifunction I/O	Yes	P0MAT.2 INT0.2 INT1.2 CLU0OUT CLU0A.9 CLU2B.8 CLU3A.8	XTAL1 ADC0.1 CMP0P.1 CMP0N.1
32	P0.1	Multifunction I/O	Yes	P0MAT.1 INT0.1 INT1.1 CLU0B.8 CLU2A.9 CLU3B.9	ADC0.0 CMP0P.0 CMP0N.0 AGND

Dimension	Min	Typ	Max

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC Solid State Outline MO-220.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

8.2 QFP32 PCB Land Pattern

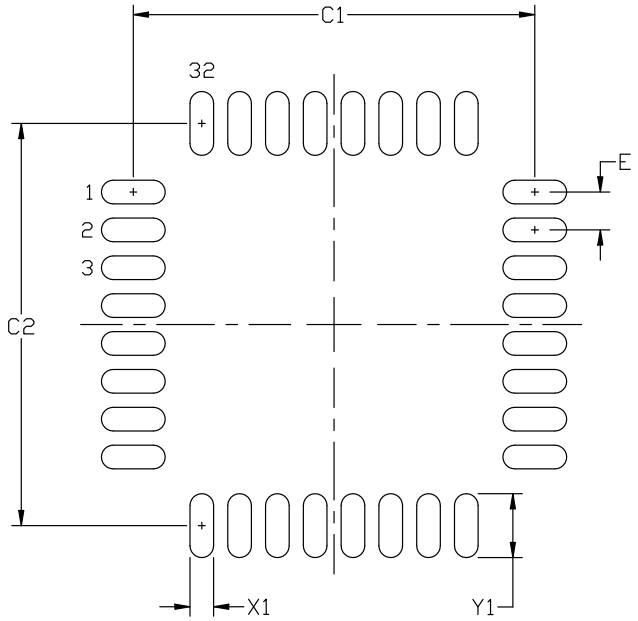

Figure 8.2. QFP32 PCB Land Pattern Drawing

Table 8.2. QFP32 PCB Land Pattern Dimensions

Dimension	Min	Max
C1	8.40	8.50
C2	8.40	8.50
E	0.80 BSC	
X1	0.55	
Y1	1.5	

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.
4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
7. A No-Clean, Type-3 solder paste is recommended.
8. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

9. QFN24 Package Specifications

9.1 QFN24 Package Dimensions

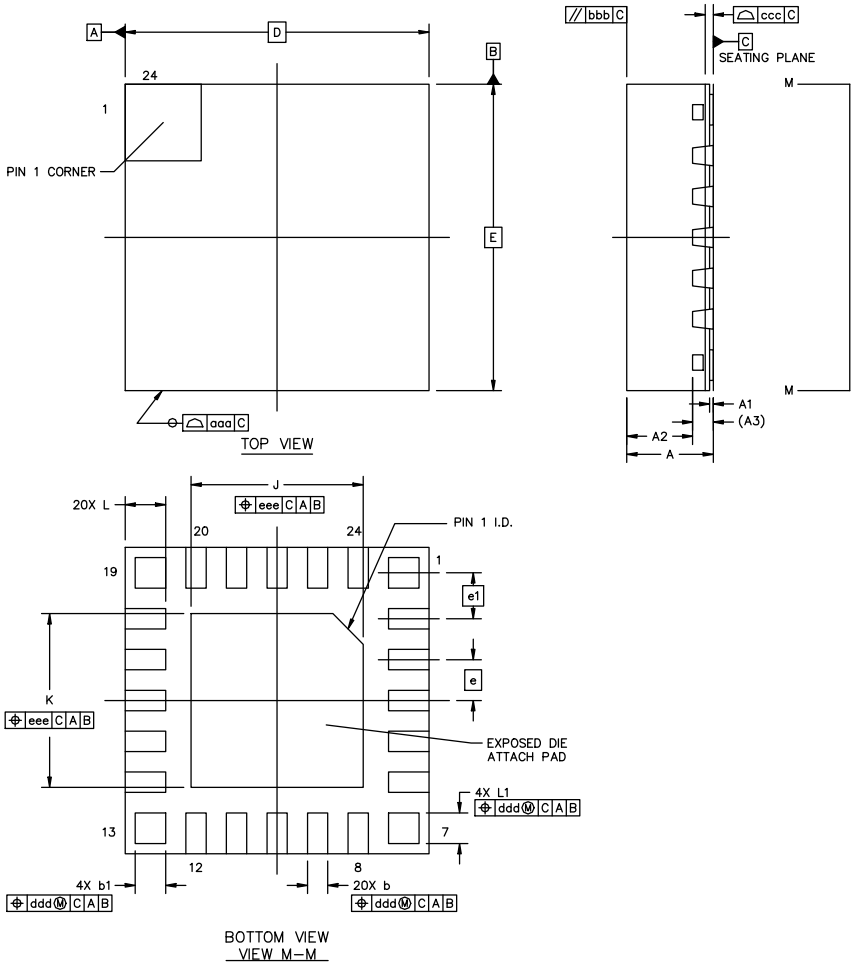

Figure 9.1. QFN24 Package Drawing

Table 9.1. QFN24 Package Dimensions

Dimension	Min	Typ	Max
A	0.8	0.85	0.9
A1	0.00	—	0.05
A2	—	0.65	—
A3		0.203 REF	
b	0.15	0.2	0.25
b1	0.25	0.3	0.35
D		3.00 BSC	
E		3.00 BSC	

Dimension	Min	Max

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on the IPC-SM-782 guidelines.
4. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.
5. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
6. The stencil thickness should be 0.125 mm (5 mils).
7. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
8. A 2 x 1 array of 0.7 mm x 1.6 mm openings on a 0.9 mm pitch should be used for the center pad.
9. A No-Clean, Type-3 solder paste is recommended.
10. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

9.3 QFN24 Package Marking

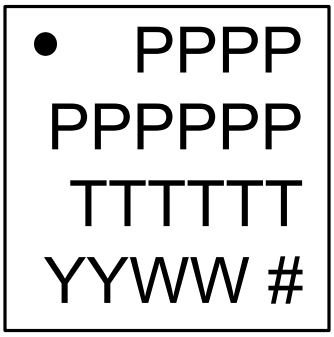

Figure 9.3. QFN24 Package Marking

The package marking consists of:

- PPPPPPPP – The part number designation.
- TTTTTT – A trace or manufacturing code.
- YY – The last 2 digits of the assembly year.
- WW – The 2-digit workweek when the device was assembled.
- # – The device revision (A, B, etc.).

10. QSOP24 Package Specifications

10.1 QSOP24 Package Dimensions

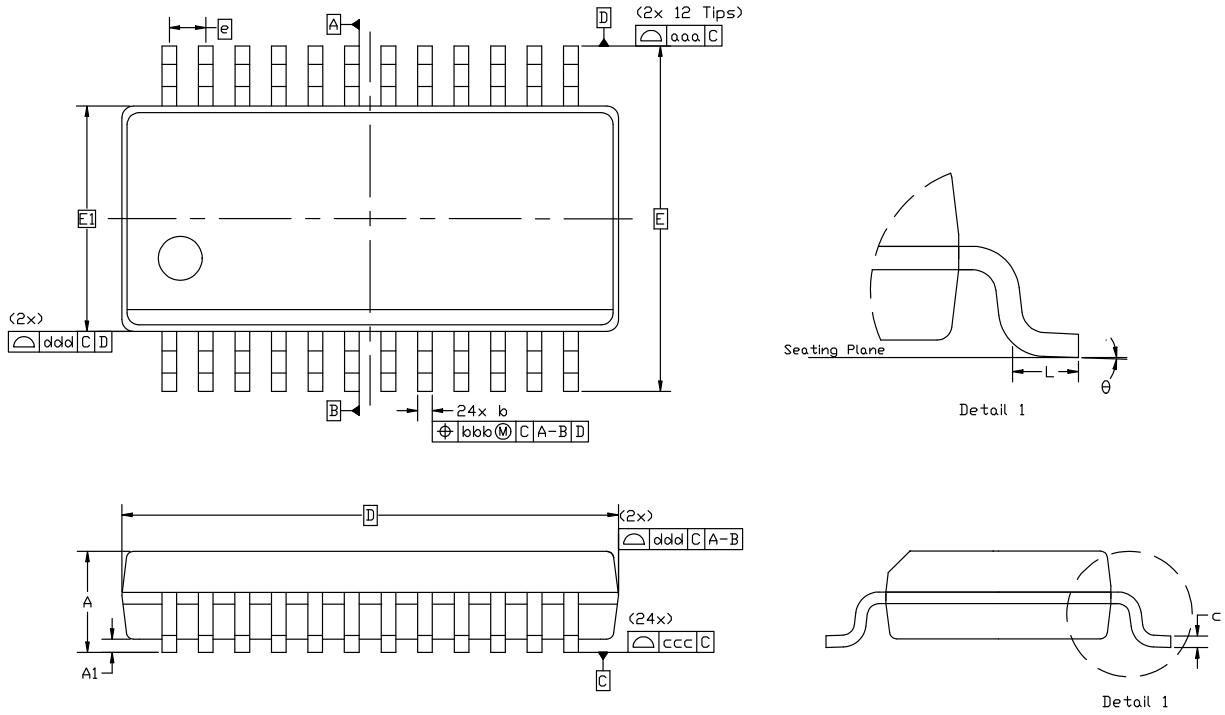

Figure 10.1. QSOP24 Package Drawing

Table 10.1. QSOP24 Package Dimensions

Dimension	Min	Typ	Max
A	—	—	1.75
A1	0.10	—	0.25
b	0.20	—	0.30
c	0.10	—	0.25
D	8.65 BSC		
E	6.00 BSC		
E1	3.90 BSC		
e	0.635 BSC		
L	0.40	—	1.27
theta	0°	—	8°

11. Revision History

11.1 Revision 1.01

October 21st, 2016

Updated Figure 2.1 EFM8BB3 Part Numbering on page 2 to include the I-grade description.

Updated QFN24 center pad stencil description.

11.2 Revision 1.0

September 6th, 2016

Filled in all TBD values in 4. Electrical Specifications.

Added a note regarding which DACs are available to Table 2.1 Product Selection Guide on page 2.

Added specifications for 4.1.16 SMBus.

Added bootloader pinout information to 3.10 Bootloader.

Added CRC Calculation Time to 4.1.4 Flash Memory.

11.3 Revision 0.4

May 12th, 2016

Filled in TBD values for DAC Integral Nonlinearity in Table 4.12 DACs on page 26.

Added I-grade devices.

Adjusted the Total Current Sunk into Supply Pin and Total Current Sourced out of Ground Pin specifications in 4.3 Absolute Maximum Ratings.

Added Operating Junction Temperature specification to 4.3 Absolute Maximum Ratings.

11.4 Revision 0.3

February 10th, 2016

Added EFM8831F16G-A-QFN24 to Table 2.1 Product Selection Guide on page 2.

Updated Figure 5.2 Debug Connection Diagram on page 34 to move the pull-up resistor on C2D / RSTb to after the series resistor instead of before.

Added mention of the pre-programmed bootloader in 1. Feature List.

Added a reference to *AN945: EFM8 Factory Bootloader User Guide* in 3.10 Bootloader.

Updated all part numbers to revision B.

Adjusted C1, C2, X2, Y2, and Y1 maximums for 7.2 QFN32 PCB Land Pattern.

Adjusted package markings for QFN32 and QSOP24 packages.

Filled in TBD minimum and maximum values for DAC Differential Nonlinearity in Table 4.12 DACs on page 26.

11.5 Revision 0.2

Added information on the bootloader to 3.10 Bootloader.

Updated some characterization TBD values.

11.6 Revision 0.1

Initial release.