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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Not For New Designs
Core Processor	CIP-51 8051
Core Size	8-Bit
Speed	50MHz
Connectivity	I <sup>2</sup> C, SMBus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	29
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2.25K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 20x10/12b SAR; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	32-WFQFN Exposed Pad
Supplier Device Package	32-QFN (5x5)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/silicon-labs/efm8bb31f32a-b-5qfn32r">https://www.e-xfl.com/product-detail/silicon-labs/efm8bb31f32a-b-5qfn32r</a>

### 3.2 Power

All internal circuitry draws power from the VDD supply pin. External I/O pins are powered from the VIO supply voltage (or VDD on devices without a separate VIO connection), while most of the internal circuitry is supplied by an on-chip LDO regulator. Control over the device power can be achieved by enabling/disabling individual peripherals as needed. Each analog peripheral can be disabled when not in use and placed in low power mode. Digital peripherals, such as timers and serial buses, have their clocks gated off and draw little power when they are not in use.

**Table 3.1. Power Modes**

Power Mode	Details	Mode Entry	Wake-Up Sources
Normal	Core and all peripherals clocked and fully operational		
Idle	<ul style="list-style-type: none"> <li>Core halted</li> <li>All peripherals clocked and fully operational</li> <li>Code resumes execution on wake event</li> </ul>	Set IDLE bit in PCON0	Any interrupt
Suspend	<ul style="list-style-type: none"> <li>Core and peripheral clocks halted</li> <li>HFOSC0 and HFOSC1 oscillators stopped</li> <li>Regulator in normal bias mode for fast wake</li> <li>Timer 3 and 4 may clock from LFOSC0</li> <li>Code resumes execution on wake event</li> </ul>	<ol style="list-style-type: none"> <li>Switch SYSCLK to HFOSC0</li> <li>Set SUSPEND bit in PCON1</li> </ol>	<ul style="list-style-type: none"> <li>Timer 4 Event</li> <li>SPI0 Activity</li> <li>I2C0 Slave Activity</li> <li>Port Match Event</li> <li>Comparator 0 Falling Edge</li> <li>CLUn Interrupt-Enabled Event</li> </ul>
Stop	<ul style="list-style-type: none"> <li>All internal power nets shut down</li> <li>Pins retain state</li> <li>Exit on any reset source</li> </ul>	<ol style="list-style-type: none"> <li>Clear STOPCF bit in REG0CN</li> <li>Set STOP bit in PCON0</li> </ol>	Any reset source
Snooze	<ul style="list-style-type: none"> <li>Core and peripheral clocks halted</li> <li>HFOSC0 and HFOSC1 oscillators stopped</li> <li>Regulator in low bias current mode for energy savings</li> <li>Timer 3 and 4 may clock from LFOSC0</li> <li>Code resumes execution on wake event</li> </ul>	<ol style="list-style-type: none"> <li>Switch SYSCLK to HFOSC0</li> <li>Set SNOOZE bit in PCON1</li> </ol>	<ul style="list-style-type: none"> <li>Timer 4 Event</li> <li>SPI0 Activity</li> <li>I2C0 Slave Activity</li> <li>Port Match Event</li> <li>Comparator 0 Falling Edge</li> <li>CLUn Interrupt-Enabled Event</li> </ul>
Shutdown	<ul style="list-style-type: none"> <li>All internal power nets shut down</li> <li>Pins retain state</li> <li>Exit on pin or power-on reset</li> </ul>	<ol style="list-style-type: none"> <li>Set STOPCF bit in REG0CN</li> <li>Set STOP bit in PCON0</li> </ol>	<ul style="list-style-type: none"> <li>RSTb pin reset</li> <li>Power-on reset</li> </ul>

### 3.3 I/O

Digital and analog resources are externally available on the device's multi-purpose I/O pins. Port pins P0.0-P2.3 can be defined as general-purpose I/O (GPIO), assigned to one of the internal digital resources through the crossbar or dedicated channels, or assigned to an analog function. Port pins P2.4 to P3.7 can be used as GPIO. Additionally, the C2 Interface Data signal (C2D) is shared with P3.0 or P3.7, depending on the package option.

The port control block offers the following features:

- Up to 29 multi-functions I/O pins, supporting digital and analog functions.
- Flexible priority crossbar decoder for digital peripheral assignment.
- Two drive strength settings for each port.
- State retention feature allows pins to retain configuration through most reset sources.
- Two direct-pin interrupt sources with dedicated interrupt vectors (INT0 and INT1).
- Up to 24 direct-pin interrupt sources with shared interrupt vector (Port Match).

### 3.4 Clocking

The CPU core and peripheral subsystem may be clocked by both internal and external oscillator resources. By default, the system clock comes up running from the 24.5 MHz oscillator divided by 8.

The clock control system offers the following features:

- Provides clock to core and peripherals.
- 24.5 MHz internal oscillator (HFOSC0), accurate to  $\pm 2\%$  over supply and temperature corners.
- 49 MHz internal oscillator (HFOSC1), accurate to  $\pm 2\%$  over supply and temperature corners.
- 80 kHz low-frequency oscillator (LFOSC0).
- External RC, CMOS, and high-frequency crystal clock options (EXTCLK).
- Clock divider with eight settings for flexible clock scaling:
  - Divide the selected clock source by 1, 2, 4, 8, 16, 32, 64, or 128.
  - HFOSC0 and HFOSC1 include 1.5x pre-scalers for further flexibility.

### 3.5 Counters/Timers and PWM

#### Programmable Counter Array (PCA0)

The programmable counter array (PCA) provides multiple channels of enhanced timer and PWM functionality while requiring less CPU intervention than standard counter/timers. The PCA consists of a dedicated 16-bit counter/timer and one 16-bit capture/compare module for each channel. The counter/timer is driven by a programmable timebase that has flexible external and internal clocking options. Each capture/compare module may be configured to operate independently in one of five modes: Edge-Triggered Capture, Software Timer, High-Speed Output, Frequency Output, or Pulse-Width Modulated (PWM) Output. Each capture/compare module has its own associated I/O line (CEXn) which is routed through the crossbar to port I/O when enabled.

- 16-bit time base
- Programmable clock divisor and clock source selection
- Up to six independently-configurable channels
- 8, 9, 10, 11 and 16-bit PWM modes (center or edge-aligned operation)
- Output polarity control
- Frequency output mode
- Capture on rising, falling or any edge
- Compare function for arbitrary waveform generation
- Software timer (internal compare) mode
- Can accept hardware “kill” signal from comparator 0 or comparator 1

## Timers (Timer 0, Timer 1, Timer 2, Timer 3, Timer 4, and Timer 5)

Several counter/timers are included in the device: two are 16-bit counter/timers compatible with those found in the standard 8051, and the rest are 16-bit auto-reload timers for timing peripherals or for general purpose use. These timers can be used to measure time intervals, count external events and generate periodic interrupt requests. Timer 0 and Timer 1 are nearly identical and have four primary modes of operation. The other timers offer both 16-bit and split 8-bit timer functionality with auto-reload and capture capabilities.

Timer 0 and Timer 1 include the following features:

- Standard 8051 timers, supporting backwards-compatibility with firmware and hardware.
- Clock sources include SYSCLK, SYSCLK divided by 12, 4, or 48, the External Clock divided by 8, or an external pin.
- 8-bit auto-reload counter/timer mode
- 13-bit counter/timer mode
- 16-bit counter/timer mode
- Dual 8-bit counter/timer mode (Timer 0)

Timer 2, Timer 3, Timer 4, and Timer 5 are 16-bit timers including the following features:

- Clock sources for all timers include SYSCLK, SYSCLK divided by 12, or the External Clock divided by 8
- LFOSC0 divided by 8 may be used to clock Timer 3 and Timer 4 in active or suspend/snooze power modes
- Timer 4 is a low-power wake source, and can be chained together with Timer 3
- 16-bit auto-reload timer mode
- Dual 8-bit auto-reload timer mode
- External pin capture
- LFOSC0 capture
- Comparator 0 capture
- Configurable Logic output capture

## Watchdog Timer (WDT0)

The device includes a programmable watchdog timer (WDT) running off the low-frequency oscillator. A WDT overflow forces the MCU into the reset state. To prevent the reset, the WDT must be restarted by application software before overflow. If the system experiences a software or hardware malfunction preventing the software from restarting the WDT, the WDT overflows and causes a reset. Following a reset, the WDT is automatically enabled and running with the default maximum time interval. If needed, the WDT can be disabled by system software or locked on to prevent accidental disabling. Once locked, the WDT cannot be disabled until the next system reset. The state of the RST pin is unaffected by this reset.

The Watchdog Timer has the following features:

- Programmable timeout interval
- Runs from the low-frequency oscillator
- Lock-out feature to prevent any modification until a system reset

## 3.6 Communications and Other Digital Peripherals

### Universal Asynchronous Receiver/Transmitter (UART0)

UART0 is an asynchronous, full duplex serial port offering modes 1 and 3 of the standard 8051 UART. Enhanced baud rate support allows a wide range of clock sources to generate standard baud rates. Received data buffering allows UART0 to start reception of a second incoming data byte before software has finished reading the previous data byte.

The UART module provides the following features:

- Asynchronous transmissions and receptions.
- Baud rates up to  $\text{SYSCLK}/2$  (transmit) or  $\text{SYSCLK}/8$  (receive).
- 8- or 9-bit data.
- Automatic start and stop generation.
- Single-byte FIFO on transmit and receive.

## 3.7 Analog

### 12/10-Bit Analog-to-Digital Converter (ADC0)

The ADC is a successive-approximation-register (SAR) ADC with 12- and 10-bit modes, integrated track-and hold and a programmable window detector. The ADC is fully configurable under software control via several registers. The ADC may be configured to measure different signals using the analog multiplexer. The voltage reference for the ADC is selectable between internal and external reference sources.

- Up to 20 external inputs
- Single-ended 12-bit and 10-bit modes
- Supports an output update rate of up to 350 ksps in 12-bit mode
- Channel sequencer logic with direct-to-XDATA output transfers
- Operation in a low power mode at lower conversion speeds
- Asynchronous hardware conversion trigger, selectable between software, external I/O and internal timer and configurable logic sources
- Output data window comparator allows automatic range checking
- Support for output data accumulation
- Conversion complete and window compare interrupts supported
- Flexible output data formatting
- Includes a fully-internal fast-settling 1.65 V reference and an on-chip precision 2.4 / 1.2 V reference, with support for using the supply as the reference, an external reference and signal ground
- Integrated temperature sensor

### 12-Bit Digital-to-Analog Converters (DAC0, DAC1, DAC2, DAC3)

The DAC modules are 12-bit Digital-to-Analog Converters with the capability to synchronize multiple outputs together. The DACs are fully configurable under software control. The voltage reference for the DACs is selectable between internal and external reference sources.

- Voltage output with 12-bit performance
- Supports an update rate of 200 ksps
- Hardware conversion trigger, selectable between software, external I/O and internal timer and configurable logic sources
- Outputs may be configured to persist through reset and maintain output state to avoid system disruption
- Multiple DAC outputs can be synchronized together
- DAC pairs (DAC0 and 1 or DAC2 and 3) support complementary output waveform generation
- Outputs may be switched between two levels according to state of configurable logic / PWM input trigger
- Flexible input data formatting
- Supports references from internal supply, on-chip precision reference, or external VREF pin

## Low Current Comparators (CMP0, CMP1)

An analog comparator is used to compare the voltage of two analog inputs, with a digital output indicating which input voltage is higher. External input connections to device I/O pins and internal connections are available through separate multiplexers on the positive and negative inputs. Hysteresis, response time, and current consumption may be programmed to suit the specific needs of the application.

The comparator includes the following features:

- Up to 10 (CMP0) or 9 (CMP1) external positive inputs
- Up to 10 (CMP0) or 9 (CMP1) external negative inputs
- Additional input options:
  - Internal connection to LDO output
  - Direct connection to GND
  - Direct connection to VDD
  - Dedicated 6-bit reference DAC
- Synchronous and asynchronous outputs can be routed to pins via crossbar
- Programmable hysteresis between 0 and  $\pm 20$  mV
- Programmable response time
- Interrupts generated on rising, falling, or both edges
- PWM output kill feature

## 3.8 Reset Sources

Reset circuitry allows the controller to be easily placed in a predefined default condition. On entry to this reset state, the following occur:

- The core halts program execution.
- Module registers are initialized to their defined reset values unless the bits reset only with a power-on reset.
- External port pins are forced to a known state.
- Interrupts and timers are disabled.

All registers are reset to the predefined values noted in the register descriptions unless the bits only reset with a power-on reset. The contents of RAM are unaffected during a reset; any previously stored data is preserved as long as power is not lost. By default, the Port I/O latches are reset to 1 in open-drain mode, with weak pullups enabled during and after the reset. Optionally, firmware may configure the port I/O, DAC outputs, and precision reference to maintain state through system resets other than power-on resets. For Supply Monitor and power-on resets, the RSTb pin is driven low until the device exits the reset state. On exit from the reset state, the program counter (PC) is reset, and the system clock defaults to an internal oscillator. The Watchdog Timer is enabled, and program execution begins at location 0x0000.

Reset sources on the device include the following:

- Power-on reset
- External reset pin
- Comparator reset
- Software-triggered reset
- Supply monitor reset (monitors VDD supply)
- Watchdog timer reset
- Missing clock detector reset
- Flash error reset

## 3.9 Debugging

The EFM8BB3 devices include an on-chip Silicon Labs 2-Wire (C2) debug interface to allow flash programming and in-system debugging with the production part installed in the end application. The C2 interface uses a clock signal (C2CK) and a bi-directional C2 data signal (C2D) to transfer information between the device and a host system. See the C2 Interface Specification for details on the C2 protocol.

## 4.1.9 ADC

Table 4.9. ADC

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Resolution	N <sub>bits</sub>	12 Bit Mode	12			Bits
		10 Bit Mode	10			Bits
Throughput Rate (High Speed Mode)	f <sub>S</sub>	10 Bit Mode	—	—	1.125	Msp/s
Throughput Rate (Low Power Mode)	f <sub>S</sub>	12 Bit Mode	—	—	340	ksps
		10 Bit Mode	—	—	360	ksps
Tracking Time	t <sub>TRK</sub>	High Speed Mode	230	—	—	ns
		Low Power Mode	450	—	—	ns
Power-On Time	t <sub>PWR</sub>		1.2	—	—	μs
SAR Clock Frequency	f <sub>SAR</sub>	High Speed Mode	—	—	18	MHz
		Low Power Mode	—	—	12.25	MHz
Conversion Time <sup>1</sup>	t <sub>CNV</sub>	12-Bit Conversion, SAR Clock = 6.125 MHz, System Clock = 49 MHz	2.0			μs
		10-Bit Conversion, SAR Clock = 16.33 MHz, System Clock = 49 MHz	0.658			μs
Sample/Hold Capacitor	C <sub>SAR</sub>	Gain = 1	—	5.2	—	pF
		Gain = 0.75	—	3.9	—	pF
		Gain = 0.5	—	2.6	—	pF
		Gain = 0.25	—	1.3	—	pF
Input Pin Capacitance	C <sub>IN</sub>		—	20	—	pF
Input Mux Impedance	R <sub>MUX</sub>		—	550	—	Ω
Voltage Reference Range	V <sub>REF</sub>		1	—	V <sub>IO</sub>	V
Input Voltage Range <sup>2</sup>	V <sub>IN</sub>		0	—	V <sub>REF</sub> / Gain	V
Power Supply Rejection Ratio	PSRR <sub>ADC</sub>	At 1 kHz	—	66	—	dB
		At 1 MHz	—	43	—	dB
DC Performance						

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>Note:</b> <ol style="list-style-type: none"> <li>Conversion Time does not include Tracking Time. Total Conversion Time is:  Total Conversion Time = <math>[RPT \times (ADTK + NUMBITS + 1) \times T(SARCLK)] + (T(ADCCLK) \times 4)</math>  where RPT is the number of conversions represented by the ADRPT field and ADCCLK is the clock selected for the ADC.</li> <li>Absolute input pin voltage is limited by the <math>V_{IO}</math> supply.</li> <li>The offset is determined using curve fitting since the specification is measured using linear search where the intercept is always positive.</li> </ol>						



#### 4.1.16 SMBus

**Table 4.16. SMBus Peripheral Timing Performance (Master Mode)**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>Standard Mode (100 kHz Class)</b>						
I2C Operating Frequency	$f_{I2C}$		0	—	70 <sup>2</sup>	kHz
SMBus Operating Frequency	$f_{SMB}$		40 <sup>1</sup>	—	70 <sup>2</sup>	kHz
Bus Free Time Between STOP and START Conditions	$t_{BUF}$		9.4	—	—	$\mu$ s
Hold Time After (Repeated) START Condition	$t_{HD:STA}$		4.7	—	—	$\mu$ s
Repeated START Condition Setup Time	$t_{SU:STA}$		9.4	—	—	$\mu$ s
STOP Condition Setup Time	$t_{SU:STO}$		9.4	—	—	$\mu$ s
Data Hold Time	$t_{HD:DAT}$		0	—	—	$\mu$ s
Data Setup Time	$t_{SU:DAT}$		4.7	—	—	$\mu$ s
Detect Clock Low Timeout	$t_{TIMEOUT}$		25	—	—	ms
Clock Low Period	$t_{LOW}$		4.7	—	—	$\mu$ s
Clock High Period	$t_{HIGH}$		9.4	—	50 <sup>3</sup>	$\mu$ s
<b>Fast Mode (400 kHz Class)</b>						
I2C Operating Frequency	$f_{I2C}$		0	—	256 <sup>2</sup>	kHz
SMBus Operating Frequency	$f_{SMB}$		40 <sup>1</sup>	—	256 <sup>2</sup>	kHz
Bus Free Time Between STOP and START Conditions	$t_{BUF}$		2.6	—	—	$\mu$ s
Hold Time After (Repeated) START Condition	$t_{HD:STA}$		1.3	—	—	$\mu$ s
Repeated START Condition Setup Time	$t_{SU:STA}$		2.6	—	—	$\mu$ s
STOP Condition Setup Time	$t_{SU:STO}$		2.6	—	—	$\mu$ s
Data Hold Time	$t_{HD:DAT}$		0	—	—	$\mu$ s
Data Setup Time	$t_{SU:DAT}$		1.3	—	—	$\mu$ s
Detect Clock Low Timeout	$t_{TIMEOUT}$		25	—	—	ms
Clock Low Period	$t_{LOW}$		1.3	—	—	$\mu$ s
Clock High Period	$t_{HIGH}$		2.6	—	50 <sup>3</sup>	$\mu$ s

**Note:**

1. The minimum SMBus frequency is limited by the maximum Clock High Period requirement of the SMBus specification.
2. The maximum I2C and SMBus frequencies are limited by the minimum Clock Low Period requirements of their respective specifications.
3. SMBus has a maximum requirement of 50  $\mu$ s for Clock High Period. Operating frequencies lower than 40 kHz will be longer than 50  $\mu$ s. I2C can support periods longer than 50  $\mu$ s.

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
15	P2.2	Multifunction I/O	Yes	P2MAT.2 CLU2OUT CLU1A.15 CLU2B.14 CLU3A.14	ADC0.15 CMP1P.4 CMP1N.4
16	P2.1	Multifunction I/O	Yes	P2MAT.1 I2C0_SCL CLU1B.14 CLU2A.15 CLU3B.15	ADC0.14 CMP1P.3 CMP1N.3
17	P2.0	Multifunction I/O	Yes	P2MAT.0 I2C0_SDA CLU1A.14 CLU2A.14 CLU3B.14	CMP1P.2 CMP1N.2
18	P1.7	Multifunction I/O	Yes	P1MAT.7 CLU0B.15 CLU1B.13 CLU2A.13	ADC0.13 CMP0P.9 CMP0N.9
19	P1.6	Multifunction I/O	Yes	P1MAT.6 CLU0A.15 CLU1B.12 CLU2A.12	ADC0.12
20	P1.5	Multifunction I/O	Yes	P1MAT.5 CLU0B.14 CLU1A.13 CLU2B.13	ADC0.11
21	P1.4	Multifunction I/O	Yes	P1MAT.4 CLU0A.14 CLU1A.12 CLU2B.12	ADC0.10
22	P1.3	Multifunction I/O	Yes	P1MAT.3 CLU0B.13 CLU1B.11 CLU2B.11 CLU3A.13	ADC0.9

## 6.2 EFM8BB3x-QFP32 Pin Definitions

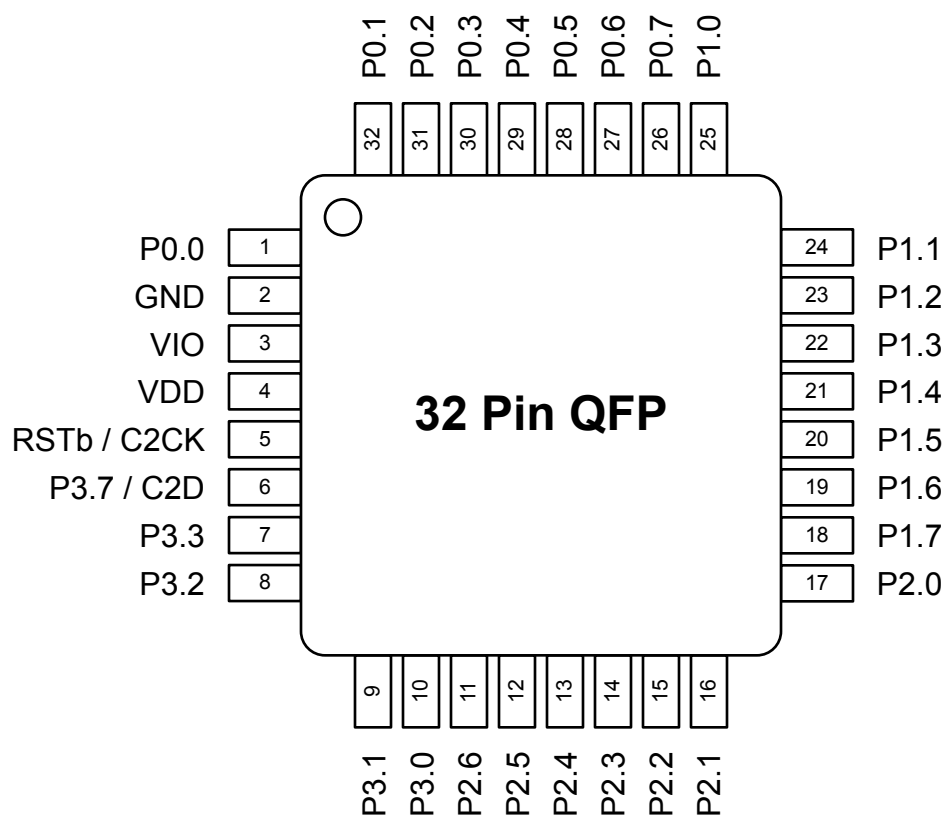


Figure 6.2. EFM8BB3x-QFP32 Pinout

Table 6.2. Pin Definitions for EFM8BB3x-QFP32

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
1	P0.0	Multifunction I/O	Yes	P0MAT.0 INT0.0 INT1.0 CLU0A.8 CLU2A.8 CLU3B.8	VREF
2	GND	Ground			
3	VIO	I/O Supply Power Input			
4	VDD	Supply Power Input			
5	RSTb / C2CK	Active-low Reset / C2 Debug Clock			

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
6	P3.7 / C2D	Multifunction I/O / C2 Debug Data			
7	P3.3	Multifunction I/O			DAC3
8	P3.2	Multifunction I/O			DAC2
9	P3.1	Multifunction I/O			DAC1
10	P3.0	Multifunction I/O			DAC0
11	P2.6	Multifunction I/O			ADC0.19 CMP1P.8 CMP1N.8
12	P2.5	Multifunction I/O		CLU3OUT	ADC0.18 CMP1P.7 CMP1N.7
13	P2.4	Multifunction I/O			ADC0.17 CMP1P.6 CMP1N.6
14	P2.3	Multifunction I/O	Yes	P2MAT.3 CLU1B.15 CLU2B.15 CLU3A.15	ADC0.16 CMP1P.5 CMP1N.5
15	P2.2	Multifunction I/O	Yes	P2MAT.2 CLU2OUT CLU1A.15 CLU2B.14 CLU3A.14	ADC0.15 CMP1P.4 CMP1N.4
16	P2.1	Multifunction I/O	Yes	P2MAT.1 I2C0_SCL CLU1B.14 CLU2A.15 CLU3B.15	ADC0.14 CMP1P.3 CMP1N.3
17	P2.0	Multifunction I/O	Yes	P2MAT.0 I2C0_SDA CLU1A.14 CLU2A.14 CLU3B.14	CMP1P.2 CMP1N.2

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
18	P1.7	Multifunction I/O	Yes	P1MAT.7 CLU0B.15 CLU1B.13 CLU2A.13	ADC0.13 CMP0P.9 CMP0N.9
19	P1.6	Multifunction I/O	Yes	P1MAT.6 CLU0A.15 CLU1B.12 CLU2A.12	ADC0.12
20	P1.5	Multifunction I/O	Yes	P1MAT.5 CLU0B.14 CLU1A.13 CLU2B.13	ADC0.11
21	P1.4	Multifunction I/O	Yes	P1MAT.4 CLU0A.14 CLU1A.12 CLU2B.12	ADC0.10
22	P1.3	Multifunction I/O	Yes	P1MAT.3 CLU0B.13 CLU1B.11 CLU2B.11 CLU3A.13	ADC0.9
23	P1.2	Multifunction I/O	Yes	P1MAT.2 CLU0A.13 CLU1A.11 CLU2B.10 CLU3A.12	ADC0.8 CMP0P.8 CMP0N.8
24	P1.1	Multifunction I/O	Yes	P1MAT.1 CLU0B.12 CLU1B.10 CLU2A.11 CLU3B.13	ADC0.7 CMP0P.7 CMP0N.7

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
2	P0.0	Multifunction I/O	Yes	P0MAT.0 INT0.0 INT1.0 CLU0A.8 CLU2A.8 CLU3B.8	VREF
3	GND	Ground			
4	VDD / VIO	Supply Power Input			
5	RSTb / C2CK	Active-low Reset / C2 Debug Clock			
6	P3.0 / C2D	Multifunction I/O / C2 Debug Data			
7	P2.3	Multifunction I/O	Yes	P2MAT.3 CLU1B.15 CLU2B.15 CLU3A.15	DAC3
8	P2.2	Multifunction I/O	Yes	P2MAT.2 CLU1A.15 CLU2B.14 CLU3A.14	DAC2
9	P2.1	Multifunction I/O	Yes	P2MAT.1 CLU1B.14 CLU2A.15 CLU3B.15	DAC1
10	P2.0	Multifunction I/O	Yes	P2MAT.0 CLU1A.14 CLU2A.14 CLU3B.14	DAC0
11	P1.6	Multifunction I/O	Yes	P1MAT.6 CLU3OUT CLU0A.15 CLU1B.12 CLU2A.12	ADC0.11 CMP1P.5 CMP1N.5

## 7. QFN32 Package Specifications

### 7.1 QFN32 Package Dimensions

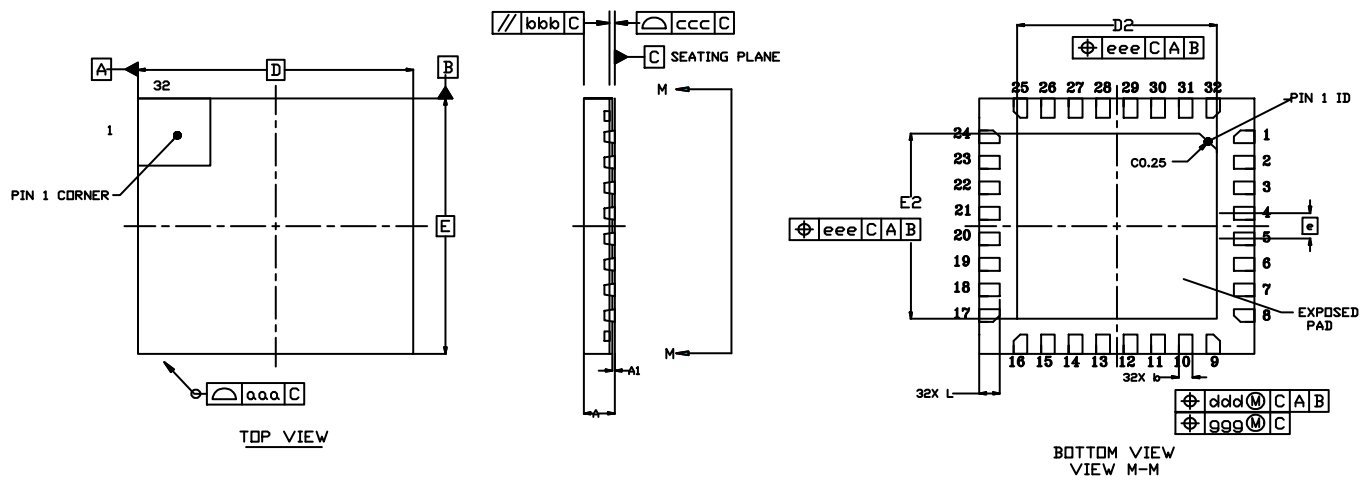


Figure 7.1. QFN32 Package Drawing

Table 7.1. QFN32 Package Dimensions

Dimension	Min	Typ	Max
A	0.45	0.50	0.55
A1	0.00	0.035	0.05
b	0.15	0.20	0.25
D	4.00 BSC.		
D2	2.80	2.90	3.00
e	0.40 BSC.		
E	4.00 BSC.		
E2	2.80	2.90	3.00
L	0.20	0.30	0.40
aaa	—	—	0.10
bbb	—	—	0.10
ccc	—	—	0.08
ddd	—	—	0.10
eee	—	—	0.10
ggg	—	—	0.05

## 7.2 QFN32 PCB Land Pattern

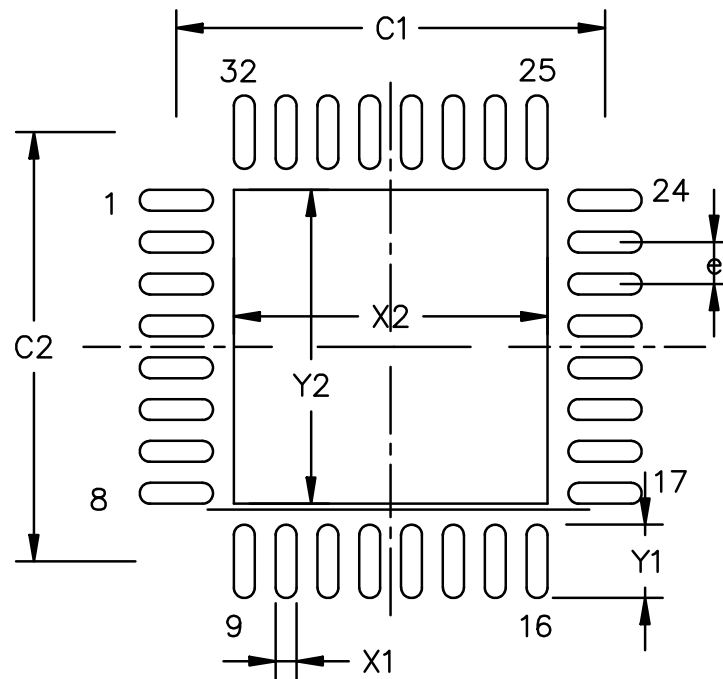


Figure 7.2. QFN32 PCB Land Pattern Drawing

Table 7.2. QFN32 PCB Land Pattern Dimensions

Dimension	Min	Max
C1	—	4.10
C2	—	4.10
X1	—	0.2
X2	—	3.0
Y1	—	0.7
Y2	—	3.0
e	—	0.4



## 8. QFP32 Package Specifications

### 8.1 QFP32 Package Dimensions

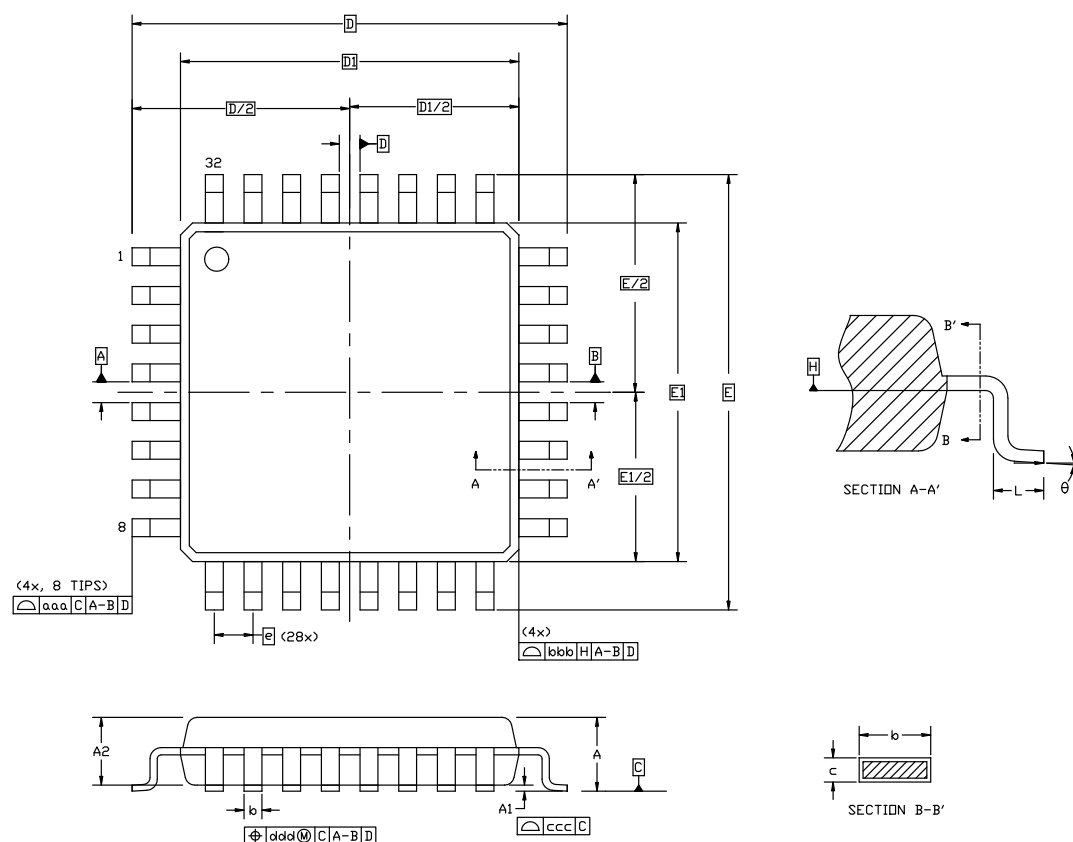


Figure 8.1. QFP32 Package Drawing

Table 8.1. QFP32 Package Dimensions

Dimension	Min	Typ	Max
A	—	—	1.20
A1	0.05	—	0.15
A2	0.95	1.00	1.05
b	0.30	0.37	0.45
c	0.09	—	0.20
D	9.00 BSC		
D1	7.00 BSC		
e	0.80 BSC		
E	9.00 BSC		
E1	7.00 BSC		
L	0.50	0.60	0.70

Dimension	Min	Typ	Max
aaa	0.20		
bbb	0.20		
ccc	0.10		
ddd	0.20		
theta	0°	3.5°	7°

**Note:**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC outline MS-026.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

## 8.2 QFP32 PCB Land Pattern

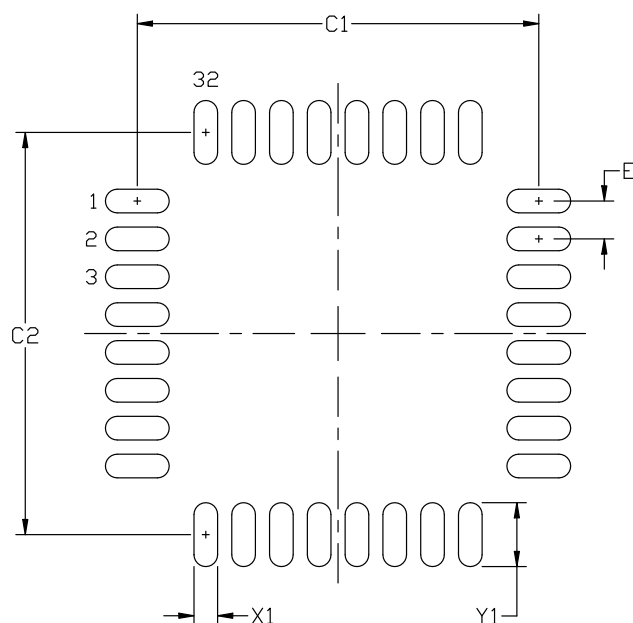


Figure 8.2. QFP32 PCB Land Pattern Drawing

Table 8.2. QFP32 PCB Land Pattern Dimensions

Dimension	Min	Max
C1	8.40	8.50
C2	8.40	8.50
E	0.80 BSC	
X1	0.55	
Y1	1.5	

**Note:**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60  $\mu\text{m}$  minimum, all the way around the pad.
4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
7. A No-Clean, Type-3 solder paste is recommended.
8. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

### 10.3 QSOP24 Package Marking



Figure 10.3. QSOP24 Package Marking

The package marking consists of:

- P P P P P P P P – The part number designation.
- T T T T T T – A trace or manufacturing code.
- Y Y – The last 2 digits of the assembly year.
- W W – The 2-digit workweek when the device was assembled.
- # – The device revision (A, B, etc.).

## 11. Revision History

### 11.1 Revision 1.01

October 21st, 2016

Updated [Figure 2.1 EFM8BB3 Part Numbering on page 2](#) to include the I-grade description.

Updated QFN24 center pad stencil description.

### 11.2 Revision 1.0

September 6th, 2016

Filled in all TBD values in [4. Electrical Specifications](#).

Added a note regarding which DACs are available to [Table 2.1 Product Selection Guide on page 2](#).

Added specifications for [4.1.16 SMBus](#).

Added bootloader pinout information to [3.10 Bootloader](#).

Added CRC Calculation Time to [4.1.4 Flash Memory](#).

### 11.3 Revision 0.4

May 12th, 2016

Filled in TBD values for DAC Integral Nonlinearity in [Table 4.12 DACs on page 26](#).

Added I-grade devices.

Adjusted the Total Current Sunk into Supply Pin and Total Current Sourced out of Ground Pin specifications in [4.3 Absolute Maximum Ratings](#).

Added Operating Junction Temperature specification to [4.3 Absolute Maximum Ratings](#).

### 11.4 Revision 0.3

February 10th, 2016

Added EFM8831F16G-A-QFN24 to [Table 2.1 Product Selection Guide on page 2](#).

Updated [Figure 5.2 Debug Connection Diagram on page 34](#) to move the pull-up resistor on C2D / RSTb to after the series resistor instead of before.

Added mention of the pre-programmed bootloader in [1. Feature List](#).

Added a reference to *AN945: EFM8 Factory Bootloader User Guide* in [3.10 Bootloader](#).

Updated all part numbers to revision B.

Adjusted C1, C2, X2, Y2, and Y1 maximums for [7.2 QFN32 PCB Land Pattern](#).

Adjusted package markings for QFN32 and QSOP24 packages.

Filled in TBD minimum and maximum values for DAC Differential Nonlinearity in [Table 4.12 DACs on page 26](#).

### 11.5 Revision 0.2

Added information on the bootloader to [3.10 Bootloader](#).

Updated some characterization TBD values.

### 11.6 Revision 0.1

Initial release.