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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Discontinued at Digi-Key
Core Processor	CIP-51 8051
Core Size	8-Bit
Speed	50MHz
Connectivity	I ² C, SMBus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	20
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2.25K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 12x10/12b SAR; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	24-VFQFN Exposed Pad
Supplier Device Package	24-QFN (3x3)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm8bb31f32g-b-qfn24r

1. Feature List

The EFM8BB3 device family are fully integrated, mixed-signal system-on-a-chip MCUs. Highlighted features are listed below.

- Core:
 - Pipelined CIP-51 Core
 - Fully compatible with standard 8051 instruction set
 - 70% of instructions execute in 1-2 clock cycles
 - 50 MHz maximum operating frequency
- Memory:
 - Up to 64 kB flash memory (63 kB user-accessible), in-system re-programmable from firmware in 512-byte sectors
 - Up to 4352 bytes RAM (including 256 bytes standard 8051 RAM and 4096 bytes on-chip XRAM)
- Power:
 - Internal LDO regulator for CPU core voltage
 - Power-on reset circuit and brownout detectors
- I/O: Up to 29 total multifunction I/O pins:
 - Up to 25 pins 5 V tolerant under bias
 - Selectable state retention through reset events
 - Flexible peripheral crossbar for peripheral routing
 - 5 mA source, 12.5 mA sink allows direct drive of LEDs
- Clock Sources:
 - Internal 49 MHz oscillator with accuracy of $\pm 2\%$
 - Internal 24.5 MHz oscillator with $\pm 2\%$ accuracy
 - Internal 80 kHz low-frequency oscillator
 - External CMOS clock option
 - External crystal/RC Oscillator (up to 25 MHz)
- Analog:
 - 12/10-Bit Analog-to-Digital Converter (ADC)
 - Internal temperature sensor
 - 4 x 12-Bit Digital-to-Analog Converters (DAC)
 - 2 x Low-current analog comparators with adjustable reference
- Communications and Digital Peripherals:
 - 2 x UART, up to 3 Mbaud
 - SPI™ Master / Slave, up to 12 Mbps
 - SMBus™/I2C™ Master / Slave, up to 400 kbps
 - I2C High-Speed Slave, up to 3.4 Mbps
 - 16-bit CRC unit, supporting automatic CRC of flash at 256-byte boundaries
 - 4 Configurable Logic Units
- Timers/Counters and PWM:
 - 6-channel programmable counter array (PCA) supporting PWM, capture/compare, and frequency output modes
 - 6 x 16-bit general-purpose timers
 - Independent watchdog timer, clocked from the low frequency oscillator
- On-Chip, Non-Intrusive Debugging
 - Full memory and register inspection
 - Four hardware breakpoints, single-stepping
- Pre-programmed UART bootloader
- Temperature range -40 to 85 °C or -40 to 125 °C

With on-chip power-on reset, voltage supply monitor, watchdog timer, and clock oscillator, the EFM8BB3 devices are truly standalone system-on-a-chip solutions. The flash memory is reprogrammable in-circuit, providing nonvolatile data storage and allowing field upgrades of the firmware. The on-chip debugging interface (C2) allows non-intrusive (uses no on-chip resources), full speed, in-circuit debugging using the production MCU installed in the final application. This debug logic supports inspection and modification of memory and registers, setting breakpoints, single stepping, and run and halt commands. All analog and digital peripherals are fully functional while debugging. Device operation is specified from 2.2 V up to a 3.6 V supply. Devices are AEC-Q100 qualified and available in 4x4 mm 32-pin QFN, 3x3 mm 24-pin QFN, 32-pin QFP, or 24-pin QSOP packages. All package options are lead-free and RoHS compliant.

3.2 Power

All internal circuitry draws power from the VDD supply pin. External I/O pins are powered from the VIO supply voltage (or VDD on devices without a separate VIO connection), while most of the internal circuitry is supplied by an on-chip LDO regulator. Control over the device power can be achieved by enabling/disabling individual peripherals as needed. Each analog peripheral can be disabled when not in use and placed in low power mode. Digital peripherals, such as timers and serial buses, have their clocks gated off and draw little power when they are not in use.

Table 3.1. Power Modes

Power Mode	Details	Mode Entry	Wake-Up Sources
Normal	Core and all peripherals clocked and fully operational		
Idle	<ul style="list-style-type: none"> Core halted All peripherals clocked and fully operational Code resumes execution on wake event 	Set IDLE bit in PCON0	Any interrupt
Suspend	<ul style="list-style-type: none"> Core and peripheral clocks halted HFOSC0 and HFOSC1 oscillators stopped Regulator in normal bias mode for fast wake Timer 3 and 4 may clock from LFOSC0 Code resumes execution on wake event 	<ol style="list-style-type: none"> Switch SYSCLK to HFOSC0 Set SUSPEND bit in PCON1 	<ul style="list-style-type: none"> Timer 4 Event SPI0 Activity I2C0 Slave Activity Port Match Event Comparator 0 Falling Edge CLUn Interrupt-Enabled Event
Stop	<ul style="list-style-type: none"> All internal power nets shut down Pins retain state Exit on any reset source 	<ol style="list-style-type: none"> Clear STOPCF bit in REG0CN Set STOP bit in PCON0 	Any reset source
Snooze	<ul style="list-style-type: none"> Core and peripheral clocks halted HFOSC0 and HFOSC1 oscillators stopped Regulator in low bias current mode for energy savings Timer 3 and 4 may clock from LFOSC0 Code resumes execution on wake event 	<ol style="list-style-type: none"> Switch SYSCLK to HFOSC0 Set SNOOZE bit in PCON1 	<ul style="list-style-type: none"> Timer 4 Event SPI0 Activity I2C0 Slave Activity Port Match Event Comparator 0 Falling Edge CLUn Interrupt-Enabled Event
Shutdown	<ul style="list-style-type: none"> All internal power nets shut down Pins retain state Exit on pin or power-on reset 	<ol style="list-style-type: none"> Set STOPCF bit in REG0CN Set STOP bit in PCON0 	<ul style="list-style-type: none"> RSTb pin reset Power-on reset

3.3 I/O

Digital and analog resources are externally available on the device's multi-purpose I/O pins. Port pins P0.0-P2.3 can be defined as general-purpose I/O (GPIO), assigned to one of the internal digital resources through the crossbar or dedicated channels, or assigned to an analog function. Port pins P2.4 to P3.7 can be used as GPIO. Additionally, the C2 Interface Data signal (C2D) is shared with P3.0 or P3.7, depending on the package option.

The port control block offers the following features:

- Up to 29 multi-functions I/O pins, supporting digital and analog functions.
- Flexible priority crossbar decoder for digital peripheral assignment.
- Two drive strength settings for each port.
- State retention feature allows pins to retain configuration through most reset sources.
- Two direct-pin interrupt sources with dedicated interrupt vectors (INT0 and INT1).
- Up to 24 direct-pin interrupt sources with shared interrupt vector (Port Match).

Low Current Comparators (CMP0, CMP1)

An analog comparator is used to compare the voltage of two analog inputs, with a digital output indicating which input voltage is higher. External input connections to device I/O pins and internal connections are available through separate multiplexers on the positive and negative inputs. Hysteresis, response time, and current consumption may be programmed to suit the specific needs of the application.

The comparator includes the following features:

- Up to 10 (CMP0) or 9 (CMP1) external positive inputs
- Up to 10 (CMP0) or 9 (CMP1) external negative inputs
- Additional input options:
 - Internal connection to LDO output
 - Direct connection to GND
 - Direct connection to VDD
 - Dedicated 6-bit reference DAC
- Synchronous and asynchronous outputs can be routed to pins via crossbar
- Programmable hysteresis between 0 and ± 20 mV
- Programmable response time
- Interrupts generated on rising, falling, or both edges
- PWM output kill feature

3.8 Reset Sources

Reset circuitry allows the controller to be easily placed in a predefined default condition. On entry to this reset state, the following occur:

- The core halts program execution.
- Module registers are initialized to their defined reset values unless the bits reset only with a power-on reset.
- External port pins are forced to a known state.
- Interrupts and timers are disabled.

All registers are reset to the predefined values noted in the register descriptions unless the bits only reset with a power-on reset. The contents of RAM are unaffected during a reset; any previously stored data is preserved as long as power is not lost. By default, the Port I/O latches are reset to 1 in open-drain mode, with weak pullups enabled during and after the reset. Optionally, firmware may configure the port I/O, DAC outputs, and precision reference to maintain state through system resets other than power-on resets. For Supply Monitor and power-on resets, the RSTb pin is driven low until the device exits the reset state. On exit from the reset state, the program counter (PC) is reset, and the system clock defaults to an internal oscillator. The Watchdog Timer is enabled, and program execution begins at location 0x0000.

Reset sources on the device include the following:

- Power-on reset
- External reset pin
- Comparator reset
- Software-triggered reset
- Supply monitor reset (monitors VDD supply)
- Watchdog timer reset
- Missing clock detector reset
- Flash error reset

3.9 Debugging

The EFM8BB3 devices include an on-chip Silicon Labs 2-Wire (C2) debug interface to allow flash programming and in-system debugging with the production part installed in the end application. The C2 interface uses a clock signal (C2CK) and a bi-directional C2 data signal (C2D) to transfer information between the device and a host system. See the C2 Interface Specification for details on the C2 protocol.

4. Electrical Specifications

4.1 Electrical Characteristics

All electrical parameters in all tables are specified under the conditions listed in [Table 4.1 Recommended Operating Conditions on page 14](#), unless stated otherwise.

4.1.1 Recommended Operating Conditions

Table 4.1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating Supply Voltage on VDD	V _{DD}		2.2	—	3.6	V
Operating Supply Voltage on VIO ^{2, 3}	V _{IO}		2.2	—	V _{DD}	V
System Clock Frequency	f _{SYSCLK}		0	—	50	MHz
Operating Ambient Temperature	T _A	G-grade devices	−40	—	85	°C
		I-grade devices	−40	—	125	°C

Note:

1. All voltages with respect to GND
2. In certain package configurations, the VIO and VDD supplies are bonded to the same pin.
3. GPIO levels are undefined whenever VIO is less than 1 V.

4.1.2 Power Consumption

Table 4.2. Power Consumption

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Digital Core Supply Current (G-grade devices, -40 °C to +85 °C)						
Normal Mode-Full speed with code executing from flash	I _{DD}	F _{SYSCLK} = 49 MHz (HFOSC1) ²	—	5	14.4	mA
		F _{SYSCLK} = 24.5 MHz (HFOSC0) ²	—	4.2	5	mA
		F _{SYSCLK} = 1.53 MHz (HFOSC0) ²	—	625	820	μA
		F _{SYSCLK} = 80 kHz ³	—	155	310	μA
Idle Mode-Core halted with peripherals running	I _{DD}	F _{SYSCLK} = 49 MHz (HFOSC1) ²	—	3.8	11.8	mA
		F _{SYSCLK} = 24.5 MHz (HFOSC0) ²	—	3.14	3.8	mA
		F _{SYSCLK} = 1.53 MHz (HFOSC0) ²	—	520	725	μA
		F _{SYSCLK} = 80 kHz ³	—	135	315	μA
Suspend Mode-Core halted and high frequency clocks stopped, Supply monitor off.	I _{DD}	LFO Running	—	125	320	μA
		LFO Stopped	—	120	300	μA
Snooze Mode-Core halted and high frequency clocks stopped. Regulator in low-power state, Supply monitor off.	I _{DD}	LFO Running	—	23	190	μA
		LFO Stopped	—	19	186	μA
Stop Mode—Core halted and all clocks stopped, Internal LDO On, Supply monitor off.	I _{DD}		—	120	300	μA
Shutdown Mode—Core halted and all clocks stopped, Internal LDO Off, Supply monitor off.	I _{DD}		—	0.2	0.91	μA
Digital Core Supply Current (I-grade devices, -40 °C to +125 °C)						
Normal Mode-Full speed with code executing from flash	I _{DD}	F _{SYSCLK} = 49 MHz (HFOSC1) ²	—	5	14.4	mA
		F _{SYSCLK} = 24.5 MHz (HFOSC0) ²	—	4.2	5.2	mA
		F _{SYSCLK} = 1.53 MHz (HFOSC0) ²	—	625	1280	μA
		F _{SYSCLK} = 80 kHz ³	—	155	765	μA
Idle Mode-Core halted with peripherals running	I _{DD}	F _{SYSCLK} = 49 MHz (HFOSC1) ²	—	3.8	11.8	mA
		F _{SYSCLK} = 24.5 MHz (HFOSC0) ²	—	3.14	4.1	mA
		F _{SYSCLK} = 1.53 MHz (HFOSC0) ²	—	520	1175	μA
		F _{SYSCLK} = 80 kHz ³	—	135	750	μA
Suspend Mode-Core halted and high frequency clocks stopped, Supply monitor off.	I _{DD}	LFO Running	—	125	775	μA
		LFO Stopped	—	120	755	μA
Snooze Mode-Core halted and high frequency clocks stopped. Regulator in low-power state, Supply monitor off.	I _{DD}	LFO Running	—	23	615	μA
		LFO Stopped	—	19	610	μA

4.1.4 Flash Memory

Table 4.4. Flash Memory

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Write Time ^{1,2}	t_{WRITE}	One Byte, $F_{\text{SYSCLK}} = 24.5 \text{ MHz}$	19	20	21	μs
Erase Time ^{1,2}	t_{ERASE}	One Page, $F_{\text{SYSCLK}} = 24.5 \text{ MHz}$	5.2	5.35	5.5	ms
V_{DD} Voltage During Programming ³	V_{PROG}		2.2	—	3.6	V
Endurance (Write/Erase Cycles)	N_{WE}		20k	100k	—	Cycles
CRC Calculation Time	t_{CRC}	One 256-Byte Block $\text{SYSCLK} = 49 \text{ MHz}$	—	5.5	—	μs

Note:

1. Does not include sequencing time before and after the write/erase operation, which may be multiple SYSCLK cycles.
2. The internal High-Frequency Oscillator 0 has a programmable output frequency, which is factory programmed to 24.5 MHz. If user firmware adjusts the oscillator speed, it must be between 22 and 25 MHz during any flash write or erase operation. It is recommended to write the HFO0CAL register back to its reset value when writing or erasing flash.
3. Flash can be safely programmed at any voltage above the supply monitor threshold (V_{VDDM}).
4. Data Retention Information is published in the Quarterly Quality and Reliability Report.

4.1.5 Power Management Timing

Table 4.5. Power Management Timing

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Idle Mode Wake-up Time	t_{IDLEWK}		2	—	3	SYSCLKs
Suspend Mode Wake-up Time	$t_{\text{SUS-}}t_{\text{PENDWK}}$	$\text{SYSCLK} = \text{HFOSC0}$ $\text{CLKDIV} = 0x00$	—	170	—	ns
Snooze Mode Wake-up Time	t_{SLEEPWK}	$\text{SYSCLK} = \text{HFOSC0}$ $\text{CLKDIV} = 0x00$	—	12	—	μs

4.1.8 Crystal Oscillator

Table 4.8. Crystal Oscillator

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Crystal Frequency	f_{XTAL}		0.02	—	25	MHz
Crystal Drive Current	I_{XTAL}	XFCN = 0	—	0.5	—	μA
		XFCN = 1	—	1.5	—	μA
		XFCN = 2	—	4.8	—	μA
		XFCN = 3	—	14	—	μA
		XFCN = 4	—	40	—	μA
		XFCN = 5	—	120	—	μA
		XFCN = 6	—	550	—	μA
		XFCN = 7	—	2.6	—	mA

4.1.9 ADC

Table 4.9. ADC

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Resolution	N _{bits}	12 Bit Mode	12			Bits
		10 Bit Mode	10			Bits
Throughput Rate (High Speed Mode)	f _S	10 Bit Mode	—	—	1.125	Msp/s
Throughput Rate (Low Power Mode)	f _S	12 Bit Mode	—	—	340	ksps
		10 Bit Mode	—	—	360	ksps
Tracking Time	t _{TRK}	High Speed Mode	230	—	—	ns
		Low Power Mode	450	—	—	ns
Power-On Time	t _{PWR}		1.2	—	—	μs
SAR Clock Frequency	f _{SAR}	High Speed Mode	—	—	18	MHz
		Low Power Mode	—	—	12.25	MHz
Conversion Time ¹	t _{CNV}	12-Bit Conversion, SAR Clock = 6.125 MHz, System Clock = 49 MHz	2.0			μs
		10-Bit Conversion, SAR Clock = 16.33 MHz, System Clock = 49 MHz	0.658			μs
Sample/Hold Capacitor	C _{SAR}	Gain = 1	—	5.2	—	pF
		Gain = 0.75	—	3.9	—	pF
		Gain = 0.5	—	2.6	—	pF
		Gain = 0.25	—	1.3	—	pF
Input Pin Capacitance	C _{IN}		—	20	—	pF
Input Mux Impedance	R _{MUX}		—	550	—	Ω
Voltage Reference Range	V _{REF}		1	—	V _{IO}	V
Input Voltage Range ²	V _{IN}		0	—	V _{REF} / Gain	V
Power Supply Rejection Ratio	PSRR _{ADC}	At 1 kHz	—	66	—	dB
		At 1 MHz	—	43	—	dB
DC Performance						

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Integral Nonlinearity	INL	12 Bit Mode	-1.9	-0.35 / +1	1.9	LSB
		10 Bit Mode	-0.6	±0.2	0.6	LSB
		T _A = -40 °C to 85 °C				
		10 Bit Mode	-0.7	±0.2	0.7	LSB
		T _A = -40 °C to 125 °C (I-grade parts only)				
Differential Nonlinearity (Guaranteed Monotonic)	DNL	12 Bit Mode	-0.9	±0.3	0.9	LSB
		T _A = -40 °C to 85 °C				
		12 Bit Mode	-1.02	±0.3	1.02	LSB
		T _A = -40 °C to 125 °C (I-grade parts only)				
		10 Bit Mode	-0.5	±0.2	0.5	LSB
Offset Error ³	E _{OFF}	12 Bit Mode	-2	0	2	LSB
		T _A = -40 °C to 85 °C				
		12 Bit Mode	-3	0	3	LSB
		T _A = -40 °C to 125 °C (I-grade parts only)				
		10 Bit Mode	-1	0	1	LSB
		T _A = -40 °C to 85 °C				
		10 Bit Mode	-1	0	1.3	LSB
		T _A = -40 °C to 125 °C (I-grade parts only)				
Offset Temperature Coefficient	TC _{OFF}		—	0.011	—	LSB/°C
Slope Error	E _M	12 Bit Mode	-2.5	—	2.5	LSB
		T _A = -40 °C to 85 °C				
		12 Bit Mode	-2.6	—	2.6	LSB
		T _A = -40 °C to 125 °C (I-grade parts only)				
		10 Bit Mode	-1.1	—	1.1	LSB
Dynamic Performance 10 kHz Sine Wave Input 1 dB below full scale, Max throughput, using AGND pin						
Signal-to-Noise	SNR	12 Bit Mode	64	68	—	dB
		10 Bit Mode	59	61	—	dB
Signal-to-Noise Plus Distortion	SNDR	12 Bit Mode	64	68	—	dB
		10 Bit Mode	59	61	—	dB
Total Harmonic Distortion (Up to 5th Harmonic)	THD	12 Bit Mode	—	-72	—	dB
		10 Bit Mode	—	-69	—	dB
Spurious-Free Dynamic Range	SFDR	12 Bit Mode	—	74	—	dB
		10 Bit Mode	—	71	—	dB

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Negative Hysteresis Mode 3 (CPMD = 11)	HYS _{CP-}	CPHYN = 00	—	-1.5	—	mV
		CPHYN = 01	—	-4	—	mV
		CPHYN = 10	—	-8	—	mV
		CPHYN = 11	—	-16	—	mV
Input Range (CP+ or CP-)	V _{IN}		-0.25	—	V _{IO} +0.25	V
Input Pin Capacitance	C _{CP}		—	7.5	—	pF
Internal Reference DAC Resolution	N _{bits}		6			bits
Common-Mode Rejection Ratio	CMRR _{CP}		—	70	—	dB
Power Supply Rejection Ratio	PSRR _{CP}		—	72	—	dB
Input Offset Voltage	V _{OFF}	T _A = 25 °C	-10	0	10	mV
Input Offset Tempco	TC _{OFF}		—	3.5	—	μV/°

4.1.14 Configurable Logic

Table 4.14. Configurable Logic

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Propagation Delay	t _{DLY}	Through single CLU Using an external pin	—	—	35.3	ns
		Through single CLU Using an internal connection	—	3	—	ns
Clocking Frequency	F _{CLK}	1 or 2 CLUs Cascaded	—	—	73.5	MHz
		3 or 4 CLUs Cascaded	—	—	36.75	MHz

4.1.16 SMBus

Table 4.16. SMBus Peripheral Timing Performance (Master Mode)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Standard Mode (100 kHz Class)						
I2C Operating Frequency	f_{I2C}		0	—	70^2	kHz
SMBus Operating Frequency	f_{SMB}		40^1	—	70^2	kHz
Bus Free Time Between STOP and START Conditions	t_{BUF}		9.4	—	—	μs
Hold Time After (Repeated) START Condition	$t_{HD:STA}$		4.7	—	—	μs
Repeated START Condition Setup Time	$t_{SU:STA}$		9.4	—	—	μs
STOP Condition Setup Time	$t_{SU:STO}$		9.4	—	—	μs
Data Hold Time	$t_{HD:DAT}$		0	—	—	μs
Data Setup Time	$t_{SU:DAT}$		4.7	—	—	μs
Detect Clock Low Timeout	$t_{TIMEOUT}$		25	—	—	ms
Clock Low Period	t_{LOW}		4.7	—	—	μs
Clock High Period	t_{HIGH}		9.4	—	50^3	μs
Fast Mode (400 kHz Class)						
I2C Operating Frequency	f_{I2C}		0	—	256^2	kHz
SMBus Operating Frequency	f_{SMB}		40^1	—	256^2	kHz
Bus Free Time Between STOP and START Conditions	t_{BUF}		2.6	—	—	μs
Hold Time After (Repeated) START Condition	$t_{HD:STA}$		1.3	—	—	μs
Repeated START Condition Setup Time	$t_{SU:STA}$		2.6	—	—	μs
STOP Condition Setup Time	$t_{SU:STO}$		2.6	—	—	μs
Data Hold Time	$t_{HD:DAT}$		0	—	—	μs
Data Setup Time	$t_{SU:DAT}$		1.3	—	—	μs
Detect Clock Low Timeout	$t_{TIMEOUT}$		25	—	—	ms
Clock Low Period	t_{LOW}		1.3	—	—	μs
Clock High Period	t_{HIGH}		2.6	—	50^3	μs

Note:

1. The minimum SMBus frequency is limited by the maximum Clock High Period requirement of the SMBus specification.
2. The maximum I2C and SMBus frequencies are limited by the minimum Clock Low Period requirements of their respective specifications.
3. SMBus has a maximum requirement of 50 μs for Clock High Period. Operating frequencies lower than 40 kHz will be longer than 50 μs . I2C can support periods longer than 50 μs .

6. Pin Definitions

6.1 EFM8BB3x-QFN32 Pin Definitions

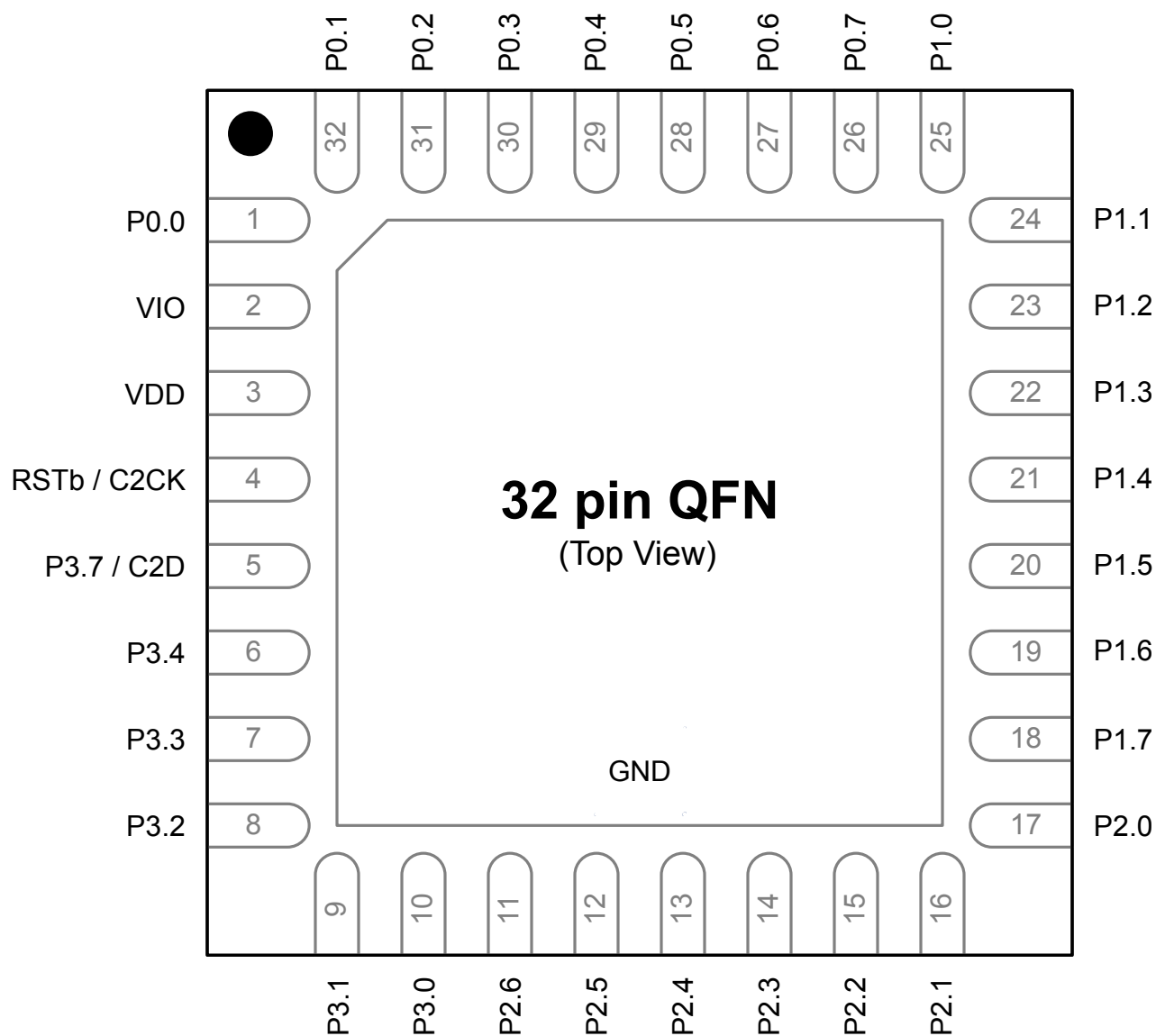


Figure 6.1. EFM8BB3x-QFN32 Pinout

6.2 EFM8BB3x-QFP32 Pin Definitions

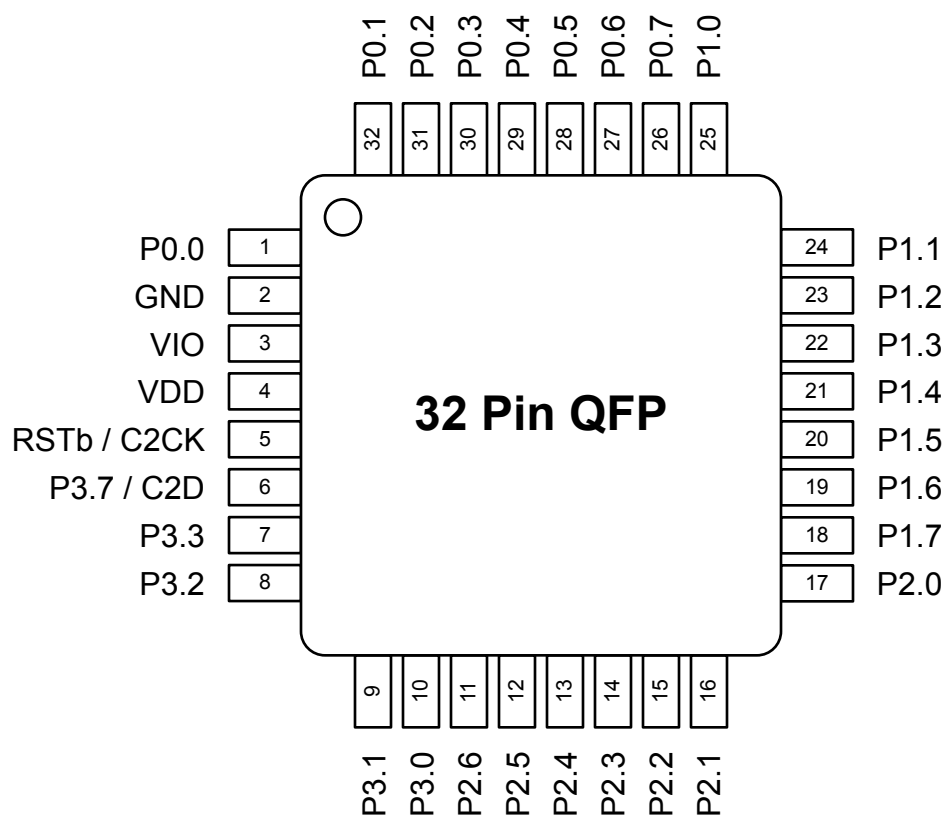


Figure 6.2. EFM8BB3x-QFP32 Pinout

Table 6.2. Pin Definitions for EFM8BB3x-QFP32

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
1	P0.0	Multifunction I/O	Yes	P0MAT.0 INT0.0 INT1.0 CLU0A.8 CLU2A.8 CLU3B.8	VREF
2	GND	Ground			
3	VIO	I/O Supply Power Input			
4	VDD	Supply Power Input			
5	RSTb / C2CK	Active-low Reset / C2 Debug Clock			

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
18	P1.7	Multifunction I/O	Yes	P1MAT.7 CLU0B.15 CLU1B.13 CLU2A.13	ADC0.13 CMP0P.9 CMP0N.9
19	P1.6	Multifunction I/O	Yes	P1MAT.6 CLU0A.15 CLU1B.12 CLU2A.12	ADC0.12
20	P1.5	Multifunction I/O	Yes	P1MAT.5 CLU0B.14 CLU1A.13 CLU2B.13	ADC0.11
21	P1.4	Multifunction I/O	Yes	P1MAT.4 CLU0A.14 CLU1A.12 CLU2B.12	ADC0.10
22	P1.3	Multifunction I/O	Yes	P1MAT.3 CLU0B.13 CLU1B.11 CLU2B.11 CLU3A.13	ADC0.9
23	P1.2	Multifunction I/O	Yes	P1MAT.2 CLU0A.13 CLU1A.11 CLU2B.10 CLU3A.12	ADC0.8 CMP0P.8 CMP0N.8
24	P1.1	Multifunction I/O	Yes	P1MAT.1 CLU0B.12 CLU1B.10 CLU2A.11 CLU3B.13	ADC0.7 CMP0P.7 CMP0N.7

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
2	P0.0	Multifunction I/O	Yes	P0MAT.0 INT0.0 INT1.0 CLU0A.8 CLU2A.8 CLU3B.8	VREF
3	GND	Ground			
4	VDD / VIO	Supply Power Input			
5	RSTb / C2CK	Active-low Reset / C2 Debug Clock			
6	P3.0 / C2D	Multifunction I/O / C2 Debug Data			
7	P2.3	Multifunction I/O	Yes	P2MAT.3 CLU1B.15 CLU2B.15 CLU3A.15	DAC3
8	P2.2	Multifunction I/O	Yes	P2MAT.2 CLU1A.15 CLU2B.14 CLU3A.14	DAC2
9	P2.1	Multifunction I/O	Yes	P2MAT.1 CLU1B.14 CLU2A.15 CLU3B.15	DAC1
10	P2.0	Multifunction I/O	Yes	P2MAT.0 CLU1A.14 CLU2A.14 CLU3B.14	DAC0
11	P1.6	Multifunction I/O	Yes	P1MAT.6 CLU3OUT CLU0A.15 CLU1B.12 CLU2A.12	ADC0.11 CMP1P.5 CMP1N.5

7. QFN32 Package Specifications

7.1 QFN32 Package Dimensions

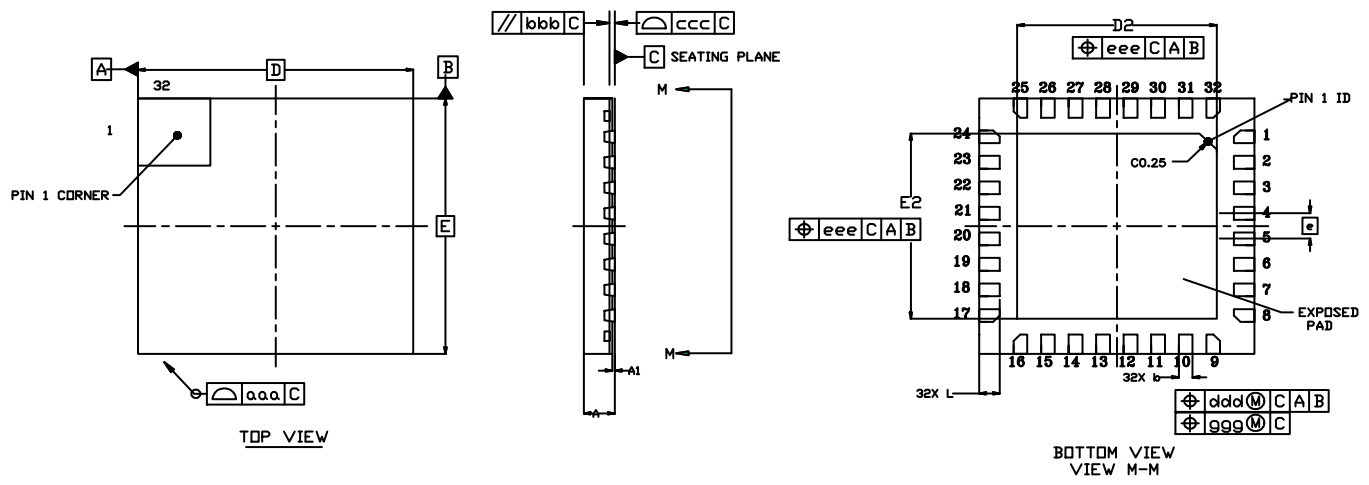


Figure 7.1. QFN32 Package Drawing

Table 7.1. QFN32 Package Dimensions

Dimension	Min	Typ	Max
A	0.45	0.50	0.55
A1	0.00	0.035	0.05
b	0.15	0.20	0.25
D	4.00 BSC.		
D2	2.80	2.90	3.00
e	0.40 BSC.		
E	4.00 BSC.		
E2	2.80	2.90	3.00
L	0.20	0.30	0.40
aaa	—	—	0.10
bbb	—	—	0.10
ccc	—	—	0.08
ddd	—	—	0.10
eee	—	—	0.10
ggg	—	—	0.05

8. QFP32 Package Specifications

8.1 QFP32 Package Dimensions

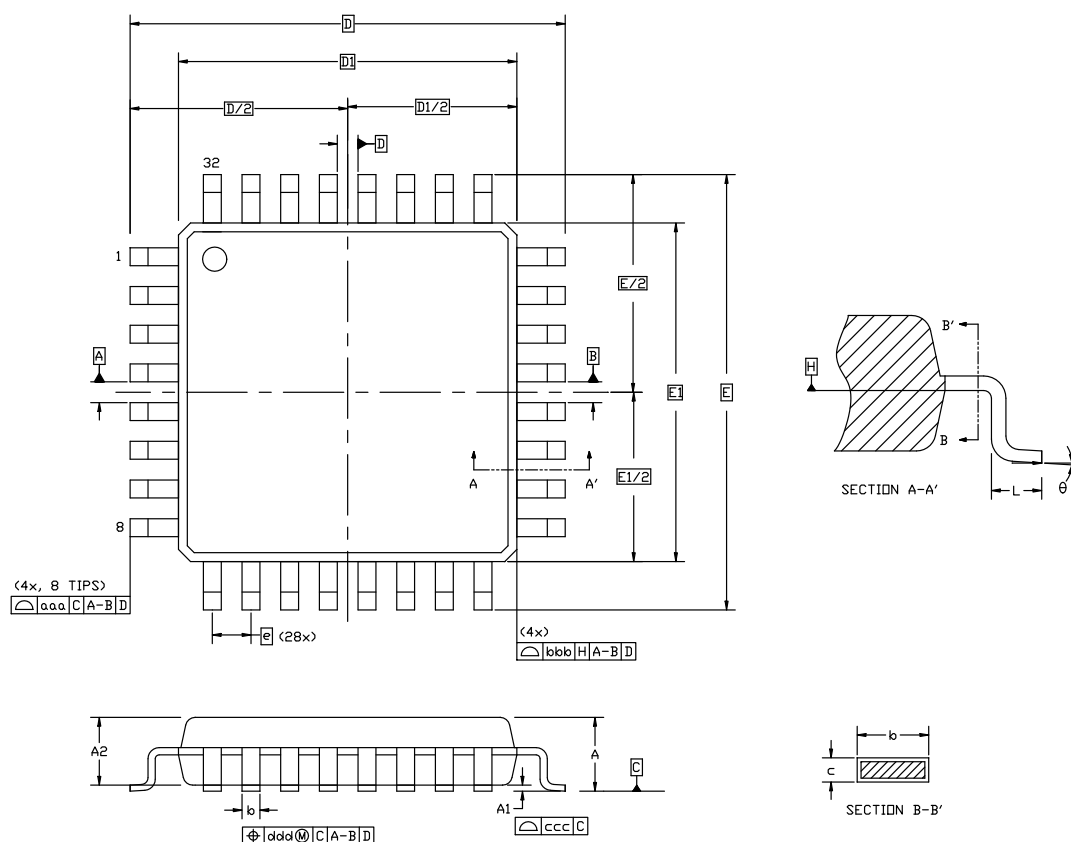


Figure 8.1. QFP32 Package Drawing

Table 8.1. QFP32 Package Dimensions

Dimension	Min	Typ	Max
A	—	—	1.20
A1	0.05	—	0.15
A2	0.95	1.00	1.05
b	0.30	0.37	0.45
c	0.09	—	0.20
D	9.00 BSC		
D1	7.00 BSC		
e	0.80 BSC		
E	9.00 BSC		
E1	7.00 BSC		
L	0.50	0.60	0.70

9. QFN24 Package Specifications

9.1 QFN24 Package Dimensions

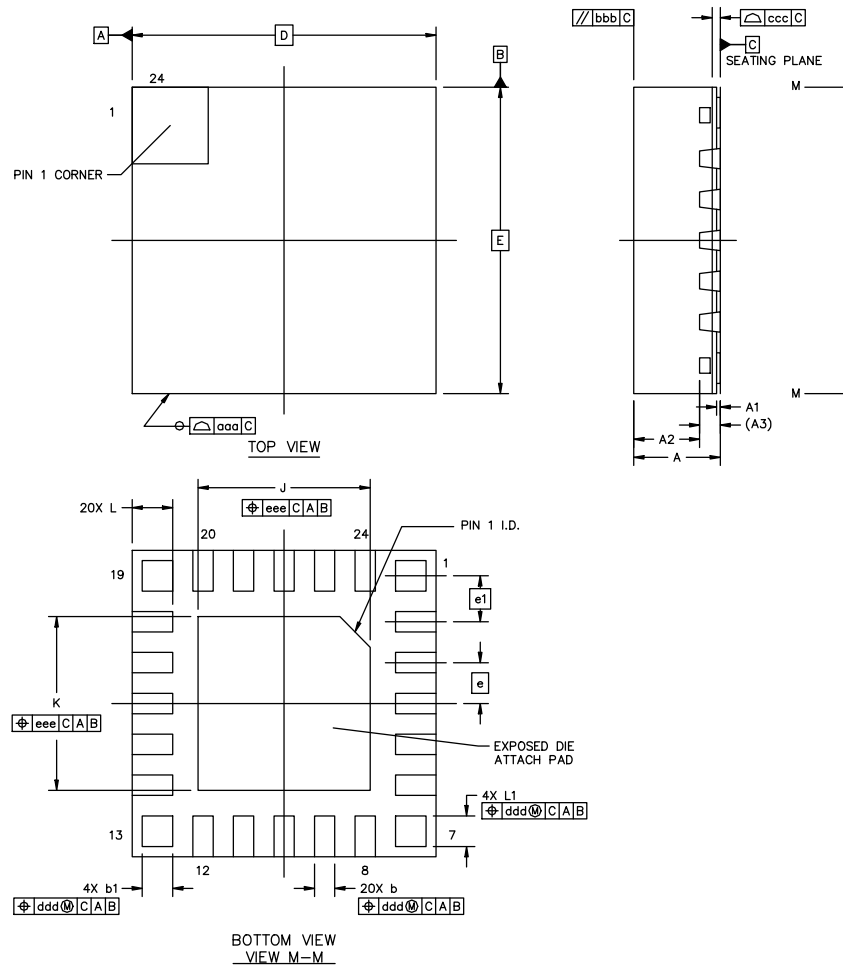


Figure 9.1. QFN24 Package Drawing

Table 9.1. QFN24 Package Dimensions

Dimension	Min	Typ	Max
A	0.8	0.85	0.9
A1	0.00	—	0.05
A2	—	0.65	—
A3	0.203 REF		
b	0.15	0.2	0.25
b1	0.25	0.3	0.35
D	3.00 BSC		
E	3.00 BSC		

10. QSOP24 Package Specifications

10.1 QSOP24 Package Dimensions

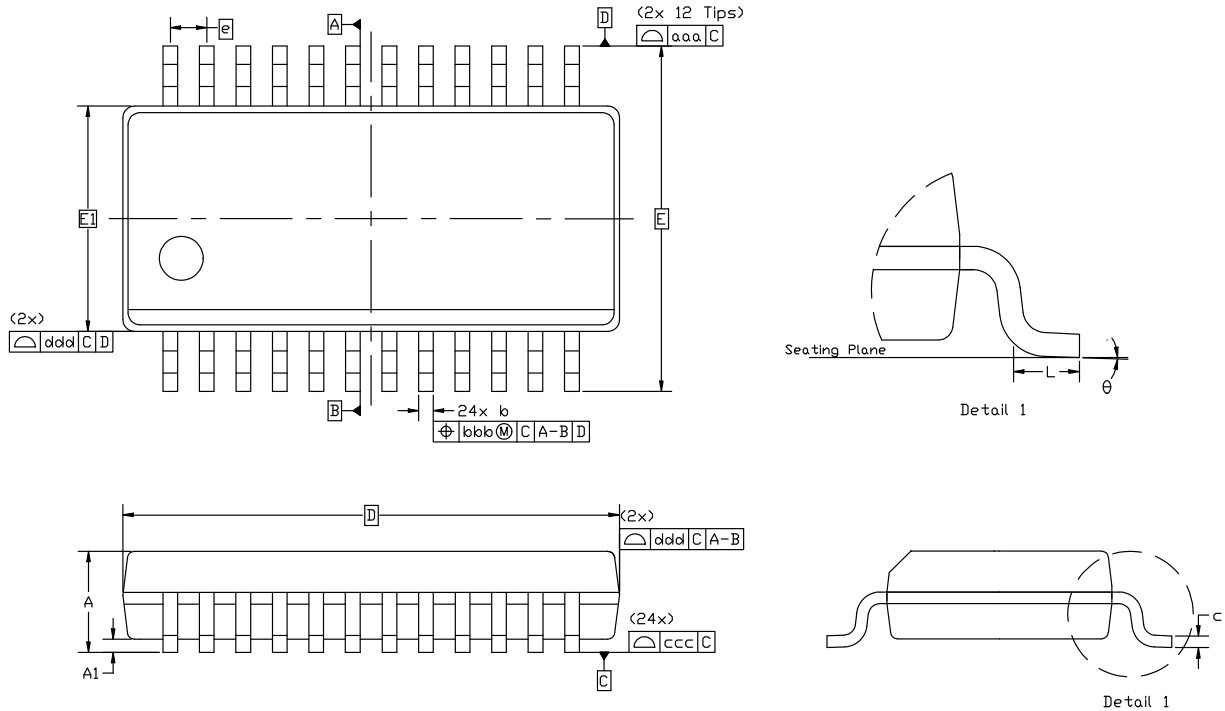


Figure 10.1. QSOP24 Package Drawing

Table 10.1. QSOP24 Package Dimensions

Dimension	Min	Typ	Max
A	—	—	1.75
A1	0.10	—	0.25
b	0.20	—	0.30
c	0.10	—	0.25
D	8.65 BSC		
E	6.00 BSC		
E1	3.90 BSC		
e	0.635 BSC		
L	0.40	—	1.27
theta	0°	—	8°

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