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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

2014110	
Product Status	Discontinued at Digi-Key
Core Processor	CIP-51 8051
Core Size	8-Bit
Speed	50MHz
Connectivity	I ² C, SMBus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	29
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4.25K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 20x10/12b SAR; D/A 4x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-UFQFN Exposed Pad
Supplier Device Package	32-QFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm8bb31f64g-b-qfn32

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

EFM8BB3 Data Sheet Ordering Information

Ordering Part Number	Flash Memory (kB)	RAM (Bytes)	Digital Port I/Os (Total)	Voltage DACs	ADC0 Channels	Comparator 0 Inputs	Comparator 1 Inputs	Pb-free (RoHS Compliant)	Temperature Range	Package
EFM8BB31F64G-B-QSOP24	64	4352	21	4	13	6	7	Yes	-40 to +85 °C	QSOP24
EFM8BB31F32G-B-QFN32	32	2304	29	2 ¹	20	10	9	Yes	-40 to +85 °C	QFN32
EFM8BB31F32G-B-QFP32	32	2304	28	2 ¹	20	10	9	Yes	-40 to +85 °C	QFP32
EFM8BB31F32G-B-QFN24	32	2304	20	2 ¹	12	6	6	Yes	-40 to +85 °C	QFN24
EFM8BB31F32G-B-QSOP24	32	2304	21	2 ¹	13	6	7	Yes	-40 to +85 °C	QSOP24
EFM8BB31F16G-B-QFN32	16	2304	29	2 ¹	20	10	9	Yes	-40 to +85 °C	QFN32
EFM8BB31F16G-B-QFP32	16	2304	28	2 ¹	20	10	9	Yes	-40 to +85 °C	QFP32
EFM8BB31F16G-B-QFN24	16	2304	20	2 ¹	12	6	6	Yes	-40 to +85 °C	QFN24
EFM8BB31F16G-B-QSOP24	16	2304	21	2 ¹	13	6	7	Yes	-40 to +85 °C	QSOP24
EFM8BB31F64I-B-QFN32	64	4352	29	4	20	10	9	Yes	-40 to +125 °C	QFN32
EFM8BB31F64I-B-QFP32	64	4352	28	4	20	10	9	Yes	-40 to +125 °C	QFP32
EFM8BB31F64I-B-QFN24	64	4352	20	4	12	6	6	Yes	-40 to +125 °C	QFN24
EFM8BB31F64I-B-QSOP24	64	4352	21	4	13	6	7	Yes	-40 to +125 °C	QSOP24
EFM8BB31F32I-B-QFN32	32	2304	29	2 ¹	20	10	9	Yes	-40 to +125 °C	QFN32
EFM8BB31F32I-B-QFP32	32	2304	28	2 ¹	20	10	9	Yes	-40 to +125 °C	QFP32
EFM8BB31F32I-B-QFN24	32	2304	20	2 ¹	12	6	6	Yes	-40 to +125 °C	QFN24
EFM8BB31F32I-B-QSOP24	32	2304	21	2 ¹	13	6	7	Yes	-40 to +125 °C	QSOP24
EFM8BB31F16I-B-QFN32	16	2304	29	2 ¹	20	10	9	Yes	-40 to +125 °C	QFN32
EFM8BB31F16I-B-QFP32	16	2304	28	2 ¹	20	10	9	Yes	-40 to +125 °C	QFP32
EFM8BB31F16I-B-QFN24	16	2304	20	2 ¹	12	6	6	Yes	-40 to +125 °C	QFN24
EFM8BB31F16I-B-QSOP24	16	2304	21	2 ¹	13	6	7	Yes	-40 to +125 °C	QSOP24

1. DAC0 and DAC1 are enabled on devices with 2 DACs available.

Low Current Comparators (CMP0, CMP1)

An analog comparator is used to compare the voltage of two analog inputs, with a digital output indicating which input voltage is higher. External input connections to device I/O pins and internal connections are available through separate multiplexers on the positive and negative inputs. Hysteresis, response time, and current consumption may be programmed to suit the specific needs of the application.

The comparator includes the following features:

- · Up to 10 (CMP0) or 9 (CMP1) external positive inputs
- · Up to 10 (CMP0) or 9 (CMP1) external negative inputs
- · Additional input options:
 - Internal connection to LDO output
 - Direct connection to GND
 - Direct connection to VDD
 - · Dedicated 6-bit reference DAC
- Synchronous and asynchronous outputs can be routed to pins via crossbar
- Programmable hysteresis between 0 and ±20 mV
- · Programmable response time
- · Interrupts generated on rising, falling, or both edges
- · PWM output kill feature

3.8 Reset Sources

Reset circuitry allows the controller to be easily placed in a predefined default condition. On entry to this reset state, the following occur:

- The core halts program execution.
- · Module registers are initialized to their defined reset values unless the bits reset only with a power-on reset.
- · External port pins are forced to a known state.
- Interrupts and timers are disabled.

All registers are reset to the predefined values noted in the register descriptions unless the bits only reset with a power-on reset. The contents of RAM are unaffected during a reset; any previously stored data is preserved as long as power is not lost. By default, the Port I/O latches are reset to 1 in open-drain mode, with weak pullups enabled during and after the reset. Optionally, firmware may configure the port I/O, DAC outputs, and precision reference to maintain state through system resets other than power-on resets. For Supply Monitor and power-on resets, the RSTb pin is driven low until the device exits the reset state. On exit from the reset state, the program counter (PC) is reset, and the system clock defaults to an internal oscillator. The Watchdog Timer is enabled, and program execution begins at location 0x0000.

Reset sources on the device include the following:

- Power-on reset
- · External reset pin
- · Comparator reset
- Software-triggered reset
- Supply monitor reset (monitors VDD supply)
- · Watchdog timer reset
- · Missing clock detector reset
- · Flash error reset

3.9 Debugging

The EFM8BB3 devices include an on-chip Silicon Labs 2-Wire (C2) debug interface to allow flash programming and in-system debugging with the production part installed in the end application. The C2 interface uses a clock signal (C2CK) and a bi-directional C2 data signal (C2D) to transfer information between the device and a host system. See the C2 Interface Specification for details on the C2 protocol.

3.10 Bootloader

All devices come pre-programmed with a UART0 bootloader. This bootloader resides in the code security page, which is the last page of code flash; it can be erased if it is not needed.

The byte before the Lock Byte is the Bootloader Signature Byte. Setting this byte to a value of 0xA5 indicates the presence of the bootloader in the system. Any other value in this location indicates that the bootloader is not present in flash.

When a bootloader is present, the device will jump to the bootloader vector after any reset, allowing the bootloader to run. The bootloader then determines if the device should stay in bootload mode or jump to the reset vector located at 0x0000. When the bootloader is not present, the device will jump to the reset vector of 0x0000 after any reset.

More information about the bootloader protocol and usage can be found in *AN945: EFM8 Factory Bootloader User Guide*. Application notes can be found on the Silicon Labs website (www.silabs.com/8bit-appnotes) or within Simplicity Studio by using the [Application Notes] tile.

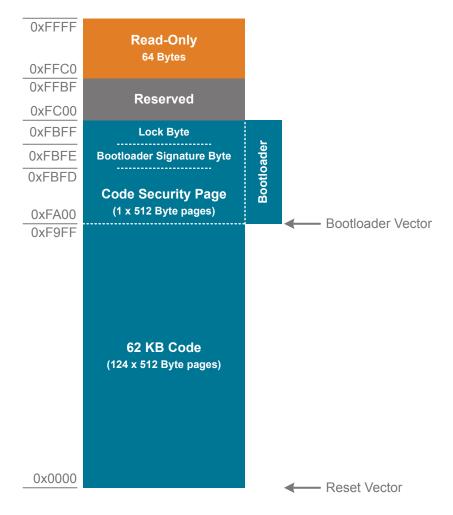


Figure 3.2. Flash Memory Map with Bootloader - 62.5 KB Devices

Bootloader	Pins for Bootload Communication
UART	TX – P0.4
	RX – P0.5

Device Package	Pin for Bootload Mode Entry
QFN32	P3.7 / C2D
QFP32	P3.7 / C2D
QFN24	P3.0 / C2D
QSOP24	P3.0 / C2D

Table 3.3. Summary of Pins for Bootload Mode Entry

4.1.8 Crystal Oscillator

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
Crystal Frequency	f _{XTAL}		0.02	_	25	MHz
Crystal Drive Current	I _{XTAL}	XFCN = 0	_	0.5	_	μA
		XFCN = 1	_	1.5	—	μA
		XFCN = 2	_	4.8	—	μA
		XFCN = 3	_	14	_	μA
		XFCN = 4	_	40	—	μA
		XFCN = 5	_	120	_	μA
		XFCN = 6	_	550	_	μA
		XFCN = 7	_	2.6	-	mA

Table 4.8. Crystal Oscillator

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
Integral Nonlinearity	INL	12 Bit Mode	-1.9	-0.35 / +1	1.9	LSB
		10 Bit Mode	-0.6	±0.2	0.6	LSB
		T _A = -40 °C to 85 °C				
		10 Bit Mode	-0.7	±0.2	0.7	LSB
		T _A = -40 °C to 125 °C (I-grade parts only)				
Differential Nonlinearity (Guaran-	DNL	12 Bit Mode	-0.9	±0.3	0.9	LSB
teed Monotonic)		$T_A = -40 \ ^\circ C \text{ to } 85 \ ^\circ C$				
		12 Bit Mode	-1.02	±0.3	1.02	LSB
		T_A = -40 °C to 125 °C (I-grade parts only)				
		10 Bit Mode	-0.5	±0.2	0.5	LSB
Offset Error ³	E _{OFF}	12 Bit Mode	-2	0	2	LSB
		$T_A = -40 \ ^\circ C \text{ to } 85 \ ^\circ C$				
		12 Bit Mode	-3	0	3	LSB
		T _A = -40 °C to 125 °C (I-grade parts only)				
		10 Bit Mode	-1	0	1	LSB
		$T_A = -40 \ ^\circ C \text{ to } 85 \ ^\circ C$				
		10 Bit Mode	-1	0	1.3	LSB
		T _A = -40 °C to 125 °C (I-grade parts only)				
Offset Temperature Coefficient	TC _{OFF}		_	0.011	—	LSB/°C
Slope Error	EM	12 Bit Mode	-2.5	_	2.5	LSB
		$T_A = -40 \ ^{\circ}C \text{ to } 85 \ ^{\circ}C$				
		12 Bit Mode	-2.6	_	2.6	LSB
		T _A = -40 °C to 125 °C (I-grade parts only)				
		10 Bit Mode	-1.1	_	1.1	LSB
Dynamic Performance 10 kHz Si	ne Wave Inp	out 1 dB below full scale, Max throu	ıghput, using	g AGND pin		
Signal-to-Noise	SNR	12 Bit Mode	64	68	_	dB
		10 Bit Mode	59	61	_	dB
Signal-to-Noise Plus Distortion	SNDR	12 Bit Mode	64	68	—	dB
		10 Bit Mode	59	61		dB
Total Harmonic Distortion (Up to	THD	12 Bit Mode		-72		dB
5th Harmonic)		10 Bit Mode		-69	_	dB
Spurious-Free Dynamic Range	SFDR	12 Bit Mode		74		dB
		10 Bit Mode	_	71	_	dB

4.1.10 Voltage Reference

Table 4.10.	Voltage	Reference
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Parameter	Symbol	Test Condition	Min	Тур	Мах	Unit
Internal Fast Settling Reference						
Output Voltage	V _{REFFS}		1.62	1.65	1.68	V
(Full Temperature and Supply Range)						
Temperature Coefficient	TC _{REFFS}		_	50	—	ppm/°C
Turn-on Time	t _{REFFS}				1.5	μs
Power Supply Rejection	PSRR _{REF} FS		—	400	_	ppm/V
On-chip Precision Reference						
Valid Supply Range	V _{DD}	1.2 V Output	2.2		3.6	V
		2.4 V Output	2.7	_	3.6	V
Output Voltage	VREFP	1.2 V Output, V _{DD} = 3.3 V, T = 25 °C	1.195	1.2	1.205	V
		1.2 V Output	1.18	1.2	1.22	V
		2.4 V Output, V _{DD} = 3.3 V, T = 25 °C	2.39	2.4	2.41	V
		2.4 V Output	2.36	2.4	2.44	V
Turn-on Time, settling to 0.5 LSB	t _{VREFP}	4.7 μF tantalum + 0.1 μF ceramic bypass on VREF pin	_	3	_	ms
		0.1 µF ceramic bypass on VREF pin	—	100	_	μs
Load Regulation	LR _{VREFP}	VREF = 2.4 V, Load = 0 to 200 μ A to GND	_	8	_	μV/μΑ
		VREF = 1.2 V, Load = 0 to 200 μA to GND	_	5	_	μV/μΑ
Load Capacitor	C _{VREFP}	Load = 0 to 200 µA to GND	0.1	_	_	μF
Short-circuit current	ISC _{VREFP}		_	_	8	mA
Power Supply Rejection	PSRR _{VRE}		_	75	-	dB
External Reference		1		1		1
Input Current	I _{EXTREF}	ADC Sample Rate = 800 ksps; VREF = 3.0 V	_	5	_	μΑ

4.1.11 Temperature Sensor

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
Offset	V _{OFF}	T _A = 0 °C		751	—	mV
Offset Error ¹	E _{OFF}	T _A = 0 °C	_	19	—	mV
Slope	М			2.82		mV/°C
Slope Error ¹	E _M		_	29	_	μV/°C
Linearity	LIN	T = -40 °C to 85 °C	_	±0.4	_	°C
		T = -40 °C to 125 °C (I-grade parts only)	_	-0.6 to 1.2	—	°C
Turn-on Time	t _{ON}		_	3.5	_	μs
Note:			1			1

Table 4.11. Temperature Sensor

1. Represents one standard deviation from the mean.

4.1.13 Comparators

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
Response Time, CPMD = 00	t _{RESP0}	+100 mV Differential	_	100	_	ns
(Highest Speed)		-100 mV Differential	_	150	_	ns
Response Time, CPMD = 11 (Low-	t _{RESP3}	+100 mV Differential	_	1.5	_	μs
est Power)		-100 mV Differential	_	3.5	_	μs
Positive Hysteresis	HYS _{CP+}	CPHYP = 00	_	0.4	_	mV
Mode 0 (CPMD = 00)		CPHYP = 01	_	8	_	mV
		CPHYP = 10	_	16	_	mV
		CPHYP = 11	_	32	_	mV
Negative Hysteresis	HYS _{CP-}	CPHYN = 00	_	-0.4	_	mV
Mode 0 (CPMD = 00)		CPHYN = 01	_	-8	_	mV
		CPHYN = 10	_	-16	_	mV
		CPHYN = 11	_	-32	_	mV
Positive Hysteresis	HYS _{CP+}	CPHYP = 00	_	0.5	_	mV
Mode 1 (CPMD = 01)		CPHYP = 01	—	6	_	mV
		CPHYP = 10	_	12	_	mV
		CPHYP = 11	_	24	_	mV
Negative Hysteresis	HYS _{CP-}	CPHYN = 00	_	-0.5	_	mV
Mode 1 (CPMD = 01)		CPHYN = 01	_	-6	_	mV
		CPHYN = 10	—	-12	_	mV
		CPHYN = 11	—	-24	_	mV
Positive Hysteresis	HYS _{CP+}	CPHYP = 00	_	0.7	_	mV
Mode 2 (CPMD = 10)		CPHYP = 01	_	4.5	_	mV
		CPHYP = 10	_	9	_	mV
		CPHYP = 11	_	18	_	mV
Negative Hysteresis	HYS _{CP-}	CPHYN = 00	_	-0.6	_	mV
Mode 2 (CPMD = 10)		CPHYN = 01	_	-4.5	_	mV
		CPHYN = 10	_	-9	_	mV
		CPHYN = 11	_	-18	_	mV
Positive Hysteresis	HYS _{CP+}	CPHYP = 00	_	1.5	_	mV
Mode 3 (CPMD = 11)		CPHYP = 01		4	_	mV
		CPHYP = 10	_	8	_	mV
		CPHYP = 11		16	_	mV

Table 4.13. Comparators

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
Negative Hysteresis	HYS _{CP-}	CPHYN = 00	_	-1.5	_	mV
Mode 3 (CPMD = 11)		CPHYN = 01	—	-4	_	mV
		CPHYN = 10	_	-8	_	mV
		CPHYN = 11	—	-16	—	mV
Input Range (CP+ or CP-)	V _{IN}		-0.25	_	V _{IO} +0.25	V
Input Pin Capacitance	C _{CP}		—	7.5	—	pF
Internal Reference DAC Resolution	N _{bits}			6	1	bits
Common-Mode Rejection Ratio	CMRR _{CP}		_	70	_	dB
Power Supply Rejection Ratio	PSRR _{CP}		_	72	_	dB
Input Offset Voltage	V _{OFF}	T _A = 25 °C	-10	0	10	mV
Input Offset Tempco	TC _{OFF}		_	3.5	_	μV/°

4.1.14 Configurable Logic

Table 4.14. Configurable Logic

Parameter	Symbol	Test Condition	Min	Тур	Мах	Unit
Propagation Delay	t _{DLY}	Through single CLU	—	_	35.3	ns
		Using an external pin				
		Through single CLU	—	3	—	ns
		Using an internal connection				
Clocking Frequency	F _{CLK}	1 or 2 CLUs Cascaded	—	—	73.5	MHz
		3 or 4 CLUs Cascaded			36.75	MHz

6. Pin Definitions

6.1 EFM8BB3x-QFN32 Pin Definitions

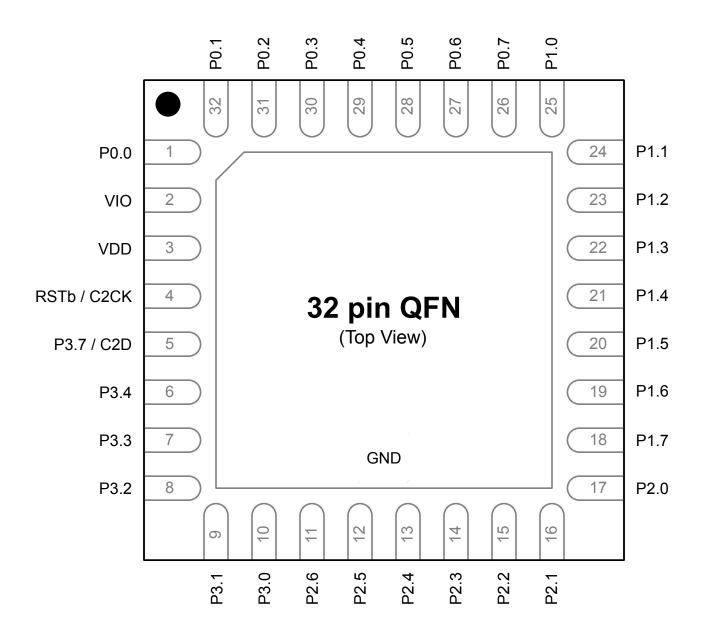


Figure 6.1. EFM8BB3x-QFN32 Pinout

6.3 EFM8BB3x-QFN24 Pin Definitions

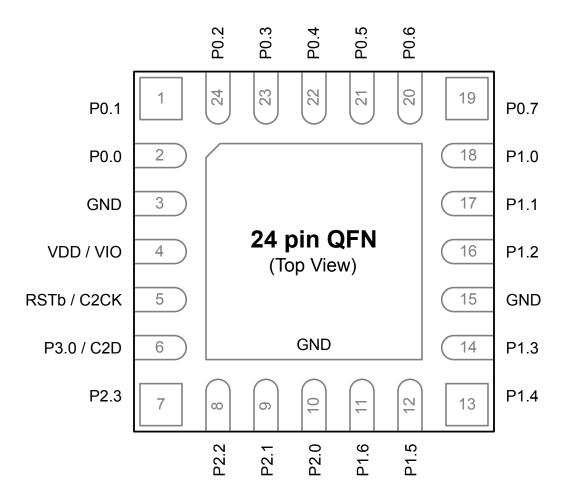




Table 6.3. Pin Definitions for EFM8BB3x-QFN24

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
1	P0.1	Multifunction I/O	Yes	P0MAT.1	ADC0.0
				INT0.1	CMP0P.0
				INT1.1	CMP0N.0
				CLU0B.8	AGND
				CLU2A.9	
				CLU3B.9	

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
2	P0.0	Multifunction I/O	Yes	P0MAT.0	VREF
				INT0.0	
				INT1.0	
				CLU0A.8	
				CLU2A.8	
				CLU3B.8	
3	GND	Ground			
4	VDD / VIO	Supply Power Input			
5	RSTb /	Active-low Reset /			
	C2CK	C2 Debug Clock			
6	P3.0 /	Multifunction I/O /			
	C2D	C2 Debug Data			
7	P2.3	Multifunction I/O	Yes	P2MAT.3	DAC3
				CLU1B.15	
				CLU2B.15	
				CLU3A.15	
8	P2.2	Multifunction I/O	Yes	P2MAT.2	DAC2
				CLU1A.15	
				CLU2B.14	
				CLU3A.14	
9	P2.1	Multifunction I/O	Yes	P2MAT.1	DAC1
				CLU1B.14	
				CLU2A.15	
				CLU3B.15	
10	P2.0	Multifunction I/O	Yes	P2MAT.0	DAC0
				CLU1A.14	
				CLU2A.14	
				CLU3B.14	
11	P1.6	Multifunction I/O	Yes	P1MAT.6	ADC0.11
				CLU3OUT	CMP1P.5
				CLU0A.15	CMP1N.5
				CLU1B.12	
				CLU2A.12	

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
24	P0.2	Multifunction I/O	Yes	P0MAT.2	XTAL1
				INT0.2	ADC0.1
				INT1.2	CMP0P.1
				CLU0OUT	CMP0N.1
				CLU0A.9	
				CLU2B.8	
				CLU3A.8	
Center	GND	Ground			

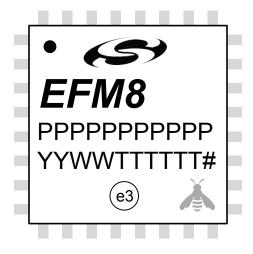


Figure 8.3. QFP32 Package Marking

The package marking consists of:

- PPPPPPP The part number designation.
- TTTTTT A trace or manufacturing code.
- YY The last 2 digits of the assembly year.
- WW The 2-digit workweek when the device was assembled.
- # The device revision (A, B, etc.).

Dimension	Min	Тур	Мах	
е		0.40 BSC		
e1		0.45 BSC		
J	1.60	1.70	1.80	
К	1.60	1.70	1.80	
L	0.35	0.40	0.45	
L1	0.25	0.30	0.35	
ааа	_	0.10	_	
bbb	_	0.10	_	
ссс	_	0.08	_	
ddd	_	0.1	_	
eee	_	0.1	_	

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.

2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.

3. This drawing conforms to JEDEC Solid State Outline MO-248 but includes custom features which are toleranced per supplier designation.

4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

10.2 QSOP24 PCB Land Pattern

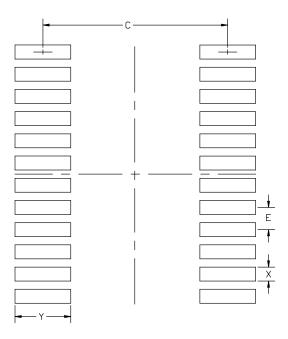


Figure 10.2. QSOP24 PCB Land Pattern Drawing

Dimension	Min	Мах	
С	5.20	5.30	
E	0.635 BSC		
X	0.30	0.40	
Y	1.50	1.60	

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.

2. This land pattern design is based on the IPC-7351 guidelines.

3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.

5. The stencil thickness should be 0.125 mm (5 mils).

6. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.

7. A No-Clean, Type-3 solder paste is recommended.

8. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.



Figure 10.3. QSOP24 Package Marking

The package marking consists of:

- PPPPPPP The part number designation.
- TTTTTT A trace or manufacturing code.
- YY The last 2 digits of the assembly year.
- WW The 2-digit workweek when the device was assembled.
- # The device revision (A, B, etc.).

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