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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Discontinued at Digi-Key
Core Processor	CIP-51 8051
Core Size	8-Bit
Speed	50MHz
Connectivity	I <sup>2</sup> C, SMBus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	28
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4.25K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 20x10/12b SAR; D/A 4x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-QFP
Supplier Device Package	32-QFP (7x7)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/silicon-labs/efm8bb31f64g-b-qfp32r">https://www.e-xfl.com/product-detail/silicon-labs/efm8bb31f64g-b-qfp32r</a>

## 3. System Overview

### 3.1 Introduction

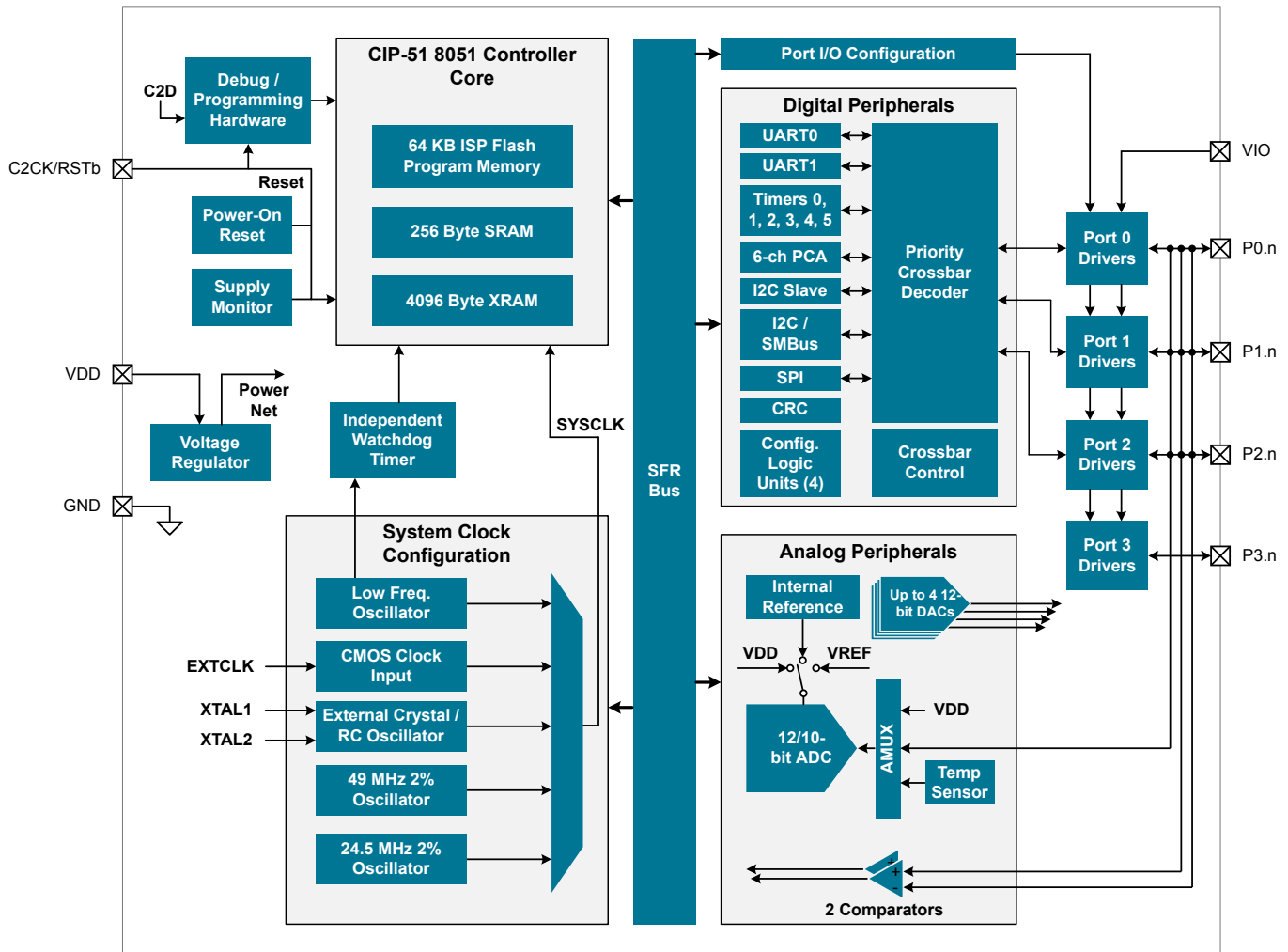


Figure 3.1. Detailed EFM8BB3 Block Diagram

## Low Current Comparators (CMP0, CMP1)

An analog comparator is used to compare the voltage of two analog inputs, with a digital output indicating which input voltage is higher. External input connections to device I/O pins and internal connections are available through separate multiplexers on the positive and negative inputs. Hysteresis, response time, and current consumption may be programmed to suit the specific needs of the application.

The comparator includes the following features:

- Up to 10 (CMP0) or 9 (CMP1) external positive inputs
- Up to 10 (CMP0) or 9 (CMP1) external negative inputs
- Additional input options:
  - Internal connection to LDO output
  - Direct connection to GND
  - Direct connection to VDD
  - Dedicated 6-bit reference DAC
- Synchronous and asynchronous outputs can be routed to pins via crossbar
- Programmable hysteresis between 0 and  $\pm 20$  mV
- Programmable response time
- Interrupts generated on rising, falling, or both edges
- PWM output kill feature

## 3.8 Reset Sources

Reset circuitry allows the controller to be easily placed in a predefined default condition. On entry to this reset state, the following occur:

- The core halts program execution.
- Module registers are initialized to their defined reset values unless the bits reset only with a power-on reset.
- External port pins are forced to a known state.
- Interrupts and timers are disabled.

All registers are reset to the predefined values noted in the register descriptions unless the bits only reset with a power-on reset. The contents of RAM are unaffected during a reset; any previously stored data is preserved as long as power is not lost. By default, the Port I/O latches are reset to 1 in open-drain mode, with weak pullups enabled during and after the reset. Optionally, firmware may configure the port I/O, DAC outputs, and precision reference to maintain state through system resets other than power-on resets. For Supply Monitor and power-on resets, the RSTb pin is driven low until the device exits the reset state. On exit from the reset state, the program counter (PC) is reset, and the system clock defaults to an internal oscillator. The Watchdog Timer is enabled, and program execution begins at location 0x0000.

Reset sources on the device include the following:

- Power-on reset
- External reset pin
- Comparator reset
- Software-triggered reset
- Supply monitor reset (monitors VDD supply)
- Watchdog timer reset
- Missing clock detector reset
- Flash error reset

## 3.9 Debugging

The EFM8BB3 devices include an on-chip Silicon Labs 2-Wire (C2) debug interface to allow flash programming and in-system debugging with the production part installed in the end application. The C2 interface uses a clock signal (C2CK) and a bi-directional C2 data signal (C2D) to transfer information between the device and a host system. See the C2 Interface Specification for details on the C2 protocol.

**Table 3.3. Summary of Pins for Bootload Mode Entry**

Device Package	Pin for Bootload Mode Entry
QFN32	P3.7 / C2D
QFP32	P3.7 / C2D
QFN24	P3.0 / C2D
QSOP24	P3.0 / C2D

#### 4.1.4 Flash Memory

Table 4.4. Flash Memory

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Write Time <sup>1,2</sup>	t <sub>WRITE</sub>	One Byte, F <sub>SYSClk</sub> = 24.5 MHz	19	20	21	μs
Erase Time <sup>1,2</sup>	t <sub>ERASE</sub>	One Page, F <sub>SYSClk</sub> = 24.5 MHz	5.2	5.35	5.5	ms
V <sub>DD</sub> Voltage During Programming <sup>3</sup>	V <sub>PROG</sub>		2.2	—	3.6	V
Endurance (Write/Erase Cycles)	N <sub>WE</sub>		20k	100k	—	Cycles
CRC Calculation Time	t <sub>CRC</sub>	One 256-Byte Block SYSClk = 49 MHz	—	5.5	—	μs

**Note:**

1. Does not include sequencing time before and after the write/erase operation, which may be multiple SYSClk cycles.
2. The internal High-Frequency Oscillator 0 has a programmable output frequency, which is factory programmed to 24.5 MHz. If user firmware adjusts the oscillator speed, it must be between 22 and 25 MHz during any flash write or erase operation. It is recommended to write the HFO0CAL register back to its reset value when writing or erasing flash.
3. Flash can be safely programmed at any voltage above the supply monitor threshold (V<sub>VDDM</sub>).
4. Data Retention Information is published in the Quarterly Quality and Reliability Report.

#### 4.1.5 Power Management Timing

Table 4.5. Power Management Timing

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Idle Mode Wake-up Time	t <sub>IDLEWK</sub>		2	—	3	SYSClks
Suspend Mode Wake-up Time	t <sub>SUS- PENDWK</sub>	SYSClk = HFOSC0 CLKDIV = 0x00	—	170	—	ns
Snooze Mode Wake-up Time	t <sub>SLEEPWK</sub>	SYSClk = HFOSC0 CLKDIV = 0x00	—	12	—	μs

#### 4.1.11 Temperature Sensor

**Table 4.11. Temperature Sensor**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Offset	$V_{OFF}$	$T_A = 0\text{ }^{\circ}\text{C}$	—	751	—	mV
Offset Error <sup>1</sup>	$E_{OFF}$	$T_A = 0\text{ }^{\circ}\text{C}$	—	19	—	mV
Slope	M		—	2.82	—	mV/ $^{\circ}\text{C}$
Slope Error <sup>1</sup>	$E_M$		—	29	—	$\mu\text{V}/^{\circ}\text{C}$
Linearity	LIN	$T = -40\text{ }^{\circ}\text{C}$ to $85\text{ }^{\circ}\text{C}$	—	$\pm 0.4$	—	$^{\circ}\text{C}$
		$T = -40\text{ }^{\circ}\text{C}$ to $125\text{ }^{\circ}\text{C}$ (I-grade parts only)	—	-0.6 to 1.2	—	$^{\circ}\text{C}$
Turn-on Time	$t_{ON}$		—	3.5	—	$\mu\text{s}$
<b>Note:</b> 1. Represents one standard deviation from the mean.						

#### 4.1.16 SMBus

**Table 4.16. SMBus Peripheral Timing Performance (Master Mode)**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>Standard Mode (100 kHz Class)</b>						
I2C Operating Frequency	$f_{I2C}$		0	—	$70^2$	kHz
SMBus Operating Frequency	$f_{SMB}$		$40^1$	—	$70^2$	kHz
Bus Free Time Between STOP and START Conditions	$t_{BUF}$		9.4	—	—	$\mu s$
Hold Time After (Repeated) START Condition	$t_{HD:STA}$		4.7	—	—	$\mu s$
Repeated START Condition Setup Time	$t_{SU:STA}$		9.4	—	—	$\mu s$
STOP Condition Setup Time	$t_{SU:STO}$		9.4	—	—	$\mu s$
Data Hold Time	$t_{HD:DAT}$		0	—	—	$\mu s$
Data Setup Time	$t_{SU:DAT}$		4.7	—	—	$\mu s$
Detect Clock Low Timeout	$t_{TIMEOUT}$		25	—	—	ms
Clock Low Period	$t_{LOW}$		4.7	—	—	$\mu s$
Clock High Period	$t_{HIGH}$		9.4	—	$50^3$	$\mu s$
<b>Fast Mode (400 kHz Class)</b>						
I2C Operating Frequency	$f_{I2C}$		0	—	$256^2$	kHz
SMBus Operating Frequency	$f_{SMB}$		$40^1$	—	$256^2$	kHz
Bus Free Time Between STOP and START Conditions	$t_{BUF}$		2.6	—	—	$\mu s$
Hold Time After (Repeated) START Condition	$t_{HD:STA}$		1.3	—	—	$\mu s$
Repeated START Condition Setup Time	$t_{SU:STA}$		2.6	—	—	$\mu s$
STOP Condition Setup Time	$t_{SU:STO}$		2.6	—	—	$\mu s$
Data Hold Time	$t_{HD:DAT}$		0	—	—	$\mu s$
Data Setup Time	$t_{SU:DAT}$		1.3	—	—	$\mu s$
Detect Clock Low Timeout	$t_{TIMEOUT}$		25	—	—	ms
Clock Low Period	$t_{LOW}$		1.3	—	—	$\mu s$
Clock High Period	$t_{HIGH}$		2.6	—	$50^3$	$\mu s$

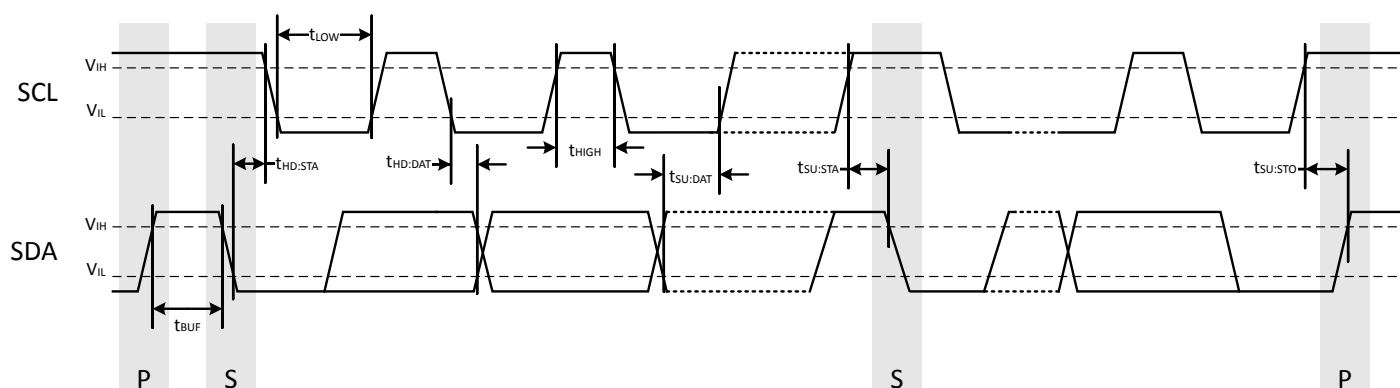
**Note:**

1. The minimum SMBus frequency is limited by the maximum Clock High Period requirement of the SMBus specification.
2. The maximum I2C and SMBus frequencies are limited by the minimum Clock Low Period requirements of their respective specifications.
3. SMBus has a maximum requirement of 50  $\mu s$  for Clock High Period. Operating frequencies lower than 40 kHz will be longer than 50  $\mu s$ . I2C can support periods longer than 50  $\mu s$ .

**Table 4.17. SMBus Peripheral Timing Formulas (Master Mode)**

Parameter	Symbol	Clocks
SMBus Operating Frequency	$f_{\text{SMB}}$	$f_{\text{CSO}} / 3$
Bus Free Time Between STOP and START Conditions	$t_{\text{BUF}}$	$2 / f_{\text{CSO}}$
Hold Time After (Repeated) START Condition	$t_{\text{HD:STA}}$	$1 / f_{\text{CSO}}$
Repeated START Condition Setup Time	$t_{\text{SU:STA}}$	$2 / f_{\text{CSO}}$
STOP Condition Setup Time	$t_{\text{SU:STO}}$	$2 / f_{\text{CSO}}$
Clock Low Period	$t_{\text{LOW}}$	$1 / f_{\text{CSO}}$
Clock High Period	$t_{\text{HIGH}}$	$2 / f_{\text{CSO}}$

**Note:**  
1.  $f_{\text{CSO}}$  is the SMBus peripheral clock source overflow frequency.



**Figure 4.1. SMBus Peripheral Timing Diagram (Master Mode)**

## 4.2 Thermal Conditions

**Table 4.18. Thermal Conditions**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Thermal Resistance	$\theta_{\text{JA}}$	QFN24 Packages	—	30	—	°C/W
		QFN32 Packages	—	26	—	°C/W
		QFP32 Packages	—	80	—	°C/W
		QSOP24 Packages	—	65	—	°C/W

**Note:**  
1. Thermal resistance assumes a multi-layer PCB with any exposed pad soldered to a PCB pad.



## 5. Typical Connection Diagrams

### 5.1 Power

Figure 5.1 Power Connection Diagram on page 33 shows a typical connection diagram for the power pins of the device.

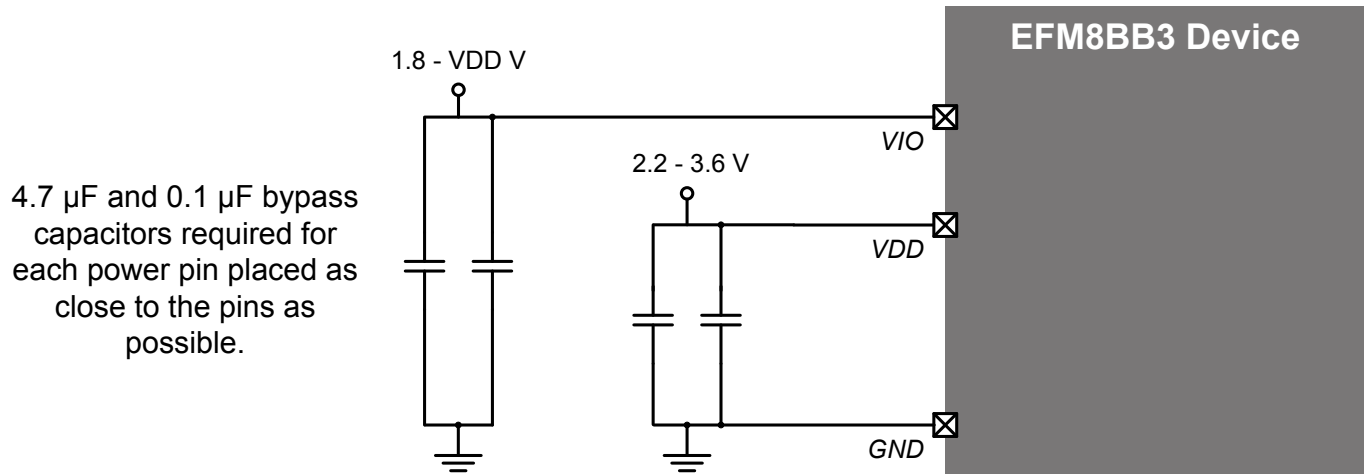


Figure 5.1. Power Connection Diagram

**Table 6.1. Pin Definitions for EFM8BB3x-QFN32**

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
1	P0.0	Multifunction I/O	Yes	P0MAT.0 INT0.0 INT1.0 CLU0A.8 CLU2A.8 CLU3B.8	VREF
2	VIO	I/O Supply Power Input			
3	VDD	Supply Power Input			
4	RSTb / C2CK	Active-low Reset / C2 Debug Clock			
5	P3.7 / C2D	Multifunction I/O / C2 Debug Data			
6	P3.4	Multifunction I/O			
7	P3.3	Multifunction I/O			DAC3
8	P3.2	Multifunction I/O			DAC2
9	P3.1	Multifunction I/O			DAC1
10	P3.0	Multifunction I/O			DAC0
11	P2.6	Multifunction I/O			ADC0.19 CMP1P.8 CMP1N.8
12	P2.5	Multifunction I/O		CLU3OUT	ADC0.18 CMP1P.7 CMP1N.7
13	P2.4	Multifunction I/O			ADC0.17 CMP1P.6 CMP1N.6
14	P2.3	Multifunction I/O	Yes	P2MAT.3 CLU1B.15 CLU2B.15 CLU3A.15	ADC0.16 CMP1P.5 CMP1N.5

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
15	P2.2	Multifunction I/O	Yes	P2MAT.2 CLU2OUT CLU1A.15 CLU2B.14 CLU3A.14	ADC0.15 CMP1P.4 CMP1N.4
16	P2.1	Multifunction I/O	Yes	P2MAT.1 I2C0_SCL CLU1B.14 CLU2A.15 CLU3B.15	ADC0.14 CMP1P.3 CMP1N.3
17	P2.0	Multifunction I/O	Yes	P2MAT.0 I2C0_SDA CLU1A.14 CLU2A.14 CLU3B.14	CMP1P.2 CMP1N.2
18	P1.7	Multifunction I/O	Yes	P1MAT.7 CLU0B.15 CLU1B.13 CLU2A.13	ADC0.13 CMP0P.9 CMP0N.9
19	P1.6	Multifunction I/O	Yes	P1MAT.6 CLU0A.15 CLU1B.12 CLU2A.12	ADC0.12
20	P1.5	Multifunction I/O	Yes	P1MAT.5 CLU0B.14 CLU1A.13 CLU2B.13	ADC0.11
21	P1.4	Multifunction I/O	Yes	P1MAT.4 CLU0A.14 CLU1A.12 CLU2B.12	ADC0.10
22	P1.3	Multifunction I/O	Yes	P1MAT.3 CLU0B.13 CLU1B.11 CLU2B.11 CLU3A.13	ADC0.9

## 6.2 EFM8BB3x-QFP32 Pin Definitions

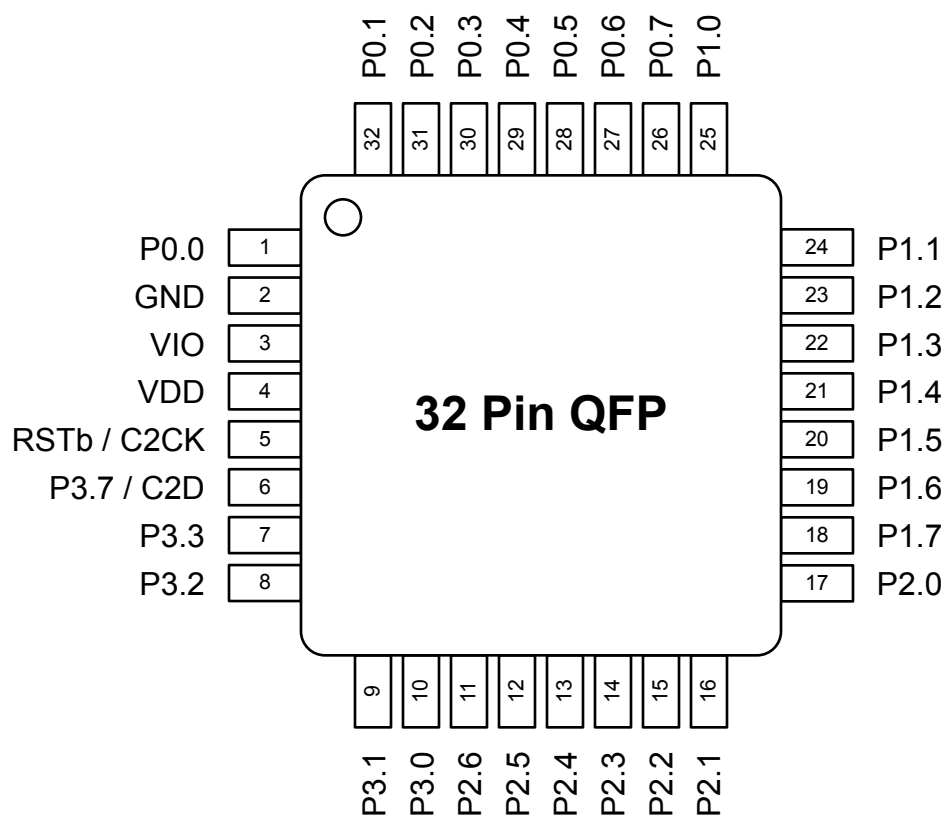


Figure 6.2. EFM8BB3x-QFP32 Pinout

Table 6.2. Pin Definitions for EFM8BB3x-QFP32

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
1	P0.0	Multifunction I/O	Yes	P0MAT.0 INT0.0 INT1.0 CLU0A.8 CLU2A.8 CLU3B.8	VREF
2	GND	Ground			
3	VIO	I/O Supply Power Input			
4	VDD	Supply Power Input			
5	RSTb / C2CK	Active-low Reset / C2 Debug Clock			

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
25	P1.0	Multifunction I/O	Yes	P1MAT.0 CLU1OUT CLU0A.12 CLU1A.10 CLU2A.10 CLU3B.12	ADC0.6 CMP0P.6 CMP0N.6 CMP1P.1 CMP1N.1
26	P0.7	Multifunction I/O	Yes	P0MAT.7 INT0.7 INT1.7 CLU0B.11 CLU1B.9 CLU3A.11	ADC0.5 CMP0P.5 CMP0N.5 CMP1P.0 CMP1N.0
27	P0.6	Multifunction I/O	Yes	P0MAT.6 CNVSTR INT0.6 INT1.6 CLU0A.11 CLU1B.8 CLU3A.10	ADC0.4 CMP0P.4 CMP0N.4
28	P0.5	Multifunction I/O	Yes	P0MAT.5 INT0.5 INT1.5 UART0_RX CLU0B.10 CLU1A.9 CLU3B.11	ADC0.3 CMP0P.3 CMP0N.3
29	P0.4	Multifunction I/O	Yes	P0MAT.4 INT0.4 INT1.4 UART0_TX CLU0A.10 CLU1A.8 CLU3B.10	ADC0.2 CMP0P.2 CMP0N.2

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
30	P0.3	Multifunction I/O	Yes	P0MAT.3 EXTCLK INT0.3 INT1.3 CLU0B.9 CLU2B.9 CLU3A.9	XTAL2
31	P0.2	Multifunction I/O	Yes	P0MAT.2 INT0.2 INT1.2 CLU0OUT CLU0A.9 CLU2B.8 CLU3A.8	XTAL1 ADC0.1 CMP0P.1 CMP0N.1
32	P0.1	Multifunction I/O	Yes	P0MAT.1 INT0.1 INT1.1 CLU0B.8 CLU2A.9 CLU3B.9	ADC0.0 CMP0P.0 CMP0N.0 AGND

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
11	P2.1	Multifunction I/O	Yes	P2MAT.1 CLU1B.14 CLU2A.15 CLU3B.15	DAC1
12	P2.0	Multifunction I/O	Yes	P2MAT.0 CLU1A.14 CLU2A.14 CLU3B.14	DAC0
13	P1.7	Multifunction I/O	Yes	P1MAT.7 CLU0B.15 CLU1B.13 CLU2A.13	ADC0.12 CMP1P.6 CMP1N.6
14	P1.6	Multifunction I/O	Yes	P1MAT.6 CLU3OUT CLU0A.15 CLU1B.12 CLU2A.12	ADC0.11 CMP1P.5 CMP1N.5
15	P1.5	Multifunction I/O	Yes	P1MAT.5 CLU2OUT CLU0B.14 CLU1A.13 CLU2B.13	ADC0.10 CMP1P.4 CMP1N.4
16	P1.4	Multifunction I/O	Yes	P1MAT.4 I2C0_SCL CLU0A.14 CLU1A.12 CLU2B.12	ADC0.9 CMP1P.3 CMP1N.3
17	P1.3	Multifunction I/O	Yes	P1MAT.3 I2C0_SDA CLU0B.13 CLU1B.11 CLU2B.11 CLU3A.13	CMP1P.2 CMP1N.2

## 7.2 QFN32 PCB Land Pattern

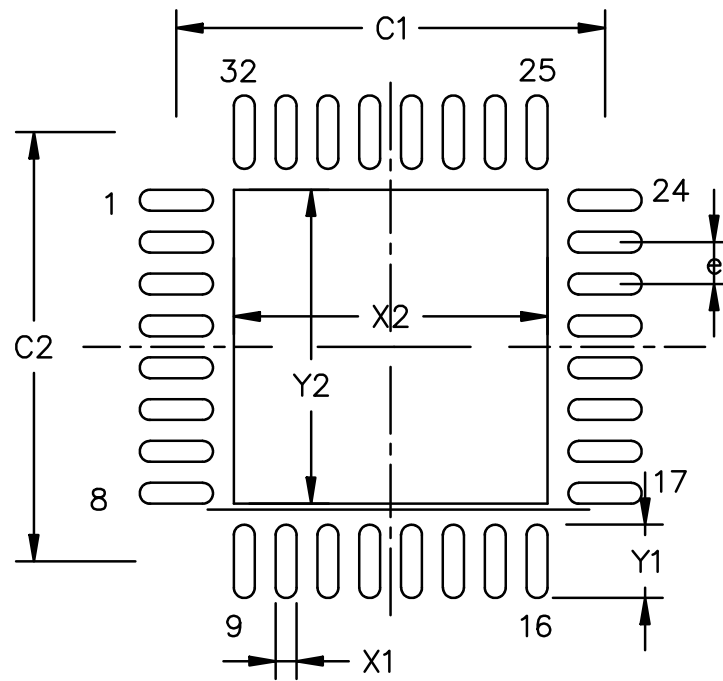


Figure 7.2. QFN32 PCB Land Pattern Drawing

Table 7.2. QFN32 PCB Land Pattern Dimensions

Dimension	Min	Max
C1	—	4.10
C2	—	4.10
X1	—	0.2
X2	—	3.0
Y1	—	0.7
Y2	—	3.0
e	—	0.4



Dimension	Min	Max
<b>Note:</b> <ol style="list-style-type: none"> <li>1. All dimensions shown are in millimeters (mm) unless otherwise noted.</li> <li>2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.</li> <li>3. This Land Pattern Design is based on the IPC-SM-782 guidelines.</li> <li>4. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.</li> <li>5. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.</li> <li>6. The stencil thickness should be 0.125 mm (5 mils).</li> <li>7. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.</li> <li>8. A 2 x 1 array of 0.7 mm x 1.6 mm openings on a 0.9 mm pitch should be used for the center pad.</li> <li>9. A No-Clean, Type-3 solder paste is recommended.</li> <li>10. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.</li> </ol>		

### 9.3 QFN24 Package Marking

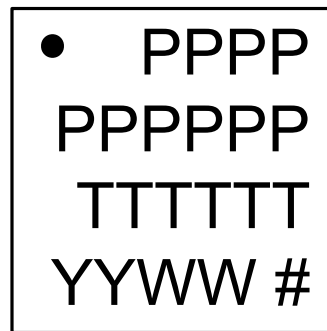


Figure 9.3. QFN24 Package Marking

The package marking consists of:

- P P P P P P P P – The part number designation.
- T T T T T T – A trace or manufacturing code.
- Y Y – The last 2 digits of the assembly year.
- W W – The 2-digit workweek when the device was assembled.
- # – The device revision (A, B, etc.).

## 10. QSOP24 Package Specifications

### 10.1 QSOP24 Package Dimensions

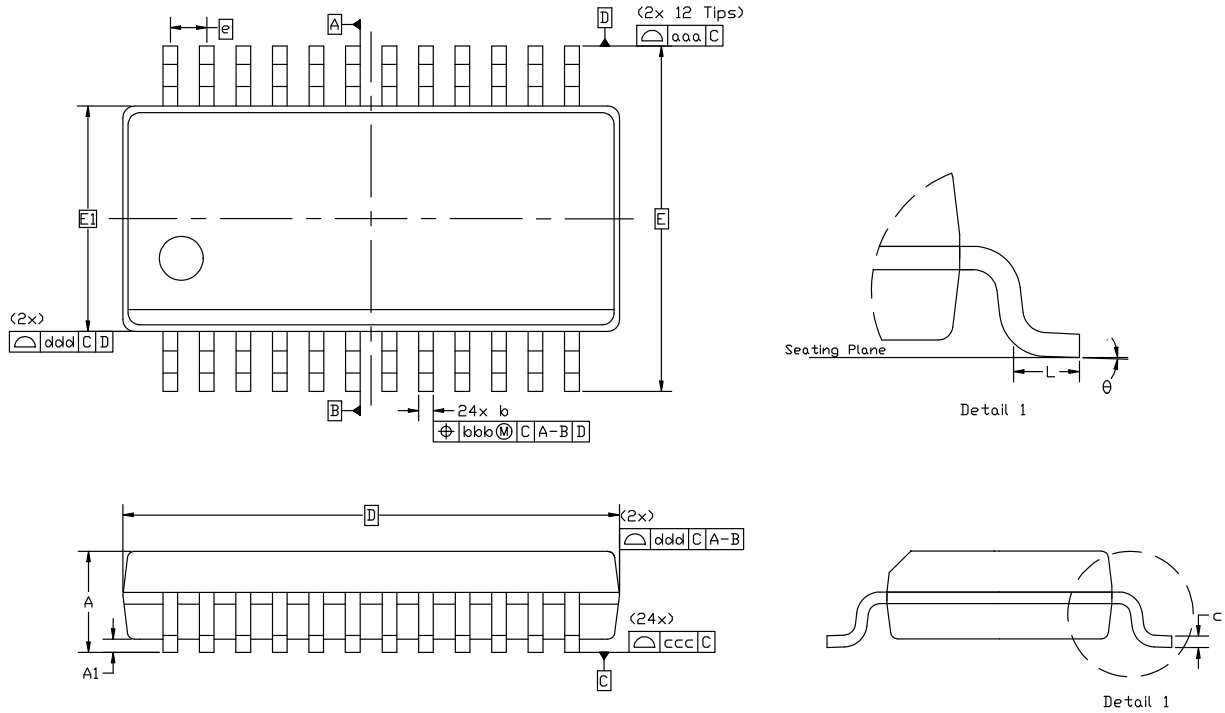
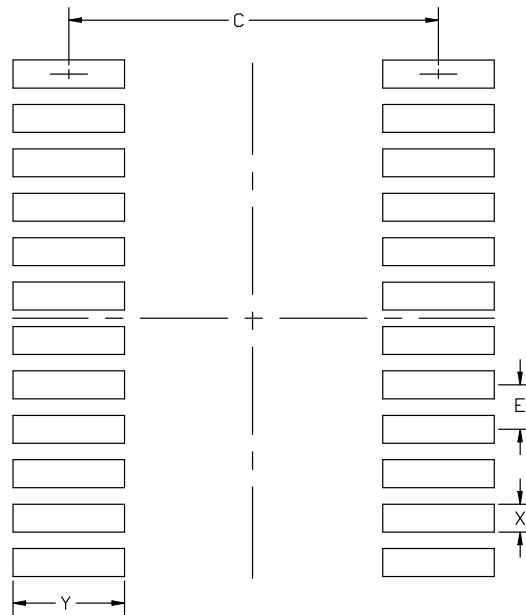


Figure 10.1. QSOP24 Package Drawing

Table 10.1. QSOP24 Package Dimensions

Dimension	Min	Typ	Max
A	—	—	1.75
A1	0.10	—	0.25
b	0.20	—	0.30
c	0.10	—	0.25
D	8.65 BSC		
E	6.00 BSC		
E1	3.90 BSC		
e	0.635 BSC		
L	0.40	—	1.27
theta	0°	—	8°

## 10.2 QSOP24 PCB Land Pattern



**Figure 10.2. QSOP24 PCB Land Pattern Drawing**

**Table 10.2. QSOP24 PCB Land Pattern Dimensions**

Dimension	Min	Max
C	5.20	5.30
E	0.635 BSC	
X	0.30	0.40
Y	1.50	1.60

**Note:**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This land pattern design is based on the IPC-7351 guidelines.
3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60  $\mu$ m minimum, all the way around the pad.
4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
7. A No-Clean, Type-3 solder paste is recommended.
8. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

## 11. Revision History

### 11.1 Revision 1.01

October 21st, 2016

Updated [Figure 2.1 EFM8BB3 Part Numbering on page 2](#) to include the I-grade description.

Updated QFN24 center pad stencil description.

### 11.2 Revision 1.0

September 6th, 2016

Filled in all TBD values in [4. Electrical Specifications](#).

Added a note regarding which DACs are available to [Table 2.1 Product Selection Guide on page 2](#).

Added specifications for [4.1.16 SMBus](#).

Added bootloader pinout information to [3.10 Bootloader](#).

Added CRC Calculation Time to [4.1.4 Flash Memory](#).

### 11.3 Revision 0.4

May 12th, 2016

Filled in TBD values for DAC Integral Nonlinearity in [Table 4.12 DACs on page 26](#).

Added I-grade devices.

Adjusted the Total Current Sunk into Supply Pin and Total Current Sourced out of Ground Pin specifications in [4.3 Absolute Maximum Ratings](#).

Added Operating Junction Temperature specification to [4.3 Absolute Maximum Ratings](#).

### 11.4 Revision 0.3

February 10th, 2016

Added EFM8831F16G-A-QFN24 to [Table 2.1 Product Selection Guide on page 2](#).

Updated [Figure 5.2 Debug Connection Diagram on page 34](#) to move the pull-up resistor on C2D / RSTb to after the series resistor instead of before.

Added mention of the pre-programmed bootloader in [1. Feature List](#).

Added a reference to *AN945: EFM8 Factory Bootloader User Guide* in [3.10 Bootloader](#).

Updated all part numbers to revision B.

Adjusted C1, C2, X2, Y2, and Y1 maximums for [7.2 QFN32 PCB Land Pattern](#).

Adjusted package markings for QFN32 and QSOP24 packages.

Filled in TBD minimum and maximum values for DAC Differential Nonlinearity in [Table 4.12 DACs on page 26](#).

### 11.5 Revision 0.2

Added information on the bootloader to [3.10 Bootloader](#).

Updated some characterization TBD values.

### 11.6 Revision 0.1

Initial release.

Silicon Labs

# Simplicity Studio™4



## Simplicity Studio

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